

Requirements for robust $2e$ periodicity in single-Cooper-pair transistors*

José AUMENTADO,[†] Mark W. KELLER, and John M. MARTINIS¹

National Institute of Standards and Technology
¹325 Broadway MS 814.03
 Boulder, CO 80305-3337

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The superconducting analog of the single-electron transistor (SET), the single-Cooper-pair transistor (SCPT), is composed of two ultras-small tunnel junctions in series forming an island (see Figure 1(a)). Transport through the SCPT depends on the electrostatic energy required to charge the island, as in the SET, and also on the Josephson coupling across the junctions. An SCPT was first demonstrated Fulton *et al.* in 1989,¹⁾ and interest has been renewed with recent work on SCPT-based qubits that have recently demonstrated coherence times on the order of $1 \mu\text{s}$.²⁾ In this paper, we address a long-standing question: What are the practical requirements for obtaining SCPT devices in which coherent transport of Cooper pairs is truly dominant, as required by various applications? We show that a controlled change in the spatial profile of the superconducting energy gap affects this transport dramatically.

As the current through an SCPT increases, it first follows a superconducting branch very near zero voltage and then switches to a finite voltage on a resistive branch, similar to a single Josephson junction. The switching current I_{sw} may be modulated by an applied gate voltage that biases the effective island charge by $C_g V_g$. If all electrons on the island are paired (the “even” state), $I_{sw}(V_g)$ is periodic with period $2e$, reflecting the charge of a Cooper pair. If an unpaired quasiparticle (QP) is present on the island (the “odd” state), the switching current is predominantly $1e$ periodic, an effect known as “quasiparticle poisoning.”³⁾

Early work on SCPTs did produced neither the desired $2e$ period, nor an understanding of why it was absent.¹⁾ In a breakthrough experiment, Joyez *et al.* demonstrated SCPTs with robust $2e$ periodicity using normal-metal regions in contact with the superconducting leads very close to the island.⁴⁾ It was believed that these normal metal contacts absorbed stray QPs and were termed “quasiparticle traps.”

While the Joyez work demonstrated an almost un-failing ability to produce purely even parity devices, other groups have seen $2e$ without QP traps.⁵⁾ It is not clear from the literature whether other groups have shown the same yield with or without these traps. At best, one can refer to the Joyez methodology for fabrication and measurement and wonder what is different amongst the other groups in these same respects. Ultimately, the mystery

seems to lie in the fact that one can obtain $2e$ periodicity *without* QP traps. This paper is concerned with the reasons for this disparity in experimental results and how one can produce robust devices at will without employing QP traps.

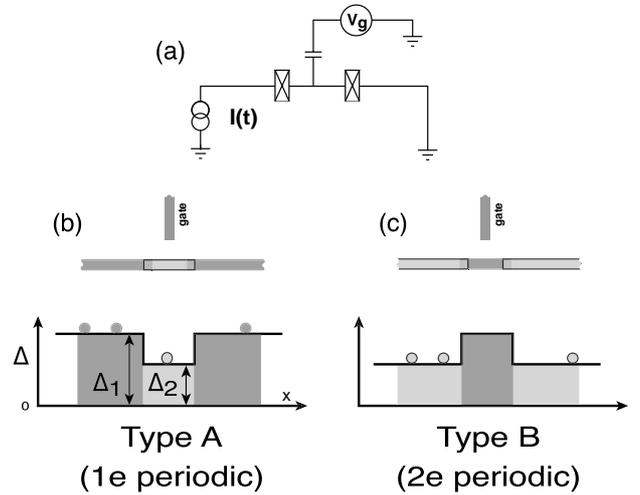


Fig. 1. (a) Schematic of SCPT device. (b)&(c) Device geometries illustrating different gaps ($\Delta_1 > \Delta_2$) in the leads and the islands with the corresponding gap profiles that QPs diffuse in. In (b) the island has a smaller gap than the leads and therefore becomes a trap. In (c) the higher gap of the island provides a potential barrier to QP tunneling.

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Almost all SCPTs studied in the literature have been fabricated using two-angle shadow evaporation of Al. Although both depositions are performed in the same session, the two Al layers may have different impurity levels due to outgassing of the deposition chamber and gettering of the Al source after it is heated. These impurities can affect the superconducting gap energy of Al, resulting in different values Δ_1 and Δ_2 for the first and second depositions. This creates a spatial profile of Δ which may dramatically influence QP poisoning. Typically, the SCPT island is comprised entirely of one deposition and the leads are formed from the other. This leads to the two types of devices shown in Figs. 1(b) and 1(c). In type A, QPs on the island see a barrier of $\Delta_1 - \Delta_2$ on either side and may remain on the island for a long time if the thermal energy kT is less than this barrier. In type B, QPs can easily leave the island.

Based on the discussion above, we expect $I_{sw}(V_g)$ to

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[†] jose.aumentado@boulder.nist.gov

have a period of $1e$ for devices of type A and $2e$ for type B. We tested this by making sets of co-deposited and nearly identical SCPTs with mirror symmetry so that each set contained both type A and type B devices. Starting from a base pressure of $\simeq 3 \times 10^{-7}$ mbar, we deposited 20 nm for the Δ_1 layer in a pressure of $\simeq 5 \times 10^{-6}$ mbar of O_2 . We then formed the junction oxide with $\simeq 130$ mbar of O_2 for 5 minutes, rotated the substrate to the second angle, and deposited 30 nm for the Δ_2 layer without extra O_2 . The first deposition was thus “dirtier” than the second⁶⁾ and had a higher gap energy. The actual geometry is similar to that shown in Fig. 1, with a lead width of 100 nm, junction area of $100 \text{ nm} \times 100 \text{ nm}$, and island size of $100 \text{ nm} \times 800 \text{ nm}$. From measurements in the normal state, we found a total resistance of 14 k Ω to 20 k Ω and a single-electron charging energy E_c of 130 μeV to 160 μeV .

We measured the zero-bias resistance of the SCPTs to determine the superconducting transition temperature, and thus the gap energy⁷⁾ of each deposition. This method gives the same value as a conventional transition temperature measurement of a thin wire of co-deposited Al from each layer. We find $\Delta_1 - \Delta_2 \sim 20\text{--}40 \mu\text{eV}$, which is much larger than $kT \simeq 2.5 \mu\text{eV}$ at a temperature of 30 mK.

We measured $I_{sw}(V_g)$ in a dilution refrigerator at $T=30$ mK using a two-probe, current-biased configuration with current source resistors of 100 k Ω to 10 M Ω at room temperature. The current was ramped at rates below 1 $\mu\text{A/s}$ with a sawtooth function offset to cycle only through the positive hysteresis loop in the IV . We recorded I_{sw} at each V_g for many cycles to accumulate histograms of I_{sw} vs. V_g . Typical results for type A and type B devices with nearly identical junction parameters, plotted in Fig. 2, show that the effect of the gap profile is profound. When the island has a lower gap, I_{sw} is fully poisoned, modulating with a period of $1e$. When the island has a higher gap, the poisoning is negligible, yielding a period of $2e$. We have seen this behavior in three sets of devices deposited in this manner, encompassing a total of 18 SCPTs, demonstrating that this fabrication method consistently avoids QP poisoning.

remains the subject of some debate.

Our work has several implications for understanding QP poisoning in SCPT devices. It must be understood that the presence of $2e$ periodicity in type B devices does not indicate that QPs are completely absent, since neighboring type A devices are still strongly poisoned. Even at low temperatures, there are significant numbers of QPs diffusing through the device. These nonequilibrium QPs may be generated by excess noise, some of which may be eliminated through careful filtering of the leads, but in practice may be impossible to eliminate completely. The most notable result of our work is that the gap profile engineered into the type B devices provides them with a

degree of immunity to QP poisoning. In this context, the QP traps used previously by other groups⁴⁾ may have not only had the effect of absorbing some of these roaming QPs, but may have also depressed the gap in the leads to below the island gap due to the proximity effect. This may explain the necessity for placing these traps very

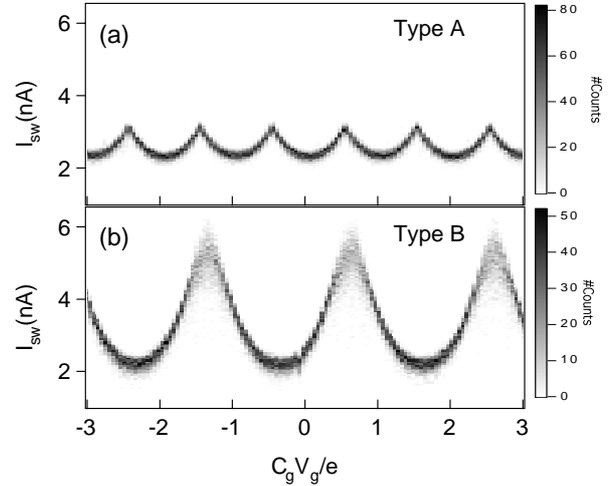


Fig. 2. I_{sw} histograms vs. effective gate charge $C_g V_g / e$ for SCPT devices in which (a) the island gap is lower than the lead gap and (b) the lead gap is lower than the island gap. $\Delta_1 = 230 \mu\text{eV}$ and $\Delta_2 = 190 \mu\text{eV}$. The two devices had nearly identical junction parameters: $R_{tot} \sim 20 \text{ k}\Omega$ and $E_c = 160 \mu\text{eV}$. Note: Random offset charges have not been subtracted out.

close (within 1 μm) to the SCPT junctions.

To summarize, we have resolved a longstanding mystery concerning QP poisoning, and perhaps more importantly, demonstrated an approach to fortifying SCPT devices against this effect. We believe that gap profile engineering will be critical for many applications of SCPT devices, most notably Cooper-pair qubits in which the presence of a single QP can destroy the delicate superposition of Cooper pair number states and may play a subtle role in decoherence outside of the island.

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