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Experimental investigation of the dielectric-semiconductor interface with scanning capacitance microscopy

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Abstract

An experimental investigation of how interface states effect scanning capacitance microscopy (SCM) measurements is presented. Different sample polishing procedures were used to make SCM samples that would have different interface state densities, but identical oxide thicknesses. By comparing SCM signals of these samples, the effect of interface states could be singled out. The interface states of these SCM samples were found to have an amphoteric energy distribution. The magnitude of the maximum SCM signals (maximum dC/dV in dC/dV versus dc bias, V_{dc}, plots) is independent of the interface-trapped charges, while the full width at half maximum (FWHM) of the dC/dV–V_{dc} curves is broadened with the interface states. The physics of SCM interface states effect is also discussed.

1. Introduction

Scanning capacitance microscopy (SCM) is a promising technique for quantitative 2-D dopant profiling of semiconductor devices, which has been identified as an urgent need for next-generation silicon devices in the International Technology Roadmap for Semiconductors. Requirements for quantitative dopant profiling are for 2 nm spatial resolution and 2% accuracy by 2016 [1]. To achieve this goal, recent research has concentrated on: improvement of spatial resolution by reducing the tip size [2] or using beveled samples [3,4]; improved understanding of the physics of interface charges [5–9] and the effect of the atomic force microscopy (AFM) laser on the measurement [10–12]; the carrier spilling effect for beveled samples [3,4]; and improved dopant profile extraction techniques [13].

As a mobile, high-spatial-resolution (to 10 nm) MOS C–V probe, the SCM tip is a useful tool with which to examine local variations in dielectric thin film quality and local variations in semiconductor substrate properties. However, the 3-D nature of the SCM tip results in differences in interpretation as compared to the established 1-D models. The purpose of this work is to better understand SCM based C–V measurements of MIS structures and develop interpretation schemes to extract the electrical properties from such structures.

The signal in SCM is the differential capacitance, dC/dV, of an MOS structure comprised of the SCM metal probe tip, a dielectric layer, and the underlying semiconductor. Both experimental and simulation evidences have shown that surface charges and interface states

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have an effect on SCM dC/dV versus dc bias characteristics. In conventional silicon MOS C–V measurements, interface states will cause a stretch-out in the high frequency C–V curve, thus resulting in a reduction of the maximum dC/dV (typically, by a factor of about 2 [14]). However, to date, no experimental evidence has been obtained to show whether interface states will give a similar effect in SCM measurements. Previous published work showed that interface states cause a flatband voltage shift and a broadening of the full width at half maximum (FWHM) of SCM dC/dV–V_{dc} curves [5]. The maximum dC/dV values obtained from samples of different interface densities could not be compared [5,8], because the samples had different oxide thicknesses. Hence, the effect of interface states on SCM measurements is still not fully understood.

For this work, we made SCM samples with different interface densities and identical oxide thicknesses in order to investigate the effect of interface states on SCM dC/dV signals. SCM samples with varying surface roughnesses were created by using diamond and colloidal silica suspensions of different particle sizes as the final step of the typical SCM sample polish process [15]. Greater surface roughness contributes more silicon dangling bond defects on the sample surfaces, resulting in higher interface state densities after oxidation [16].

2. Experimental procedures

Both unipolar and p–n junction samples were used in this study. The unipolar samples were p-type silicon (100) wafers with a uniform dopant concentration of $1 \times 10^{16}\ \mathrm{cm}^{-3}$. The p–n junction samples consisted of an n-type epitaxial layer (doped at $4.6 \times 10^{15}\ \mathrm{cm}^{-3}$, 12.2 μm thickness) and a (110) p$^+$ substrate (doped at $2.3 \times 10^{18}\ \mathrm{cm}^{-3}$).

Three experiments were performed. The first experiment was to investigate the dependence of the maximum SCM dC/dV signal on interface states. Here the unipolar sample was polished using a standard procedure, which was then terminated with a final polishing step of 0.02 μm colloidal silica suspension, 0.25, 0.5, 1.0 μm diamond slurry, or 0.1 μm diamond lapping film (samples named here as 1-1, 1-2, 1-3, 1-4, and 1-5, respectively). After each polishing process, the sample was cleaned and oxidized in an UV-ozone photoreactor for 20 min at room temperature, giving nearly a native oxide (∼2 nm thick) [17]. The dC/dV–V_{dc} curves were measured directly after the UV-ozone oxidation process using the same SCM tip (PtIr5 coated EFM tips from Nanosensors) and SCM operational conditions. The second experiment was conducted on two pieces of the unipolar sample. These two pieces were polished and finished using 0.02 μm colloidal silica suspension (sample 2-1) and 0.25 μm diamond slurry (sample 2-2). After UV-ozone oxidation, the two samples were oxidized at the same time at 300 °C in 5% ozone/95% oxygen for 2 h, giving both samples an oxide thickness of around 4 nm [18]. The dC/dV–V_{dc} curves of these two samples were measured with 20 kHz ac tip biases, V_{ac}, of different amplitudes to investigate the interface state response to V_{ac}. The third experiment was conducted on the p–n junction sample. Two pieces of the samples were polished using 0.02 μm colloidal silica suspension and 0.5 m diamond slurry (samples 3-1 and 3-2, respectively). Sample 3-1 was oxidized at 300 °C in 4.5% ozone for 1 h and sample 3-2 was oxidized at 280 °C in 5% ozone for 1 h, resulting in a slightly thicker oxide on sample 3-2. The dC/dV–V_{dc} curves in the n- and p$^+$-type neutral regions were then measured, which revealed some information about the energy distribution of the interface states.

The SCM measurements were performed using a Veeco Nanoscope IIIa [1] Atomic Force Microscope. All the dC/dV signals were detected in the true dark condition (i.e., with the AFM laser off) to avoid the photovoltaic effect of the AFM laser illumination on the SCM signal. Details concerning the ozone enhanced oxidation facilities can be found in [17].

3. Results and conclusions

The rms surface roughness of samples 1-1, 1-2, 1-3, 1-4, and 1-5, calculated from an AFM image are 0.23, 0.48, 0.77, 1.07, and 1.95 nm, respectively. Fig. 1 shows the dC/dV–V_{tip} curves of these five samples, averaged over 40 measurements to suppress noise. Note that V_{dc} is applied with the tip grounded. The tip dc voltage, $V_{tip} = -V_{dc}$, corresponds to the usual gate bias of a MOS capacitor. Fig. 1 shows that the magnitude of the maximum dC/dV does not change with increasing interface state densities. The slightly lower dC/dV peak of sample 1-1 can be attributed to additional surface passivation by the colloidal silica suspension. The FWHM of the dC/dV–V_{tip} curves spreads dramatically with increasing interface state density; i.e. for samples 1-1 to 1-5 the FWHM values are 2.1, 2.2, 4.2, 4.7, and 4.7 V, respectively. Moreover, the flatband voltage shifts to the negative of the V_{tip} axis with increasing interface state density, indicating positive interface charges.

Fig. 2 shows the dC/dV–V_{tip} data of samples 2-1 and 2-2 measured with different amplitudes of V_{ac} at 20 kHz (0.1, 0.5, and 1 V). In conventional high frequency MOS

[1] Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment used are necessarily the best available for the purpose.

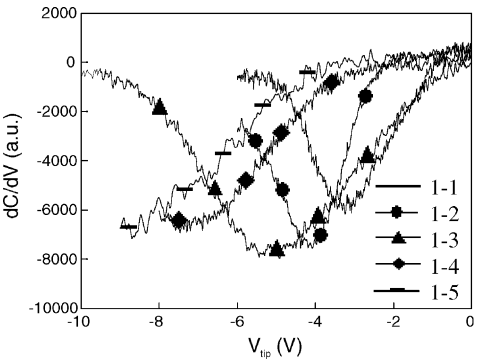

Fig. 1. SCM dC/dV–V_{tip} data measured for five samples (1-1 to 1-5) with different interface state densities, but the same oxide thickness (∼2 nm).

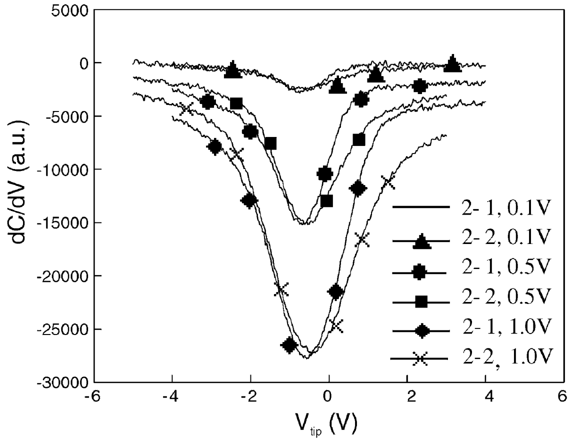

Fig. 2. SCM dC/dV–V_{tip} data measured from two samples (2-1 and 2-2) with different interface state densities and an identical oxide thickness (∼4 nm) at different V_{ac} amplitudes.

C–V measurements, interface states are usually able to respond to ac voltage frequencies up to around 1 MHz [14]. If the interface states react to the 20 kHz V_{ac} signal in this SCM C–V measurement, they should give some capacitive contribution to the total MOS capacitance. As a result, the total capacitance and the maximum slope of the C–V curve (maximum dC/dV) should slightly increase [19]. However, Fig. 2 shows that the maximum dC/dV values of the two samples, which have an identical oxide thickness, are nearly the same for all three V_{ac} values in the SCM measurement. This indicates no apparent interface states response to V_{ac}. At the same time, the FWHM value of sample 2-2, which has the higher interface states density, is bigger than that of sample 2-1, indicating the interface states respond to V_{dc}.

Fig. 3 shows the dC/dV–V_{tip} curves obtained in the n- and p$^+$-regions of samples 3-1 and 3-2, normalized

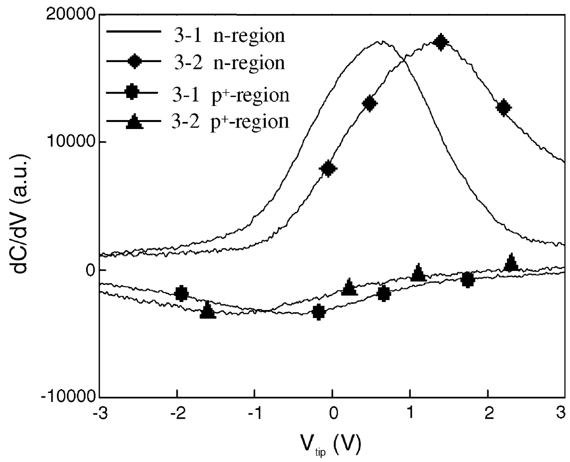

Fig. 3. Normalized SCM dC/dV–V_{tip} data measured from two identical p–n junction samples (3-1 and 3-2) with different interface state densities.

to their peak dC/dV values. In Fig. 3, the flatband voltages measured in the n- and p$^+$-regions of sample 3-2, which has the higher interface states density, shift in the opposite direction along the V_{tip} axis in comparison with those of sample 3-1. That is, the flatband voltage in the n-region shifts to the positive and, the voltage in the p$^+$-region shifts to the negative. This suggests that the interface states in these SCM sample have an amphoteric energy distribution; i.e., donor interface states in the lower part of the band gap and acceptors in the upper band gap.

In summary, our measurement results demonstrate that interface states have no response to V_{ac} in the SCM measurement. This is attributed to two experimental facts: (1) The voltage transition from the accumulation to inversion condition in the SCM dC/dV–V_{dc} curves (∼4 V) is wider than that in the conventional high frequency MOS C–V curves (∼2.5 V) [9]. This is due to the sharp 3-D geometry of the tip, which is similar to the narrow gate-width effects on the threshold voltage of MOSFETs [20]. As a result, the small amplitude V_{ac} (less than 1 V) used in our experiment does not disturb the surface potential too much, resulting in only a slight change of the interface trapped charges. (2) The interface state density near midgap is small due to the amphoteric energy distribution of the interface states. Thus, the interface-trapped charge density in a weak depletion condition is small compared to other types of interface charges, such as fixed charges and mobile charges. The amount of interface-trapped charge will not appreciably change with V_{ac}, and the interface states can be regarded as only responding to V_{dc}. This means, at a given V_{dc}, the interface states behave in the same way as fixed charges. Due to this behavior of interface states in SCM measurements, the FWHM of

dC/dV–V_{dc} curves spreads along the V_{tip} axis because of the shift of the local C–V curves caused by the interface charges and, at the same time, the magnitude of the maximum dC/dV is independent of the interface states. These experimental results validated our earlier simulation work for the interface states model of SCM measurements [7], and this simple behavior of interface states in SCM measurements could make the dopant profile extraction significantly easier than expected. Characterization of interface states with SCM is still qualitative at this stage. The quantitative application of SCM as an interface states characterization tool will rely on calibrating the fringing field of the 3-D SCM tip in both the simulation and the experiment.

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