Automating Thermo-Mechanical Warpage Estimation of PCBs/PCAs using a Design-Analysis Integration Framework

Authors:
Manas Bajaj (Georgia Tech), Russell Peak (Georgia Tech), Dirk Zwemer (AkroMetrix),
Thomas Thurman (Rockwell Collins), Lothar Klein (LKSoft),
Giedrius Liutkus (LKSoft), Kevin Brady (NIST), John Messina (NIST), Mike Dickerson (InterCAX)

http://eislab.gatech.edu/pubs/conferences/2006-user2user-bajaj/

Abstract

Accurate prediction, validation and reduction of thermally-induced PCB warpage are critical for enhancing manufacturing yield and reliability in time-to-market driven electronics product realization.

In this paper, we describe a methodology to simulate thermally-induced warpage of PCBs and PCAs. We will demonstrate this analysis methodology using the following path: read ECAD designs from *Mentor Board Station*, identify features relevant to warpage analysis, create idealized analysis models, select solution technique and create solver-specific models (e.g. ANSYS models for finite-element solution), identify warpage-hotspots and calculate metrics to assist PCB/A designers in reducing warpage. We shall also present initial results from experimental verification of this technique using Shadow Moiré (TherMoiré®) method.

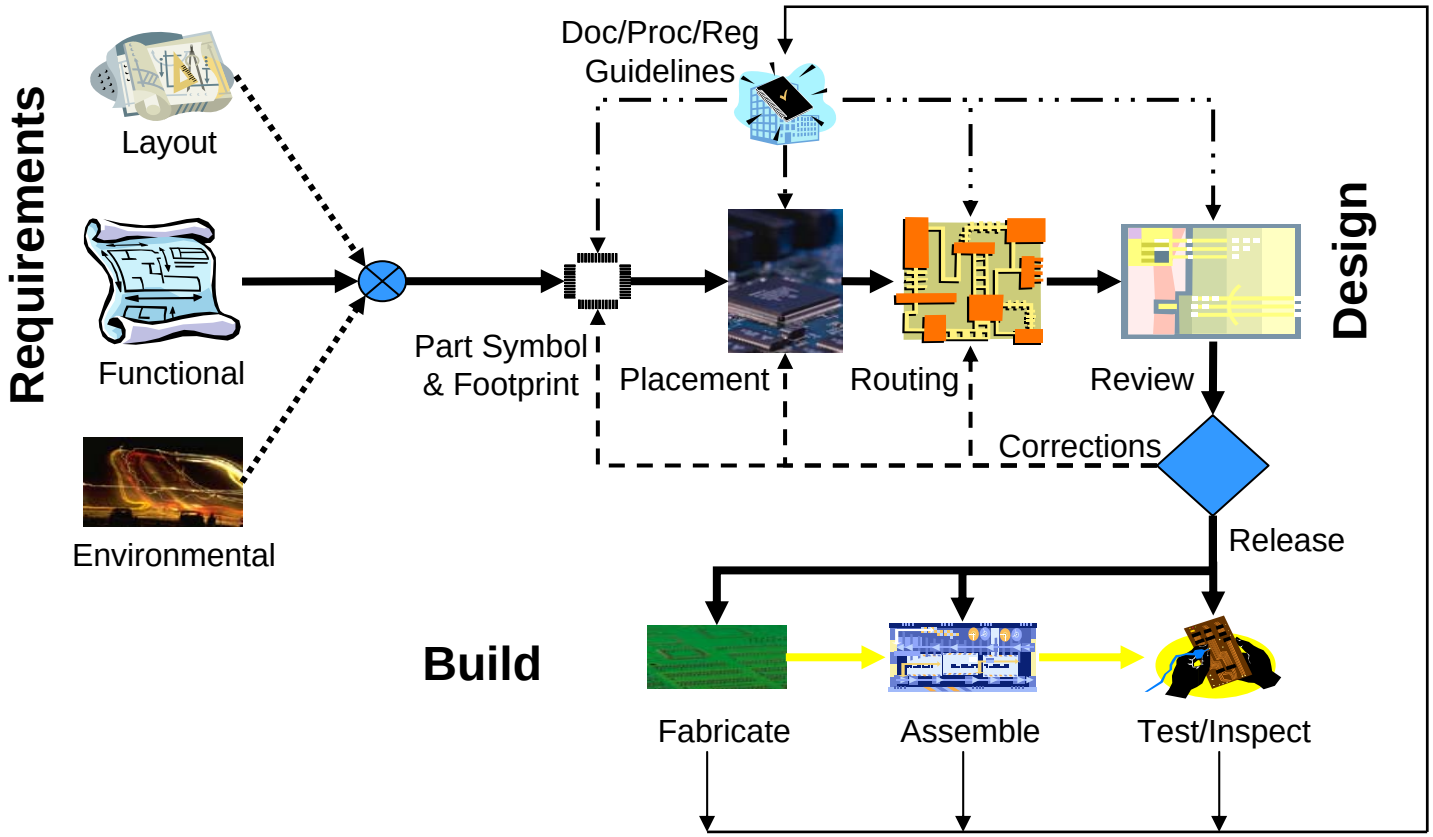
This methodology reuses analysis concepts, idealizations, and solution techniques for modularized and configurable simulation studies. It uses ISO 10303 technologies (STEP AP210 – www.ap210.org and Standard Data Access Interface - see www.jsdai.net).

Project page: http://eislab.gatech.edu/projects/nist-warpage/

Contents

- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results
- Methodology
  - MRA-based Design Analysis Integration Framework
- Conclusion

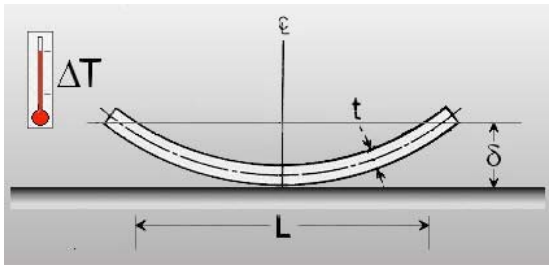
Electronics Product Realization



Learn today
Utilize tomorrow

Warpage - *Definition*

- **WARPAGE is out of plane deformation of the artifact, caused by differential (non-homogenous) shrinkage or expansion of elements composing the artifact.**



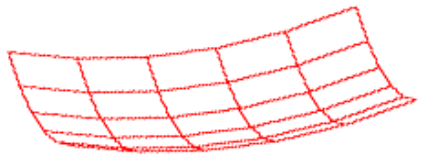
Out of plane deformation of a linear element

$\delta = (\alpha_b L^2 \Delta T) / t$ where

L: Undeformed Length; **t**: Undeformed Thickness; **ΔT**: Temperature Change; α_b: Specific Co-efficient of Thermal Bending

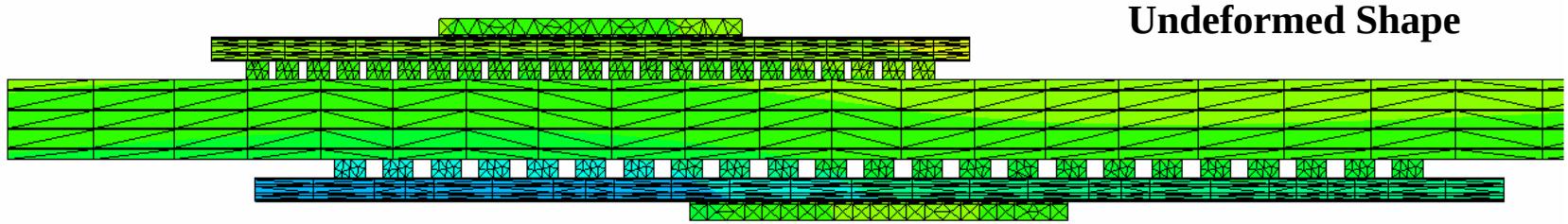
Warpage of 2D artifacts (basic modes)

Saddle Deformation

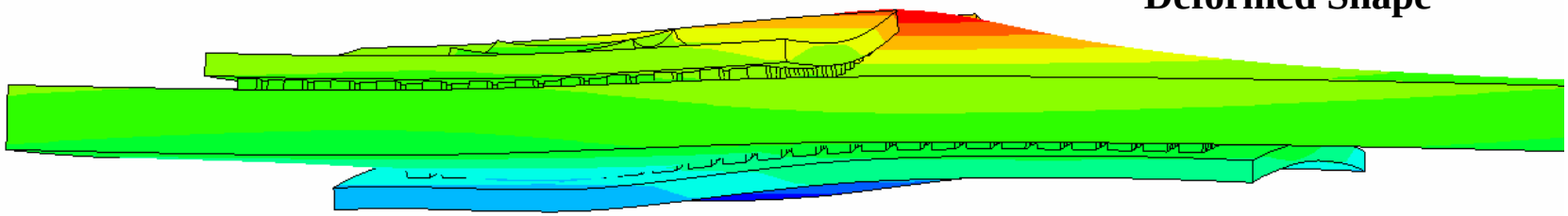


Bowl Deformation

PCA/B Warpage - Illustration



Undeformed Shape



Deformed Shape

Warpage – Factors and Effects

[after Ding, 2003; et al.]

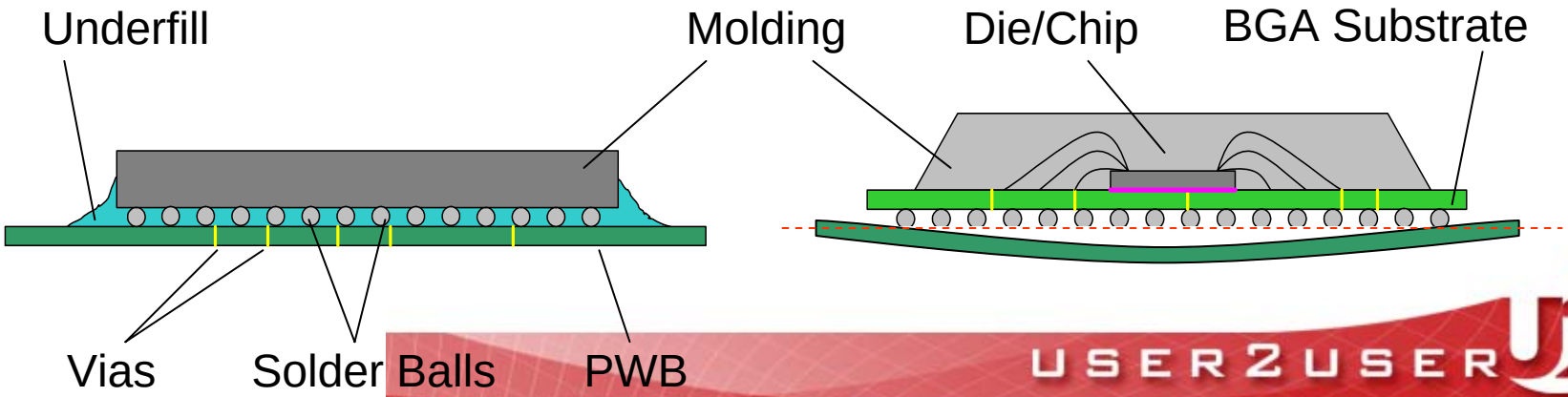
Estimated Impact: $100M / year

Factors:

- **CTE mismatch**
- **Material rigidity**
- **Thermal conductivity**
- **Geometric size & aspect ratio**
- **Component layout**
- **Temperature variation**
- **Temperature gradient**

Consequences:

- **Misregistration**
- **Delamination**
- **Die crack**
- **Solder fatigue**
- **Solder shortening**
- **Solder opening**



Warpage – Impact and Requirements

Ref: Thinking Globally, Measuring Locally
Editorial by Patrick Hassell, AkroMetrix

Impact

- **Low manufacturing yield and high rework of interconnects**
  - **Lack of co-planarity of component footprints**
  - **Fine pitch technology**
  - **Low solder paste volume**

Requirements

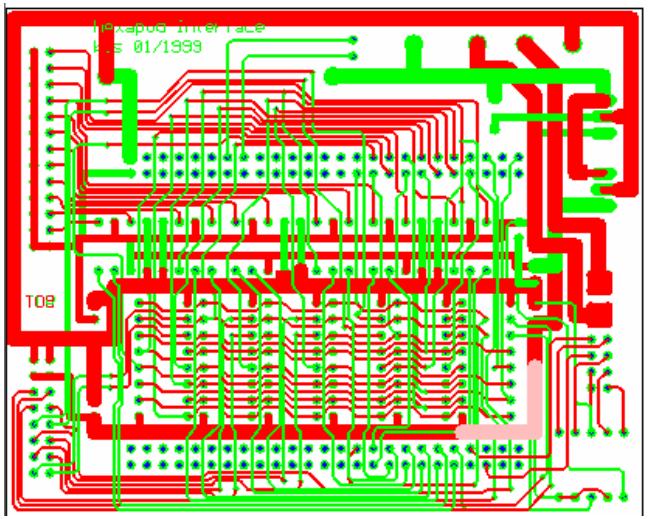
- **Managing warpage requirements**
  - **Enforce local warpage requirements**
  - **Relax global warpage requirements**

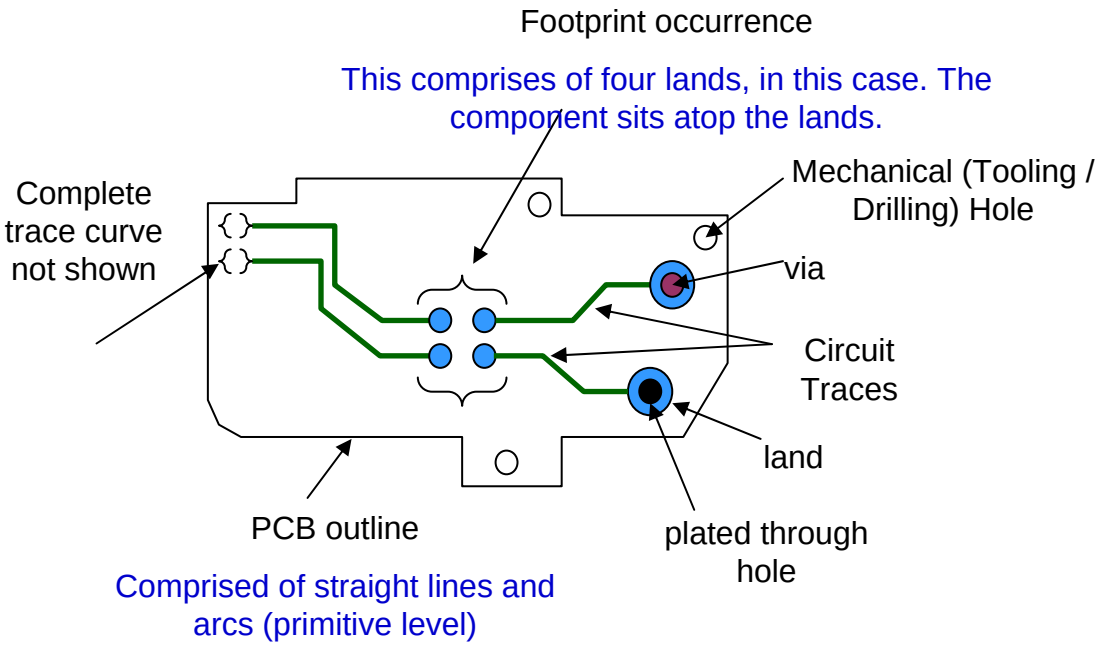
Contents

- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results
- Methodology
  - MRA-based Design Analysis Integration Framework
- Conclusion

Complex Features Affecting Thermo-Mechanical Behavior

PCB level

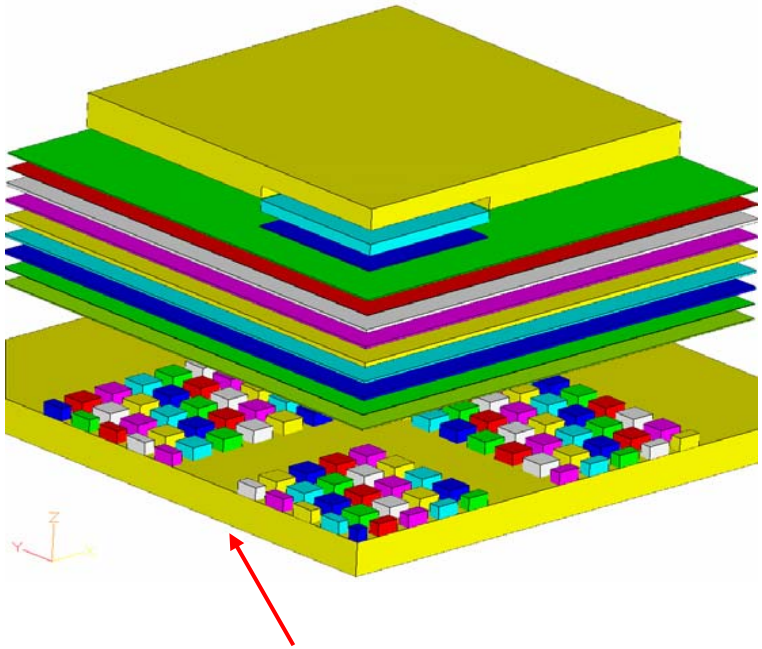




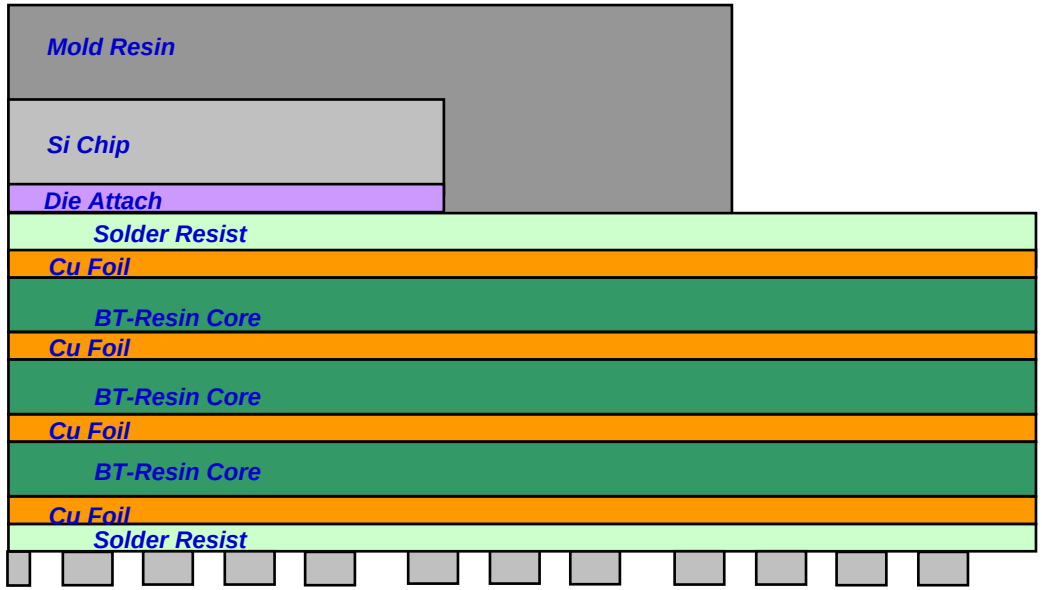
Complex Features Affecting Thermo-Mechanical Behavior

PCA level

Isometric View



Side View



Solder Balls (Diagonal Grid Pattern)

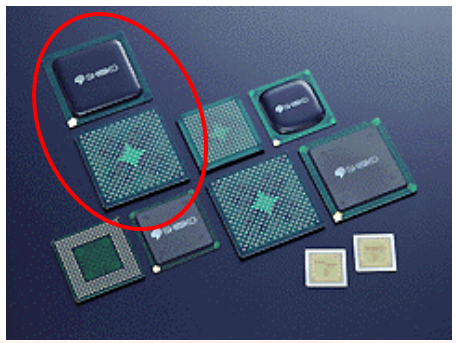


Photo: www.shinko.co.jp

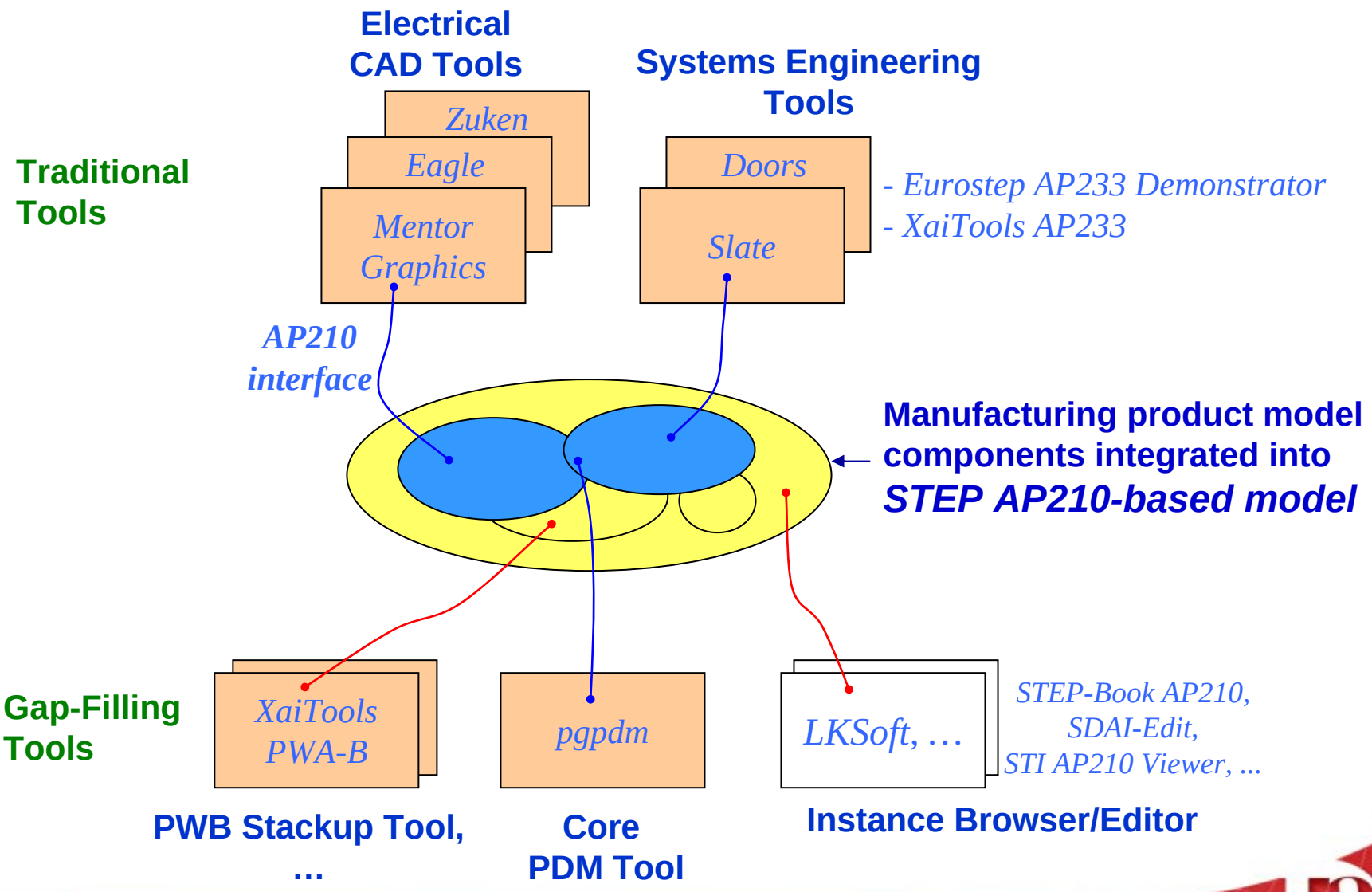
Contents

- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results and Validation
- Methodology and Tools
  - Multi-Representation Architecture
  - Beta-level PWB warpage estimation tool
  - Prototype-level PWAB warpage estimation tool
- Conclusion

Requirements for Warpage Analysis

- **Availability of a rich product model**
  - **ECAD design details**
  - **PCB layer stackup details**
  - **Material behavior and properties**
- **Analysis model creation capabilities**
  - **Idealized PCB/A features**
  - **Boundary conditions**
  - **Thermal loading**
- **FEA Model creation and solution capabilities**
  - **FE mesher**
  - **FE solver**

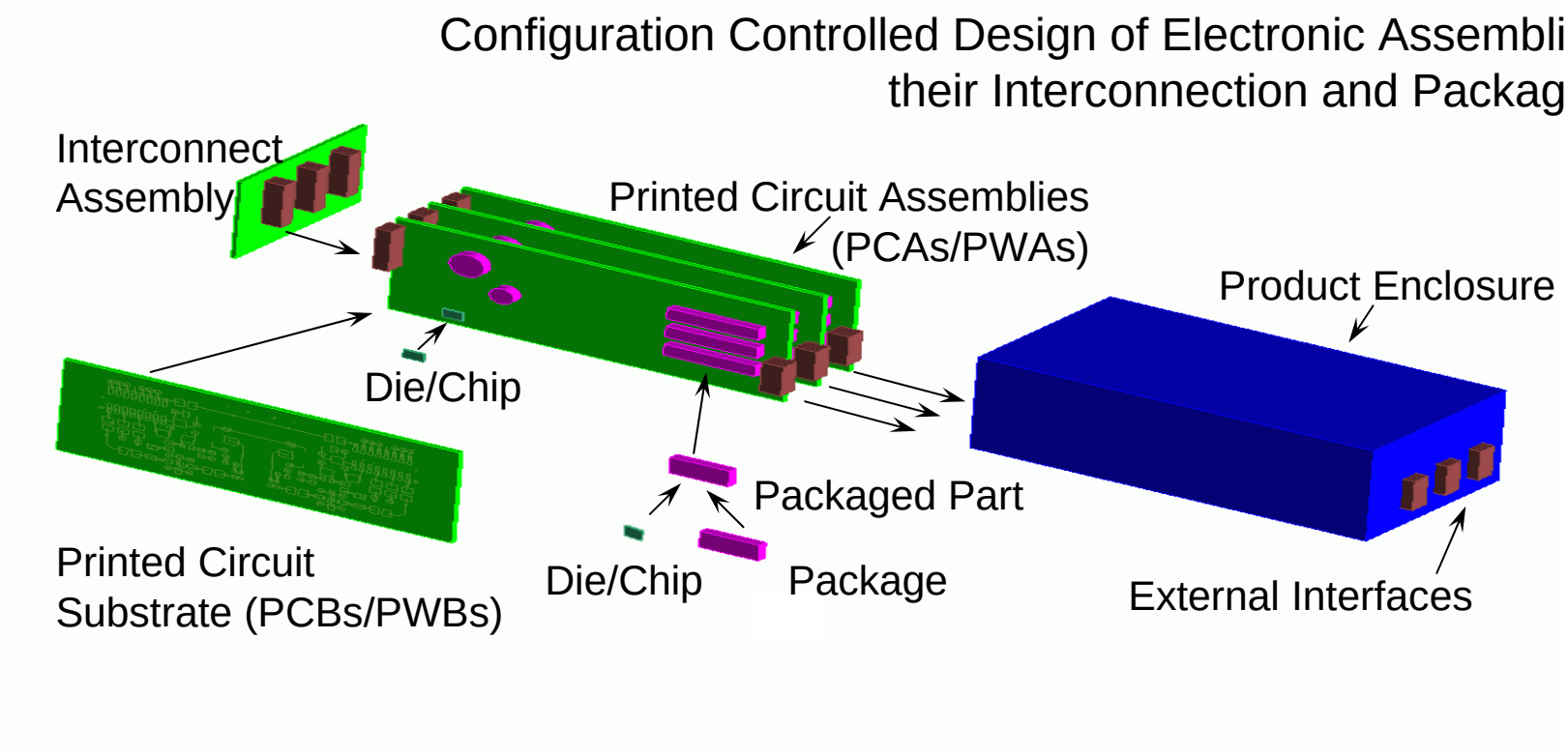
Rich Product Model



STEP AP210 (ISO 10303-210)
Domain: Electronics Design

PDES, Inc.®

~950 standardized concepts (many applicable to other domains)
Development investment: O(100 man-years) over ~10 years



STEP AP210 (ISO 10303-210)

Scope

http://www.ap210.org

Functional Models

- Functional Unit
- Interface Declaration
- Network Listing
- Simulation Models
- Signals
- Test Bench

Requirements Models

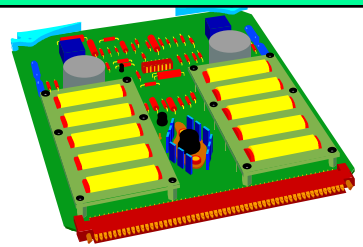
- Design
- Constraints
- Interface
- Allocation

Component / Part Models

- Analysis Support
- Package
- Material Product
- Properties
- “White Box”/ “Black Box”
- Test Bench

Rules Models

- Design
- Manufacturing
- …



Assembly Models

- User View
- Design View
- Component Placement
- Material product
- Complex Assemblies with Multiple Interconnect

Interconnect Models

- User View
- Design View
- Bare Board Design
- Layout templates
- Layers

Design Control

- Geometric Dimensioning and Tolerancing

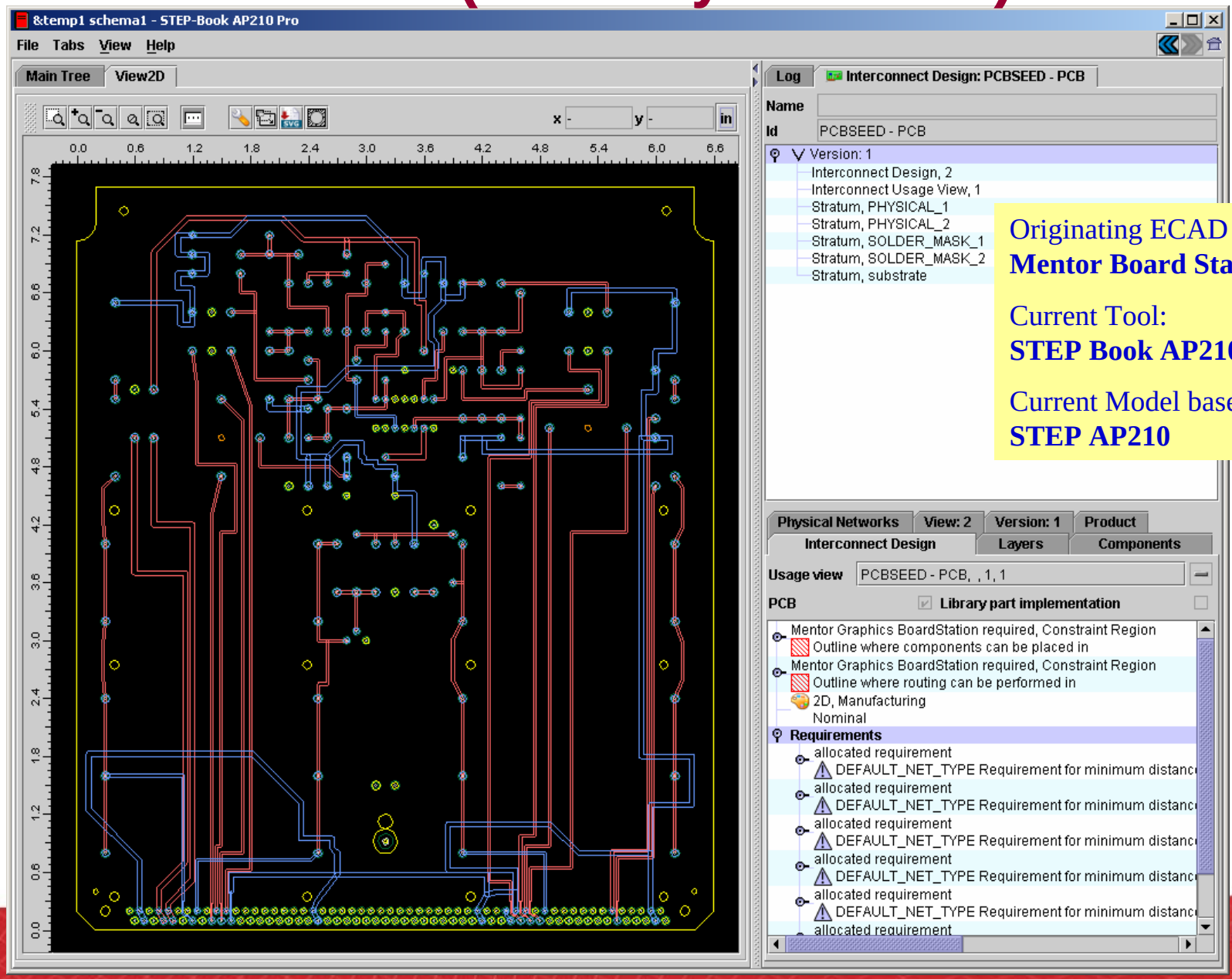
Configuration Mgmt

- Identification
- Authority
- Effectivity
- Control
- Net Change

Geometric Models

- 2D
- 3D
- CSG, Brep…
- EDIF, IPC, GDSII compatible “trace” model

Example Design in STEP Book AP210 Pro (PCB Layout View)

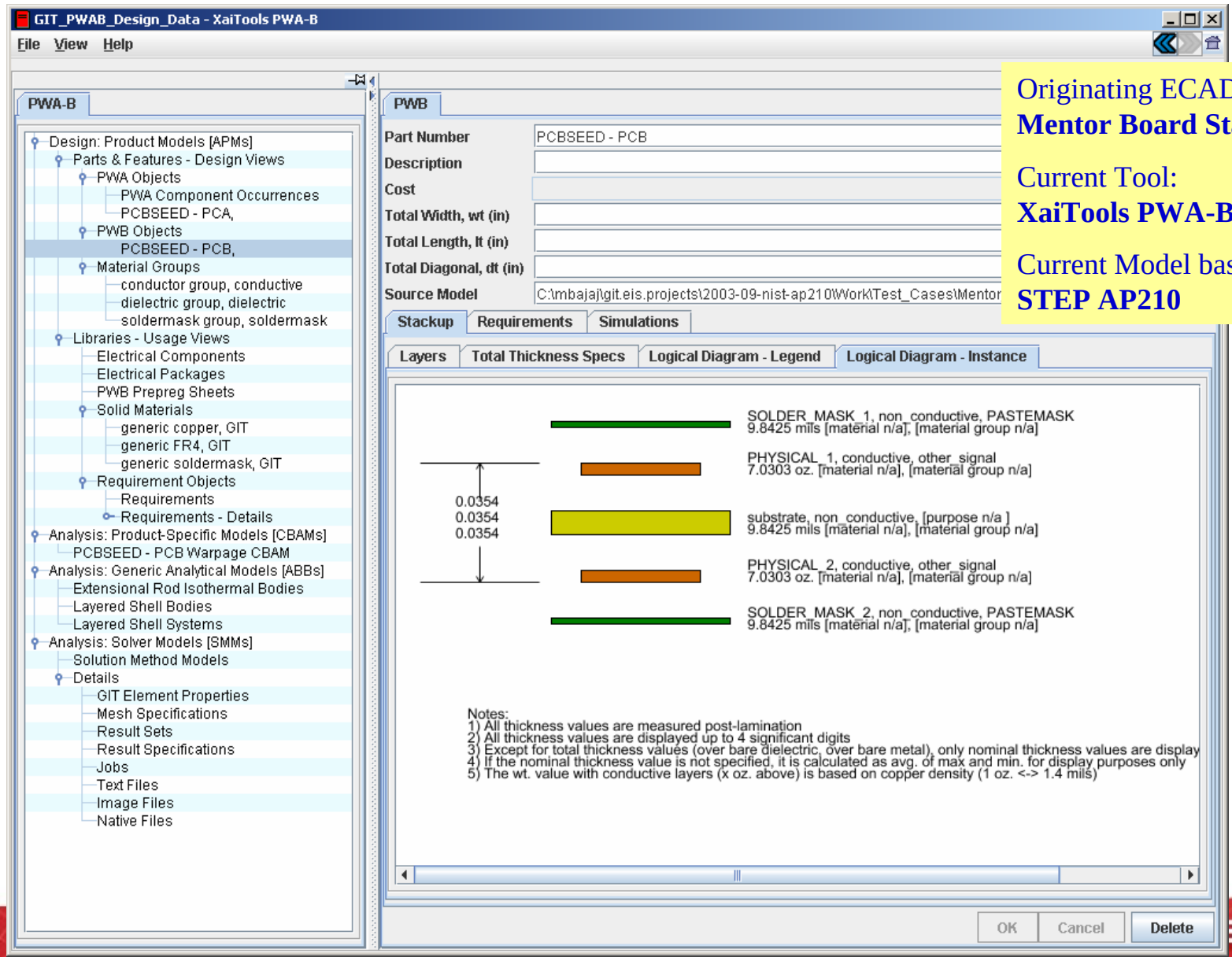


Originating ECAD Model from:
Mentor Board Station

Current Tool:
STEP Book AP210 v2.3

Current Model based on:
STEP AP210

Example Design in XaiTools PWA-B 2.0.b1 Stackup Editor



Originating ECAD from:
Mentor Board Station

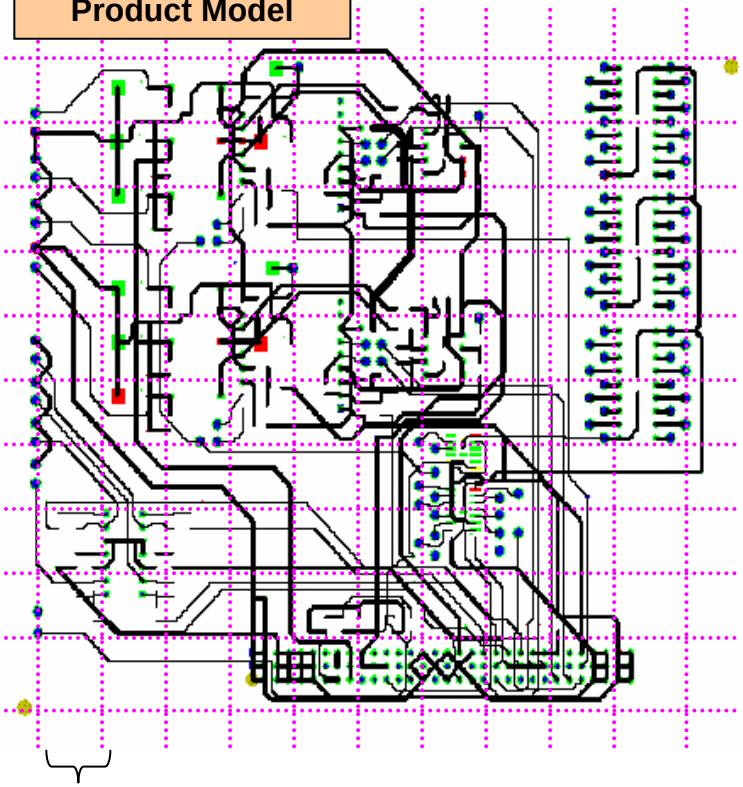
Current Tool:
XaiTools PWA-B v2.0.b1

Current Model based on:
STEP AP210

PCB Warpage Analysis Model Creation

AP210-based Manufacturing Product Model

Single Layer View



Grid (Sieve) Size

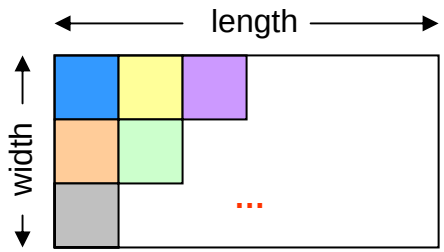
Context

Effective Material Property Computation

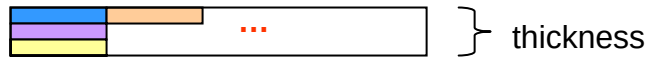
Context Attributes

- Thermal loading profile
- Boundary Conditions (mostly displacement)
- Idealize PWB stackup as a layered shell

Building Block-based Analysis Model



Top view of “effective” grid elements in top layer of the PCB



Side view of the PCB with “effective” grid elements across the stratums

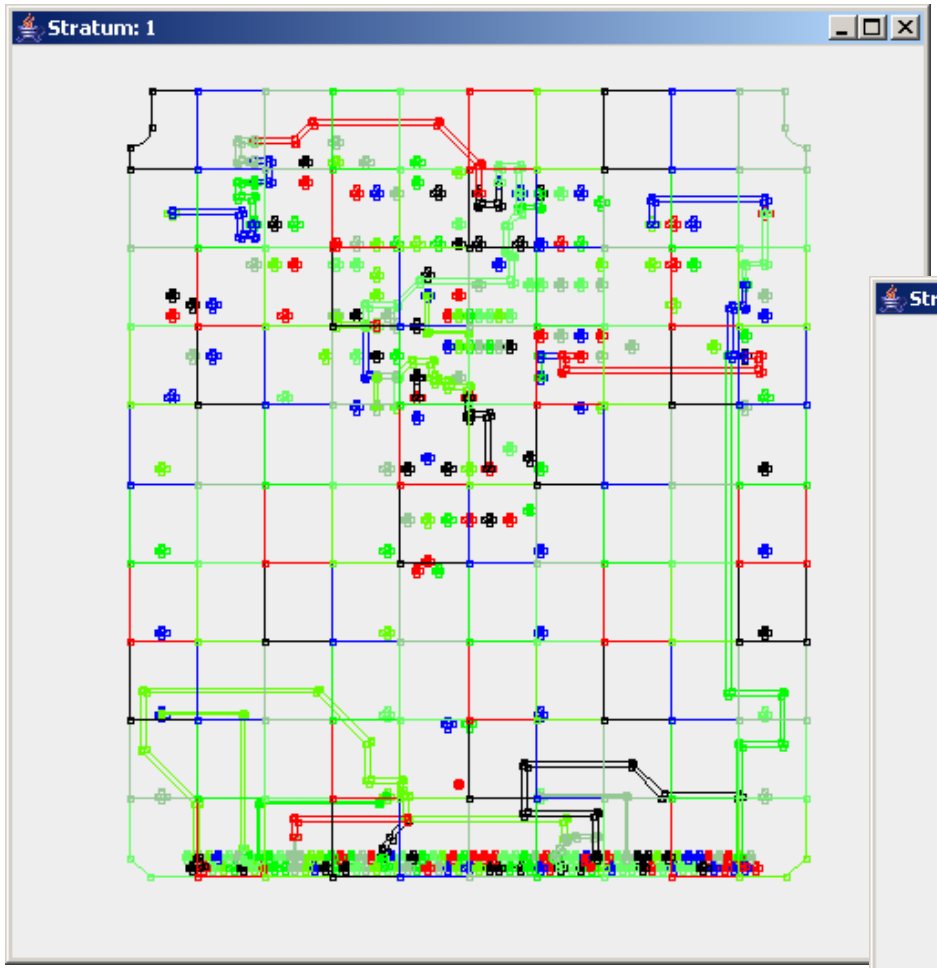
Given:

- Thermal loading profile
- Boundary Conditions (mostly displacement)
- Idealize PWB stackup as a layered shell

Contents

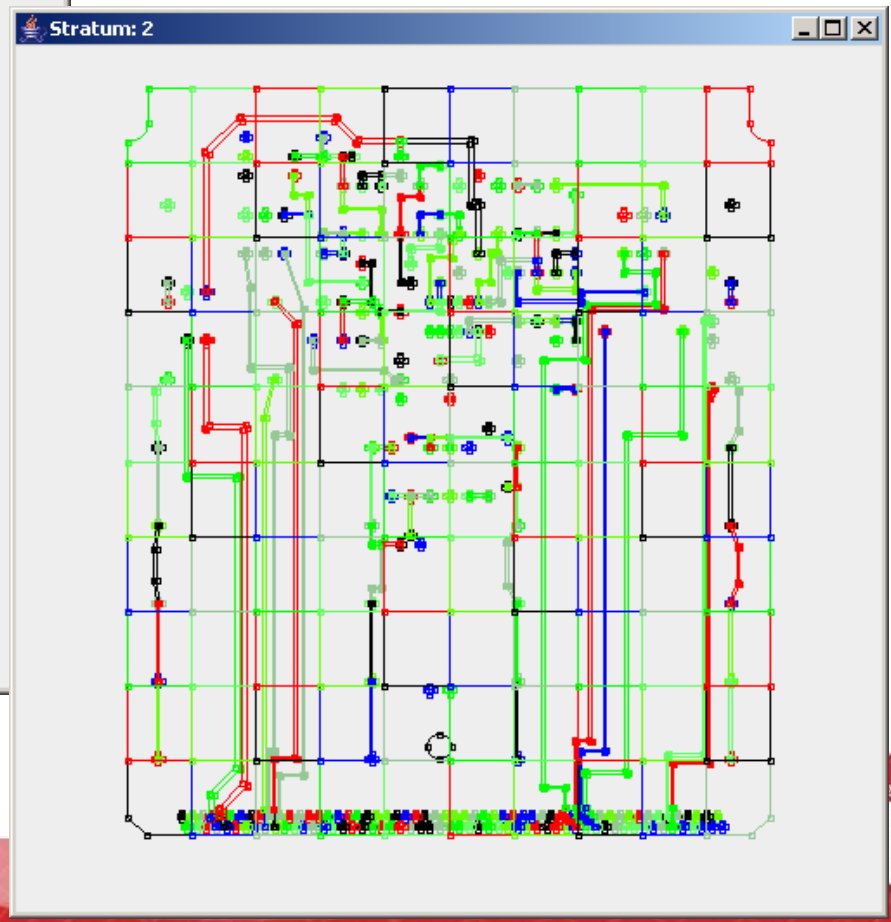
- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results and Validation
- Methodology and Tools
  - Multi-Representation Architecture
  - Beta-level PWB warpage estimation tool
  - Prototype-level PWAB warpage estimation tool
- Conclusion

Chopped PCB Regions for Analysis in XaiTools PWA-B 2.0.b1

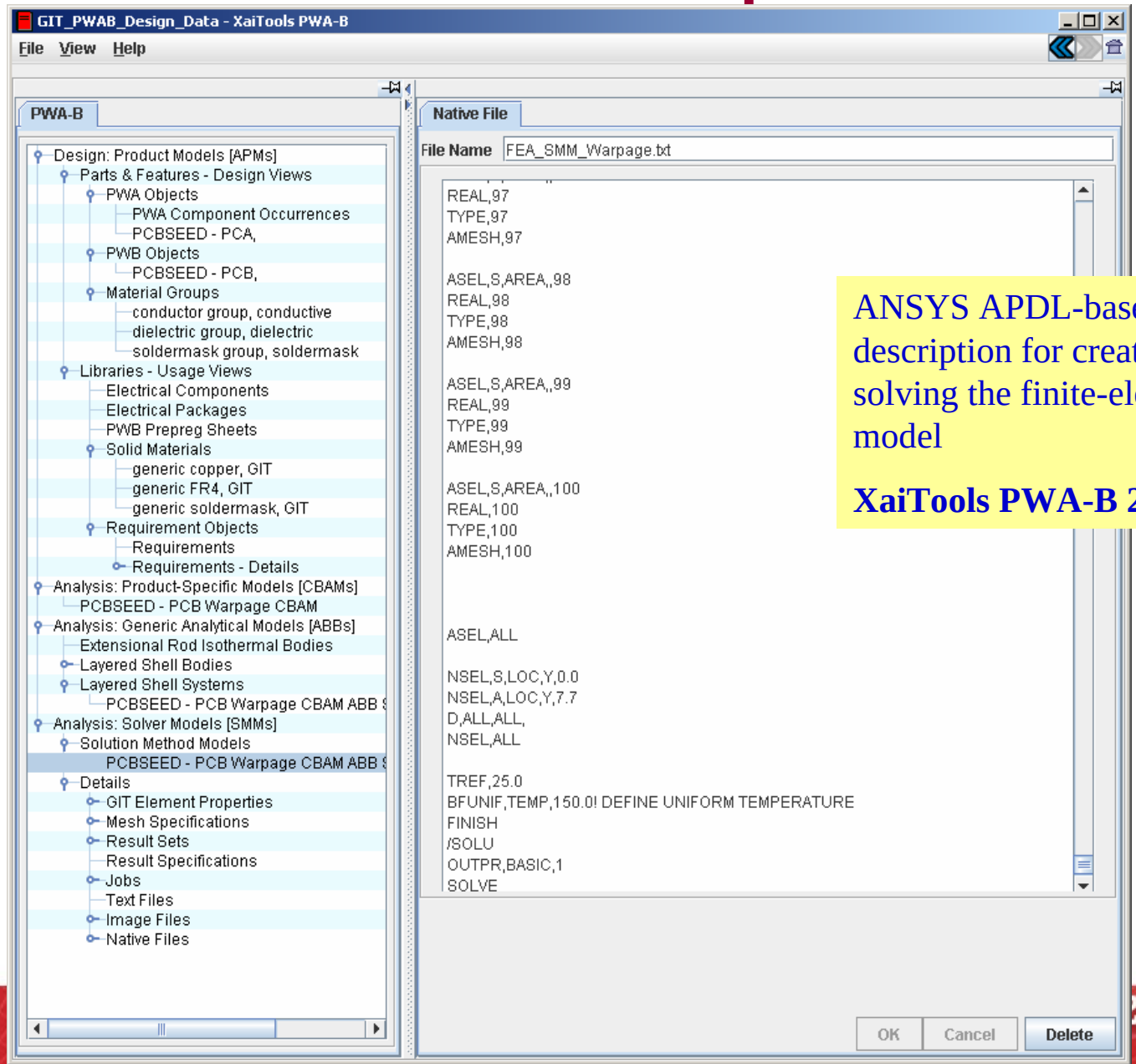


First (Top) Design Layer

Second (Bottom) Design Layer



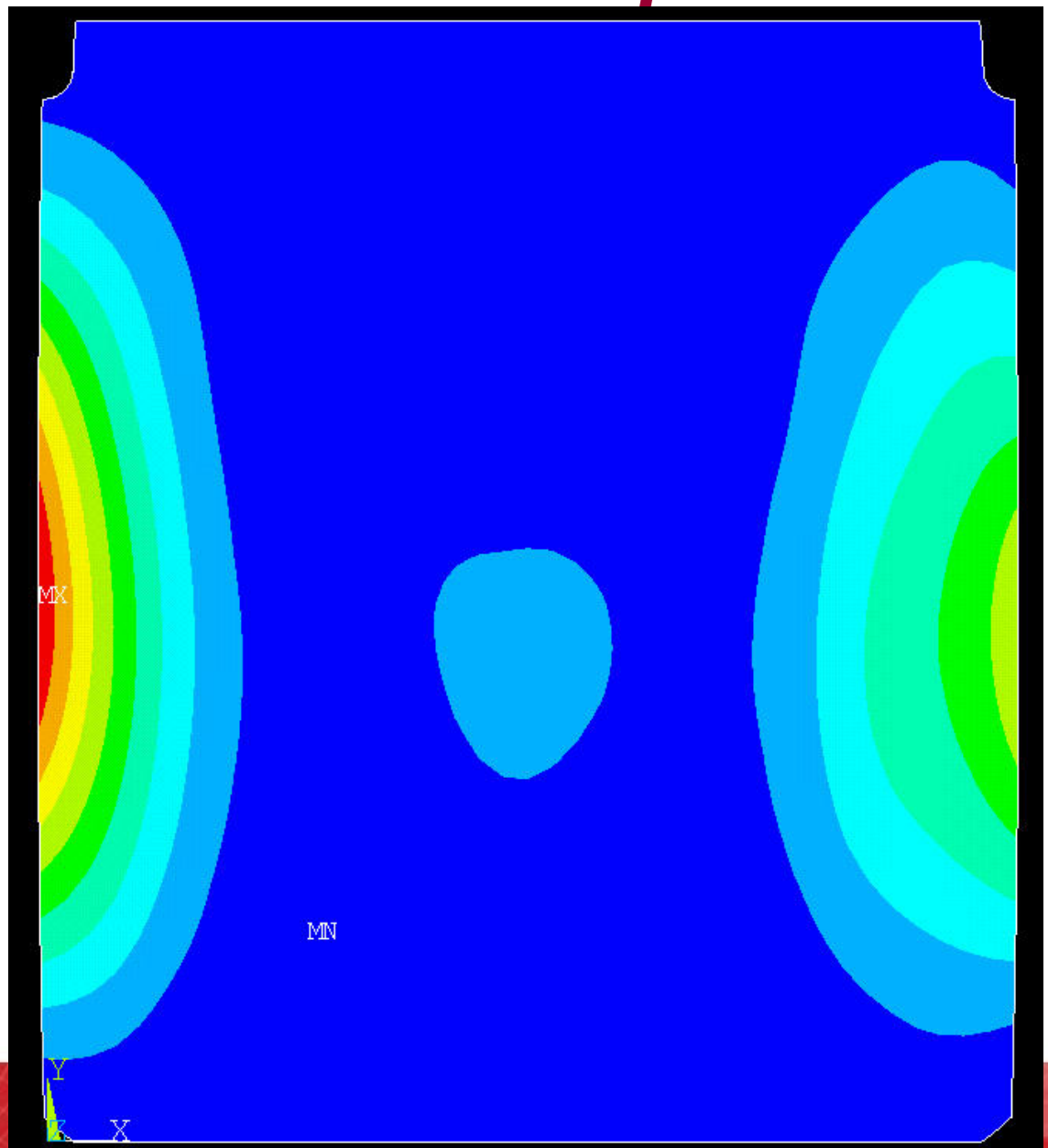
Example Design - Finite-Element Model Creation and Solution Input to ANSYS



ANSYS APDL-based description for creating and solving the finite-element model

XaiTools PWA-B 2.0.b1

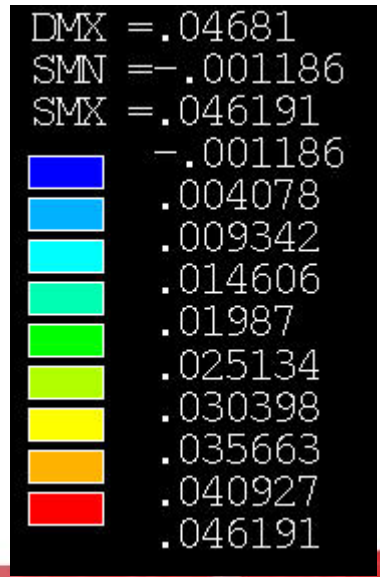
Example Design
Out-of-plane deformation



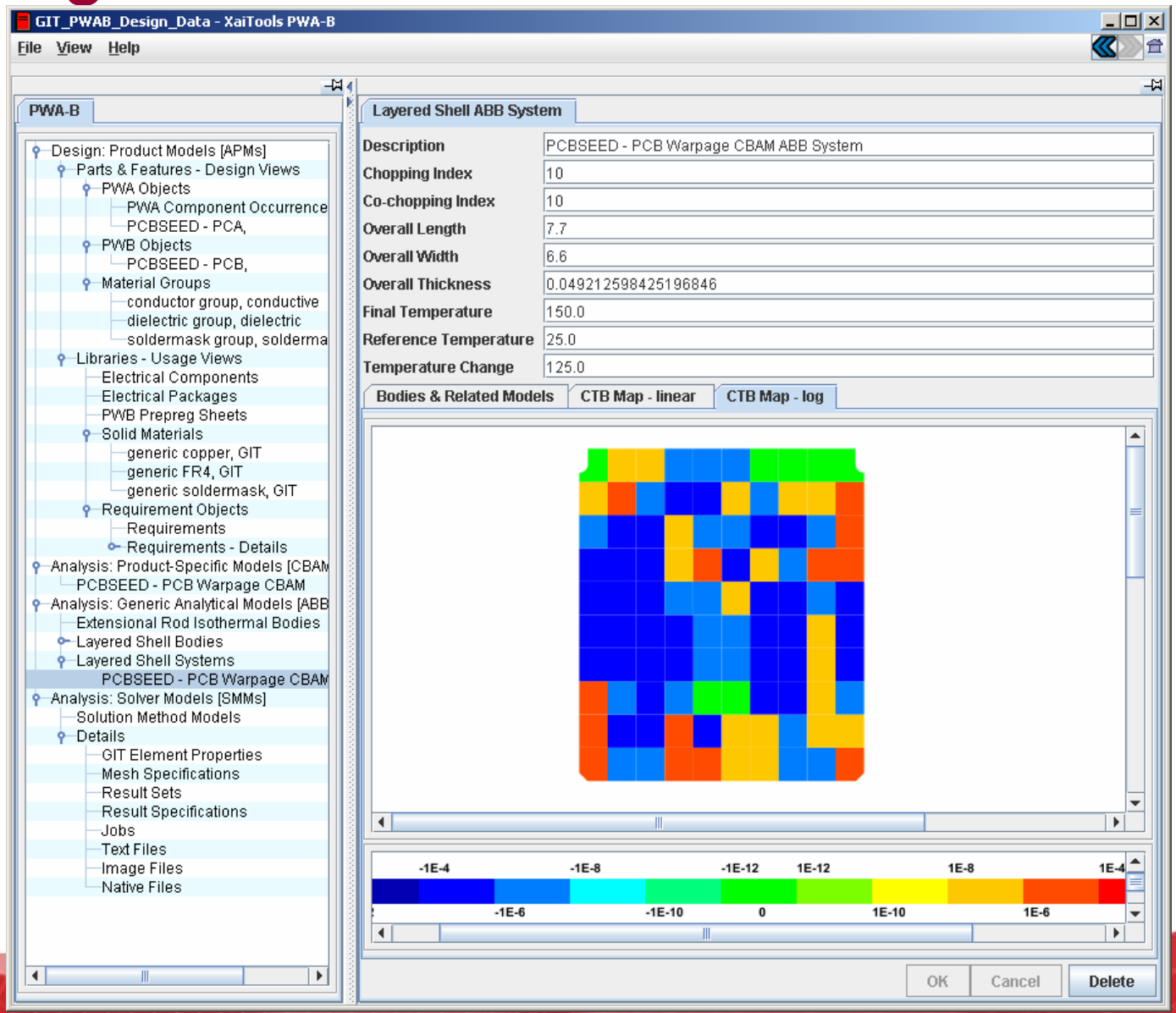
Conditions

ΔT = 125 deg. C - *uniform heating from 25 deg. C to 150 deg. C*

Outermost edges along Y-axis are fully constrained

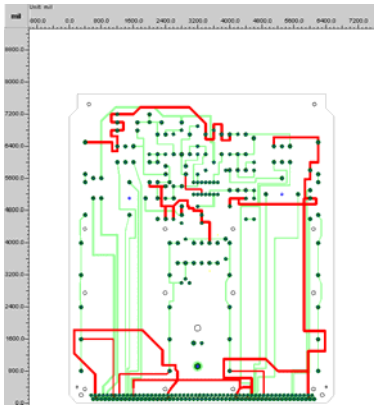


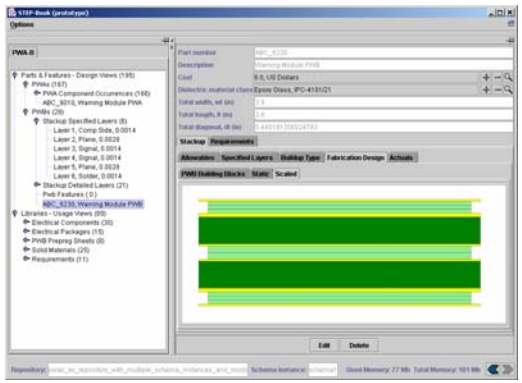
Example Design - Coeff. Of Thermal Bending results in XaiTools PWA-B 2.0.b1



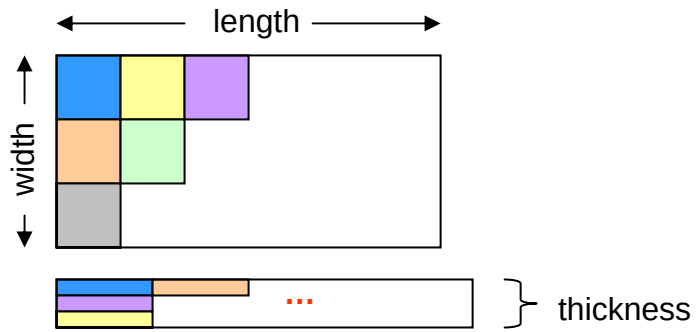
Overall Process - Circuit Board Stackup Design & Warpage Analysis Using AP210 (WIP)

GIT and NIST EEEL in collaboration with AkroMetrix, InterCAX/LKSoft, and Rockwell Collins



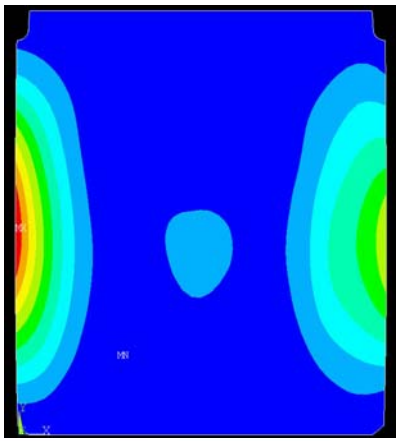


STEP AP210-based
Product Model

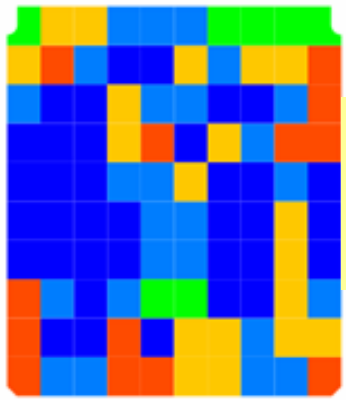


Analysis Building Block Model
(idealized bodies with effective material properties)

Feedback



PCB Warpage Profile
(given: thermal profile + boundary conditions)



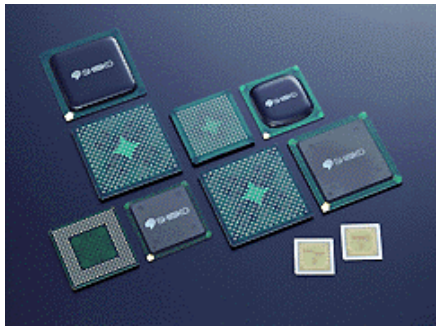
CTB Map

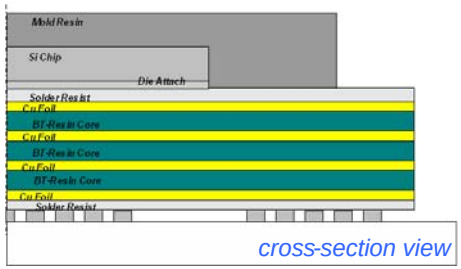
(smeared property to identify material distribution)

http://eislab.gatech.edu/projects/

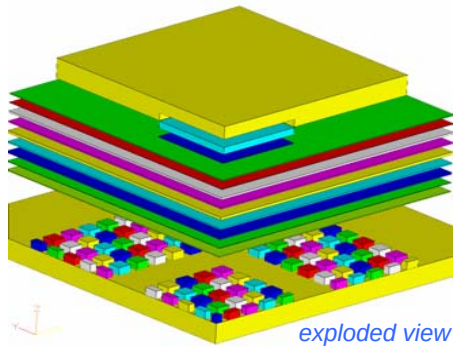
Identification of warpage "hotspots" on a PCB

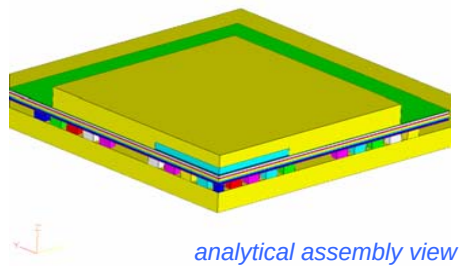
PCA Warpage Analysis Model Creation





cross-section view


exploded view


analytical assembly view

c1. component designs / libraries (e.g., chip packages like plastic ball grid arrays (PBGAs))

Γ_i

c2. Idealized component designs (APMs) and simulation templates (CBAMs)

$_{APM}\Phi_{ABB}$

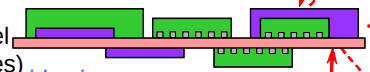
c3. Analytical system models (ABBs) (~400 analytical bodies per component)

Idealized components

$_{APM}\Phi_{ABB}$

d1. Combined analytical system model (~1000+ analytical bodies)

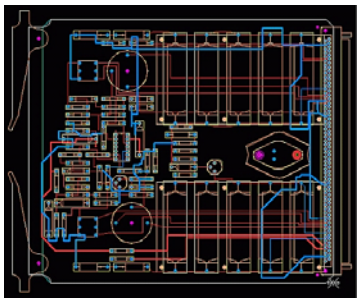
Idealized PCA


side view

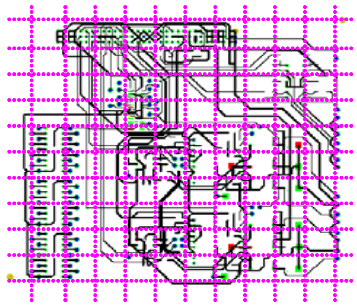
$_{ABB}\Psi_{SMM}$

e1. Combined FEA mesh model (SMM) (~50K elements avg. per complex component)

ECAD layout view



idealization preparation view

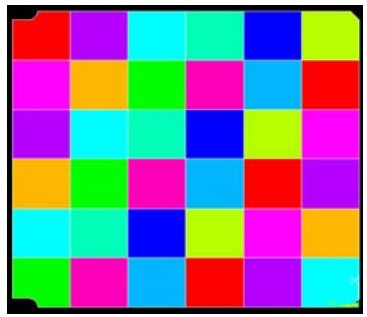


Γ_i

a1. PCA design plus b1. PCB design

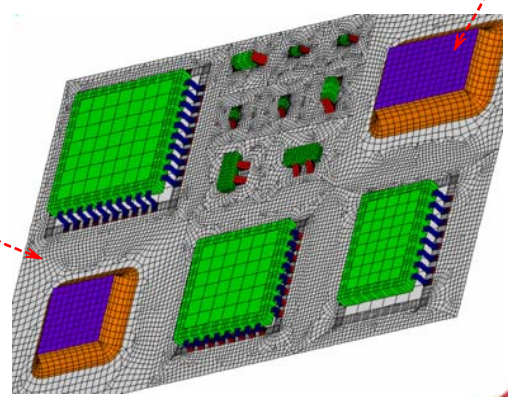
b2. Idealized PCB design (APM) and simulation template (CBAM)

$_{APM}\Phi_{ABB}$



b3. Analytical system model (ABBs) (~50 analytical multilayer shell bodies)

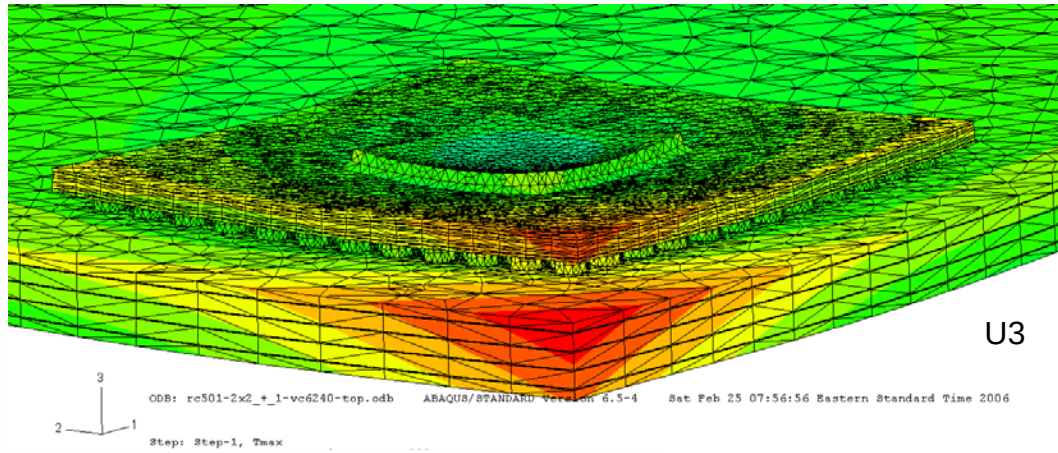
Idealized PCB

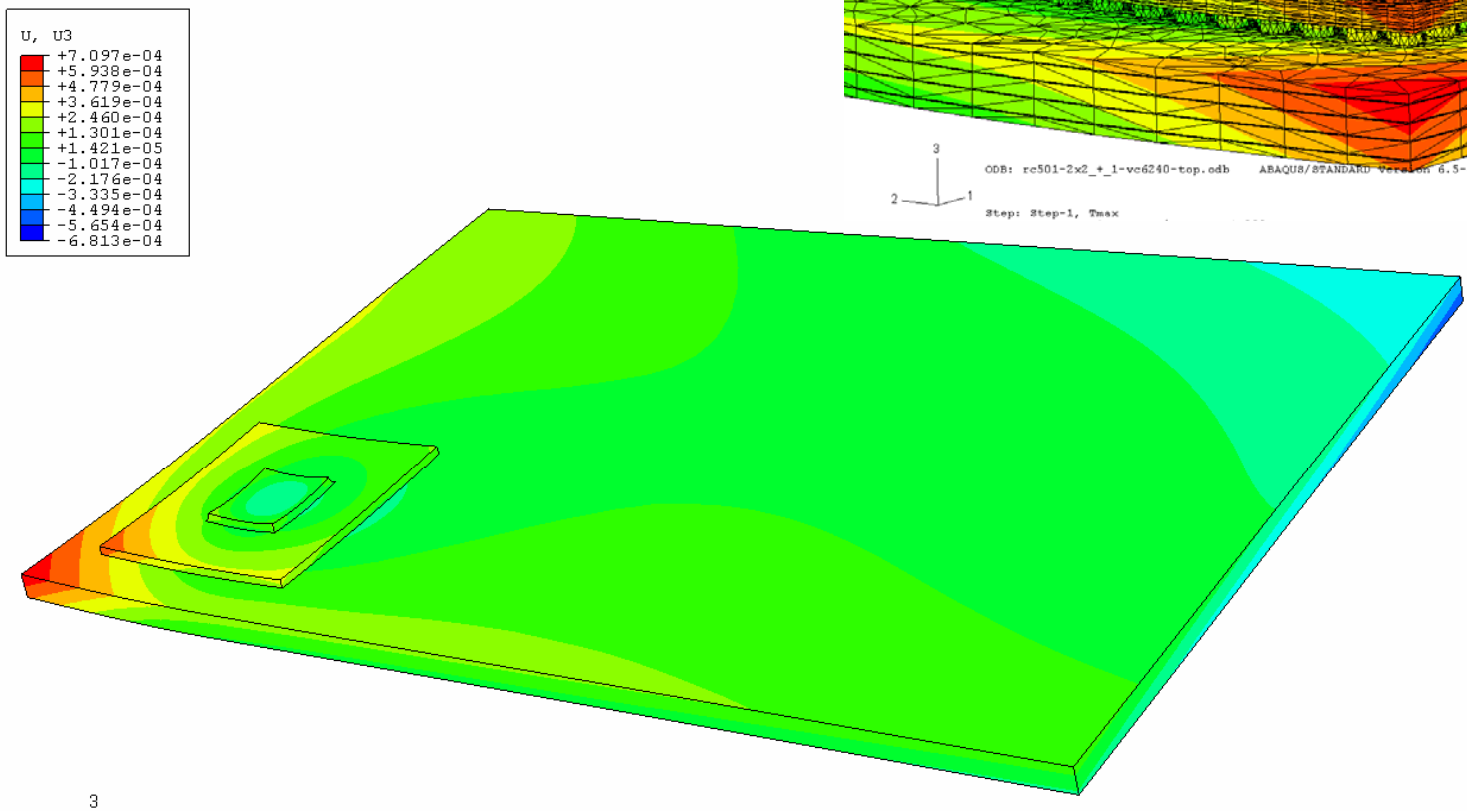


PCB = printed circuit board (bare board) PCA = printed circuit assembly = PCB + components, etc.

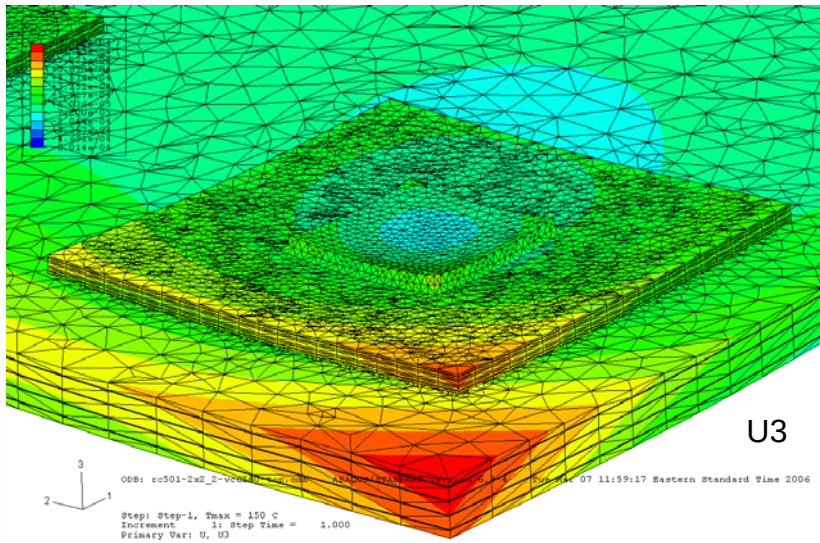
Case 1:
1 PBGA 265 on top

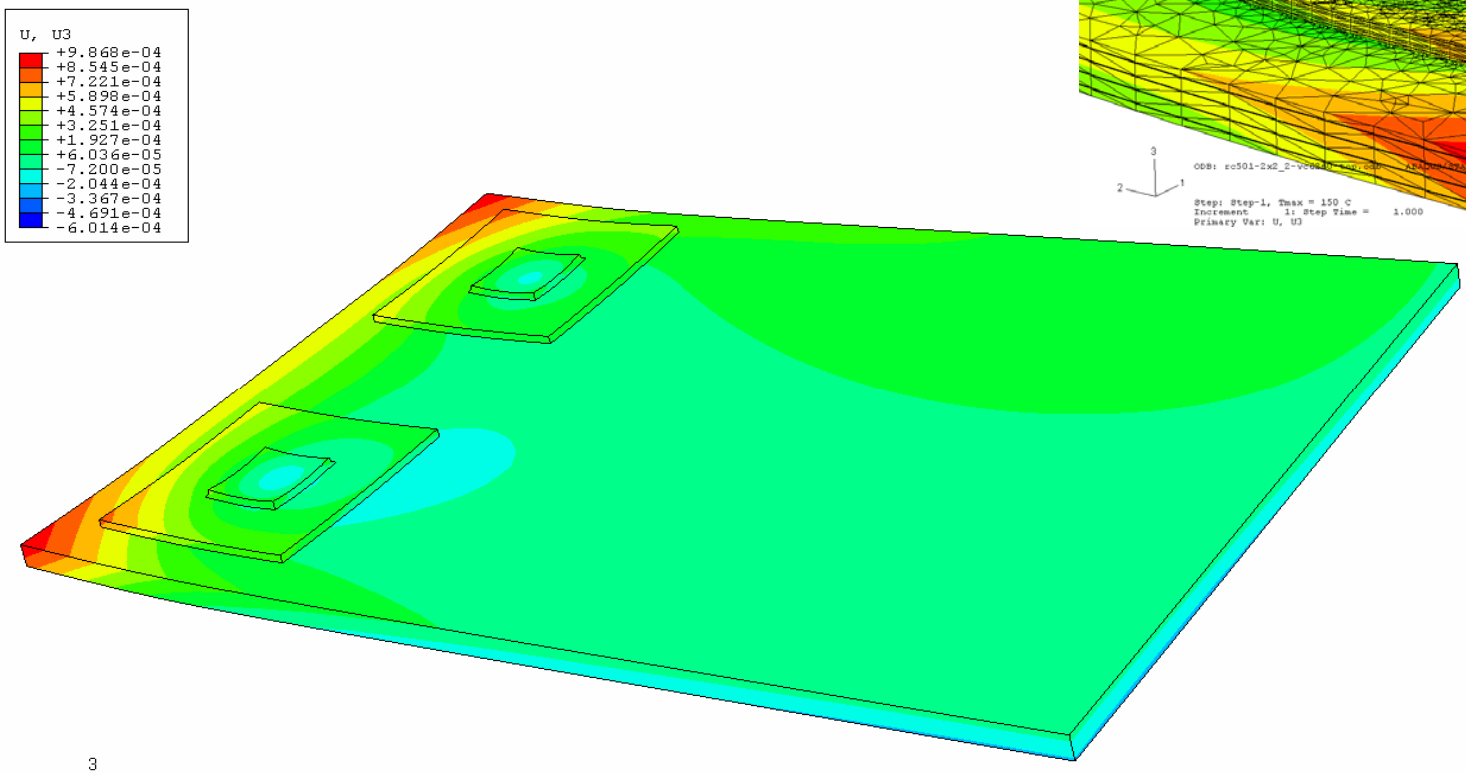
Automated PCA design warpage analysis



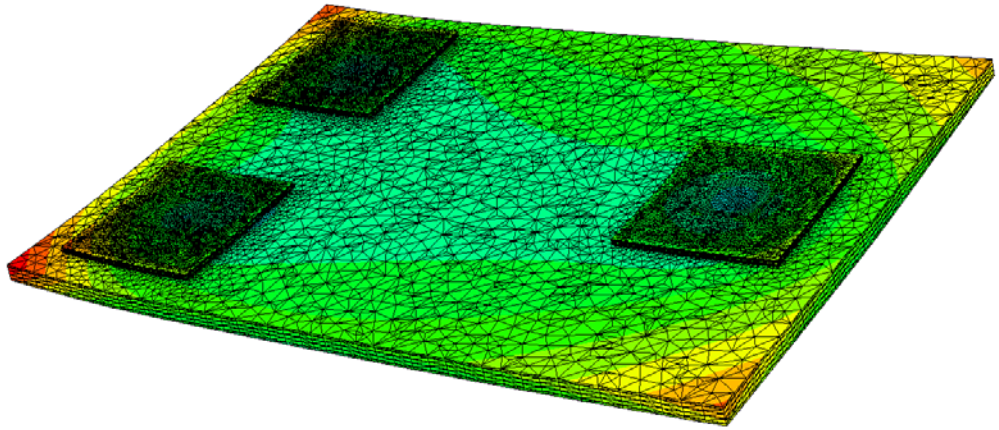


Case 2:
2 PBGA 265s on top





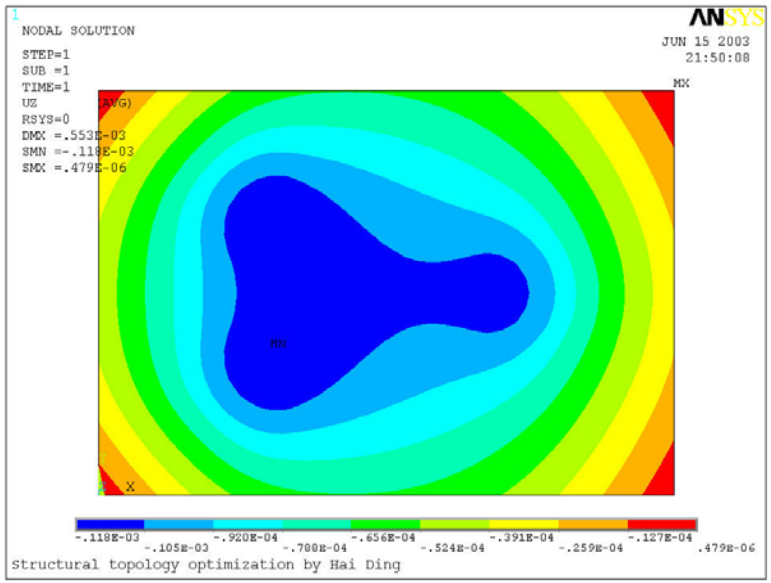
Case 3:
3 PBGA 265s on to

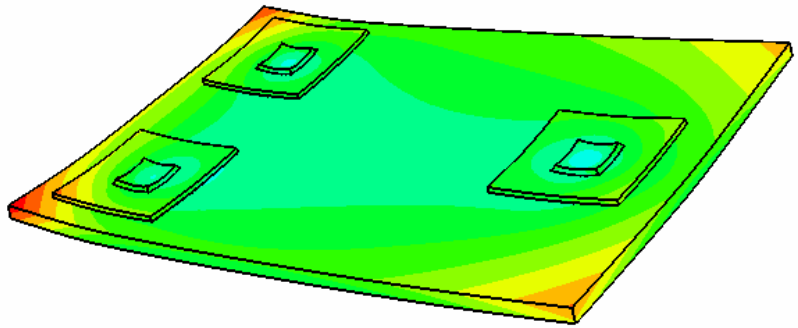


Qualitative comparison

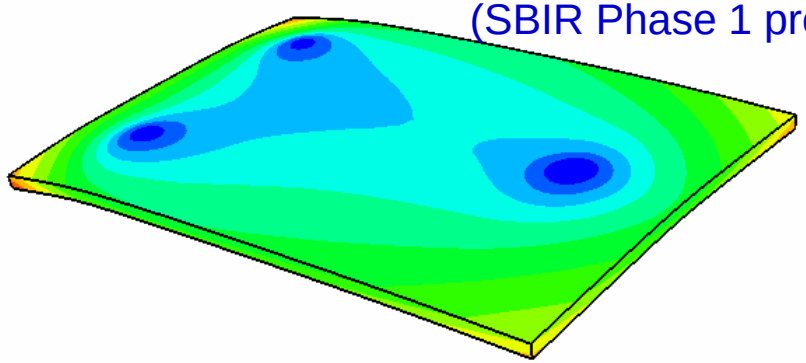
- Different board & components (somewhat similar)
- Good warpage shape results comparison
- Similar total warpage results (2.2 mils vs. 1.7 mils = ~23% delta)

[Ding, 2004] results





InterCAX results
XaiTools Electronics
(SBIR Phase 1 prototype)



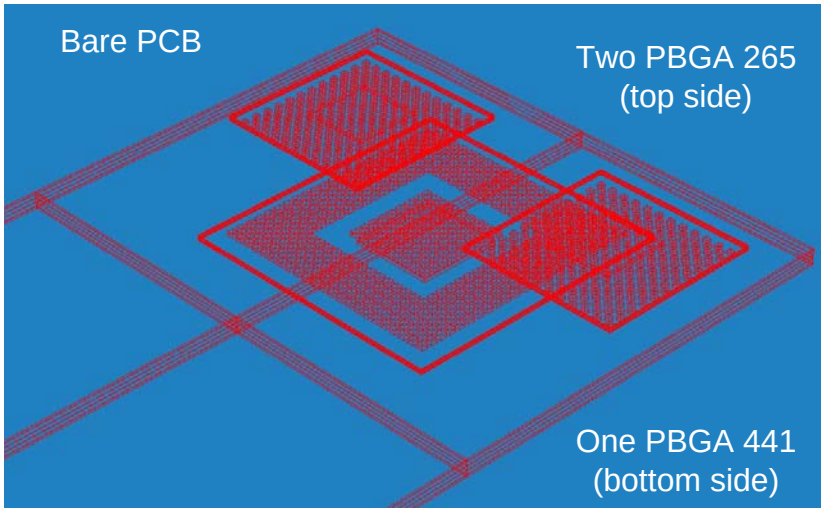
Total Warpage for ΔT=150°C: = 0.0022 in
[scaled from 0.07 mm @ ΔT=183°C]

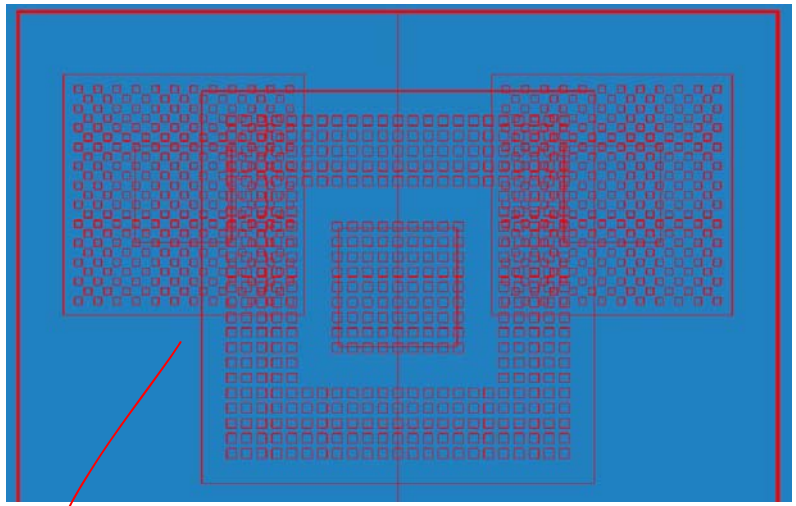
Total Warpage for ΔT=150°C: 0.0017 in

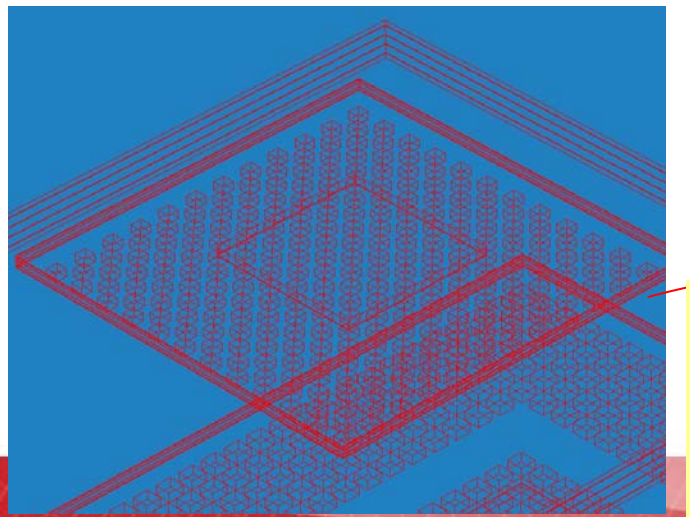
Case 4: PCA with top & bottom PBGAs

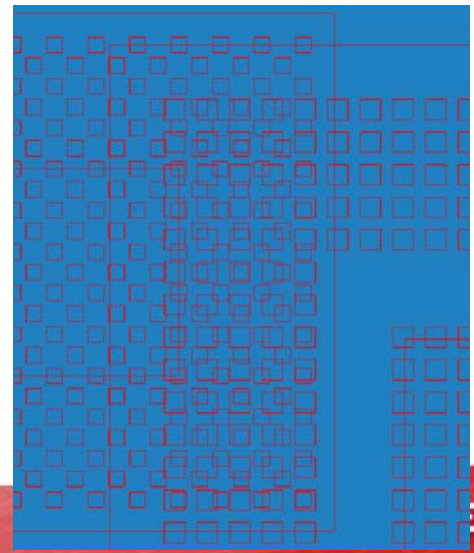
Analytical model in IDA-STEP as imported from AP203

Produced by idealizing AP210-based PCB design (from Zuken Visula ECAD tool)
and combining with idealized chip package models in *XaiTools Electronics* prototype (XE), and exporting as AP203





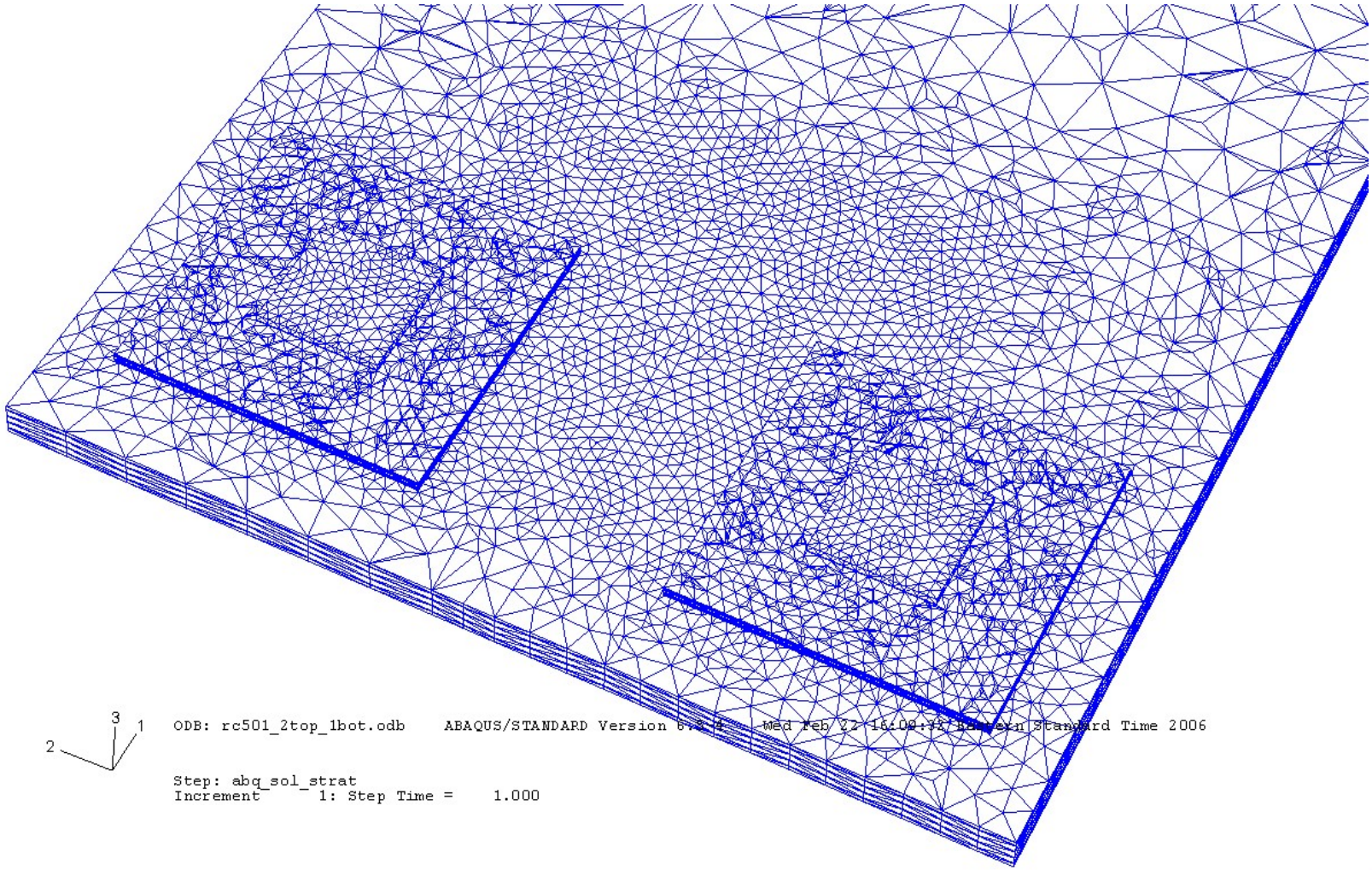




Dense off-pitch body interactions (challenging for FEA meshers)

Case 4: PCA with top & bottom PBGAs

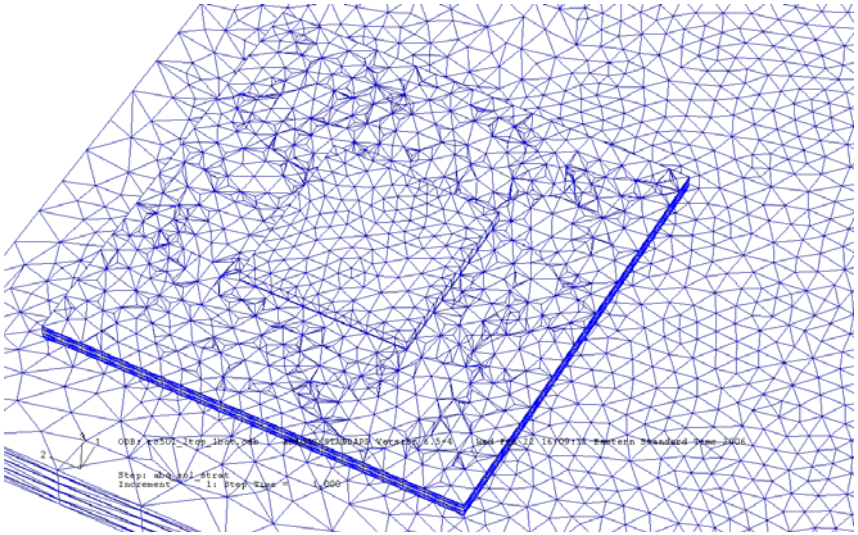
Mesh model in Abaqus as imported from native Abaqus format

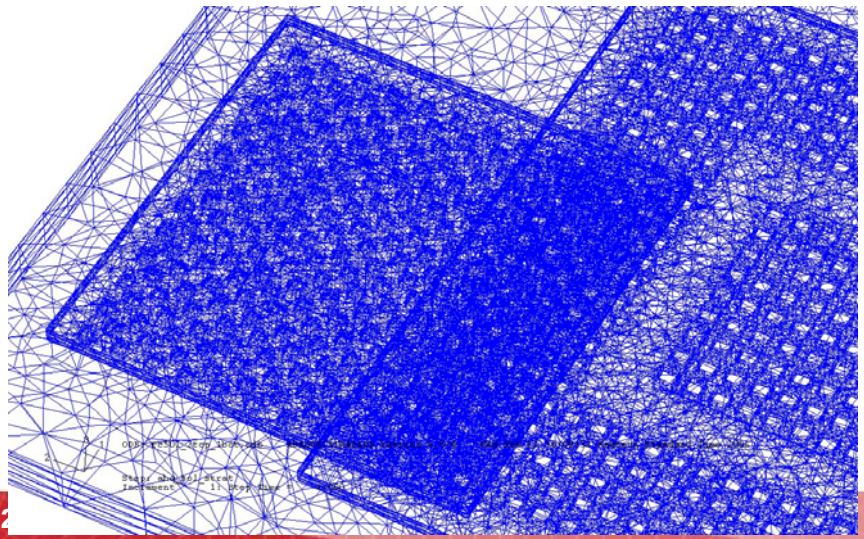


Case 4: PCA with top & bottom PBGAs

FEA mesh model in Abaqus (cont.)

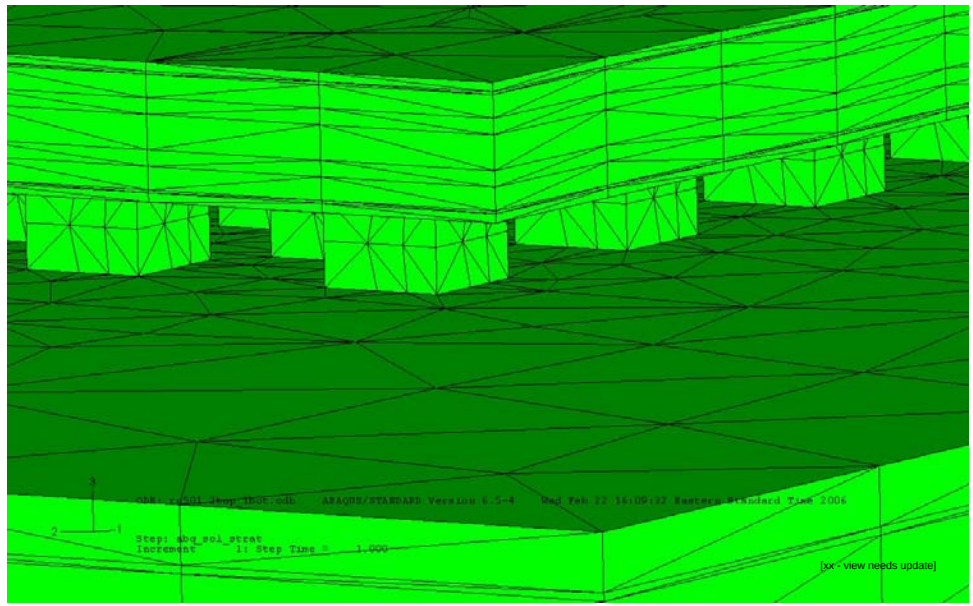
Mesh in dense chip package solder ball regions





(same region in full wireframe view)

Auto-generated mesh between chip package substrate layers, solder balls, and PCB layers

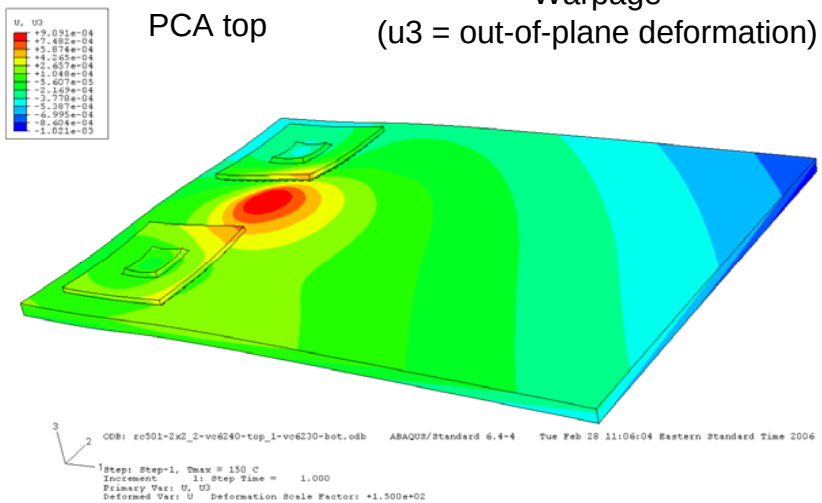


Case 4: PCA with top & bottom PBGAs

Solved FEA model in Abaqus

PCA top

Warpage
(u3 = out-of-plane deformation)



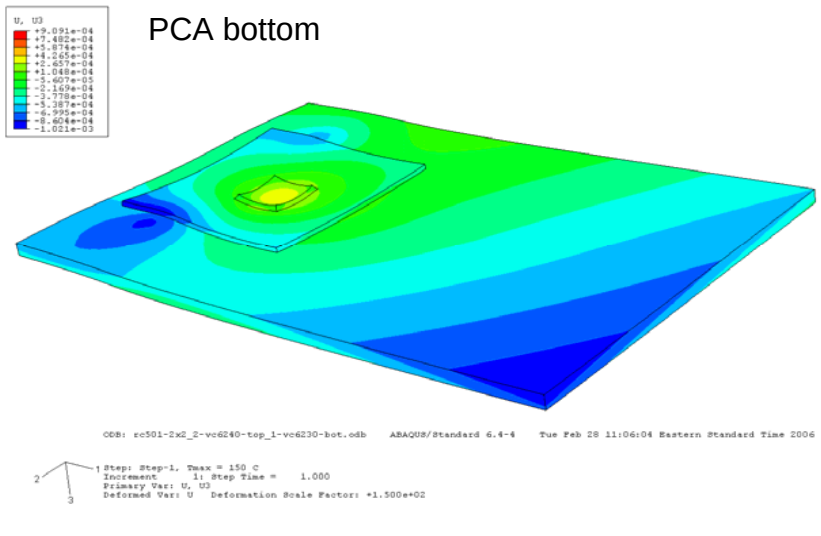
Preliminary Warpage Results

(to be further validated in Phase 2)

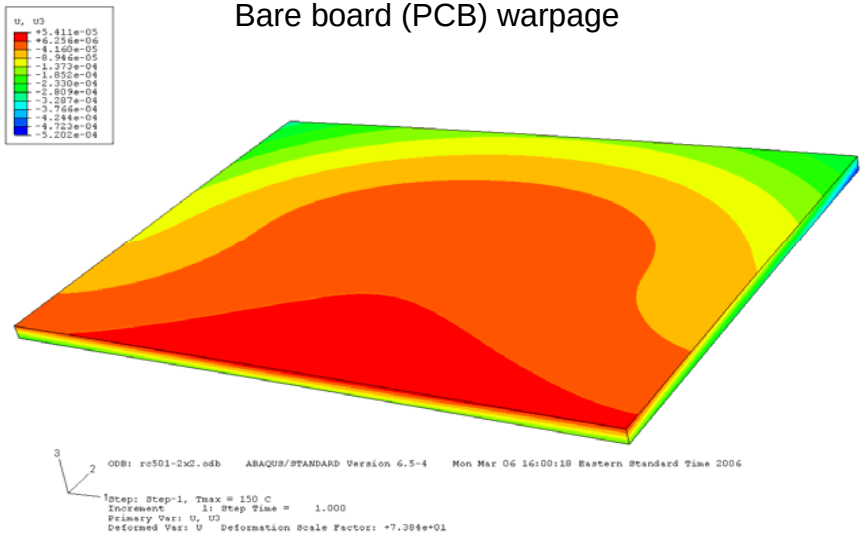
Results - Case 4:

- Demonstrated FEA meshing feasibility (main challenge)
- Good results, trends, and compatibility with similar cases [Ding, 2004; Powell, 2006]
- Results reveal anticipated asymmetric effects
  - High fidelity PCB model considers local feature density differences
- Future work will try more effective idealizations (ex. shells) & correlate with physical measurements

PCA bottom



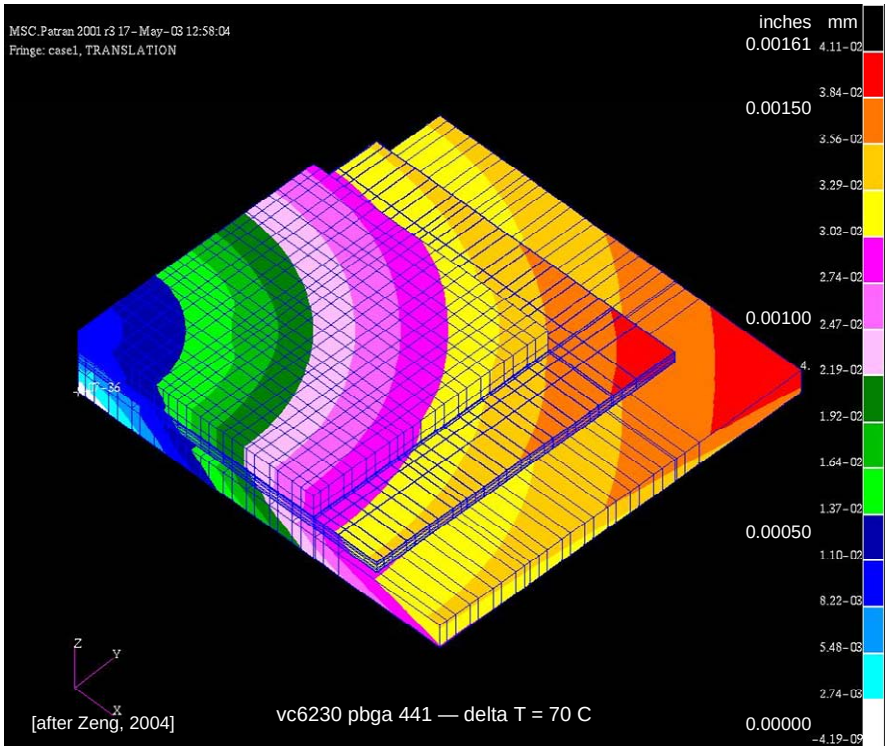
Bare board (PCB) warpage



Case 5: PBGA Chip Package on Sample PCB

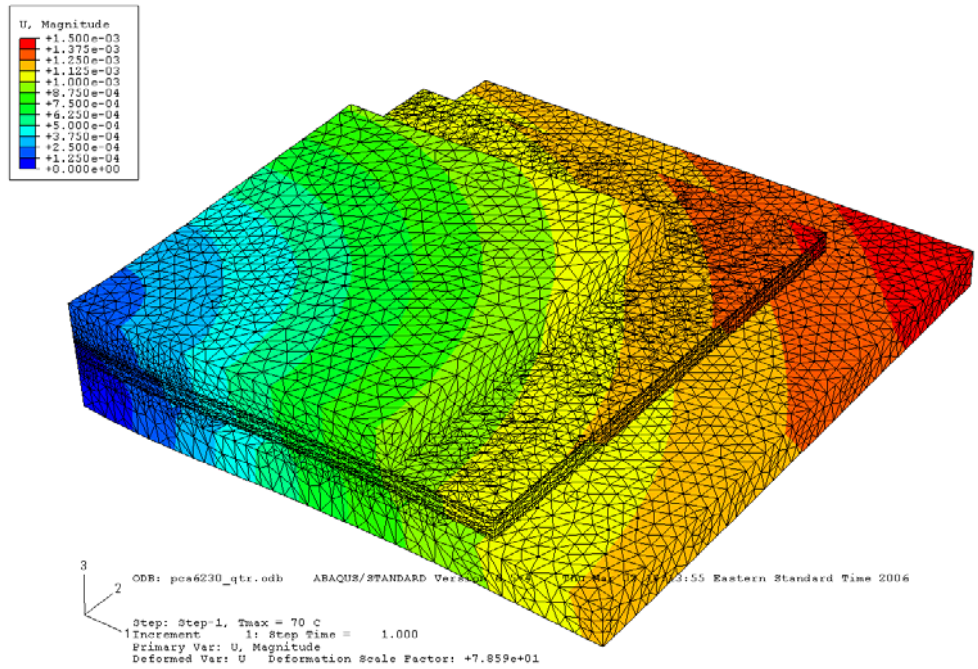
Deformation magnitude results: PCA 6230 (with PBGA 441)

Known Results [Zeng, 2004; Shinko]



XCP + Patran pre-processing
Abaqus solving and Patran post-processing

InterCAX SBIR Phase 1 Results



XE + Simmetrix pre-processing
Abaqus solving and post-processing

Phase 1 Results - Case 5

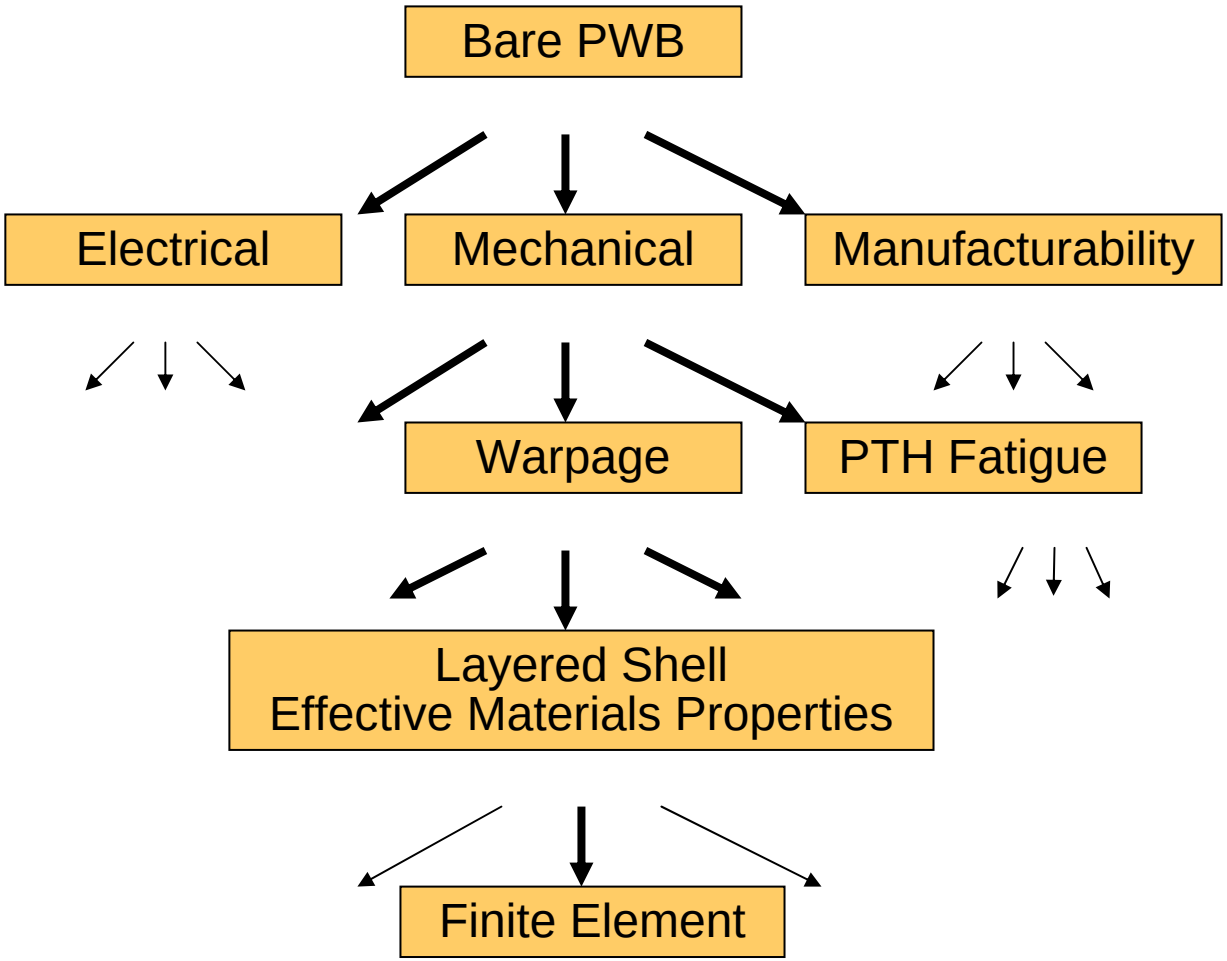
- Excellent comparison of deformation pattern
- Very good comparison of max. warpage values (1.61 mils vs. 1.50 mils = ~7% delta)
  - Possible deviation causes: different meshing approach, different solver version, etc.

Contents

- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results and Validation
- Methodology and Tools
  - Multi-Representation Architecture
  - Beta-level PWB warpage estimation tool
  - Prototype-level PWAB warpage estimation tool
- Conclusion

Multi-Representation Architecture (MRA) for Design Analysis Integration

Tree View



Manufacturing Product Model

Analysis Product Model

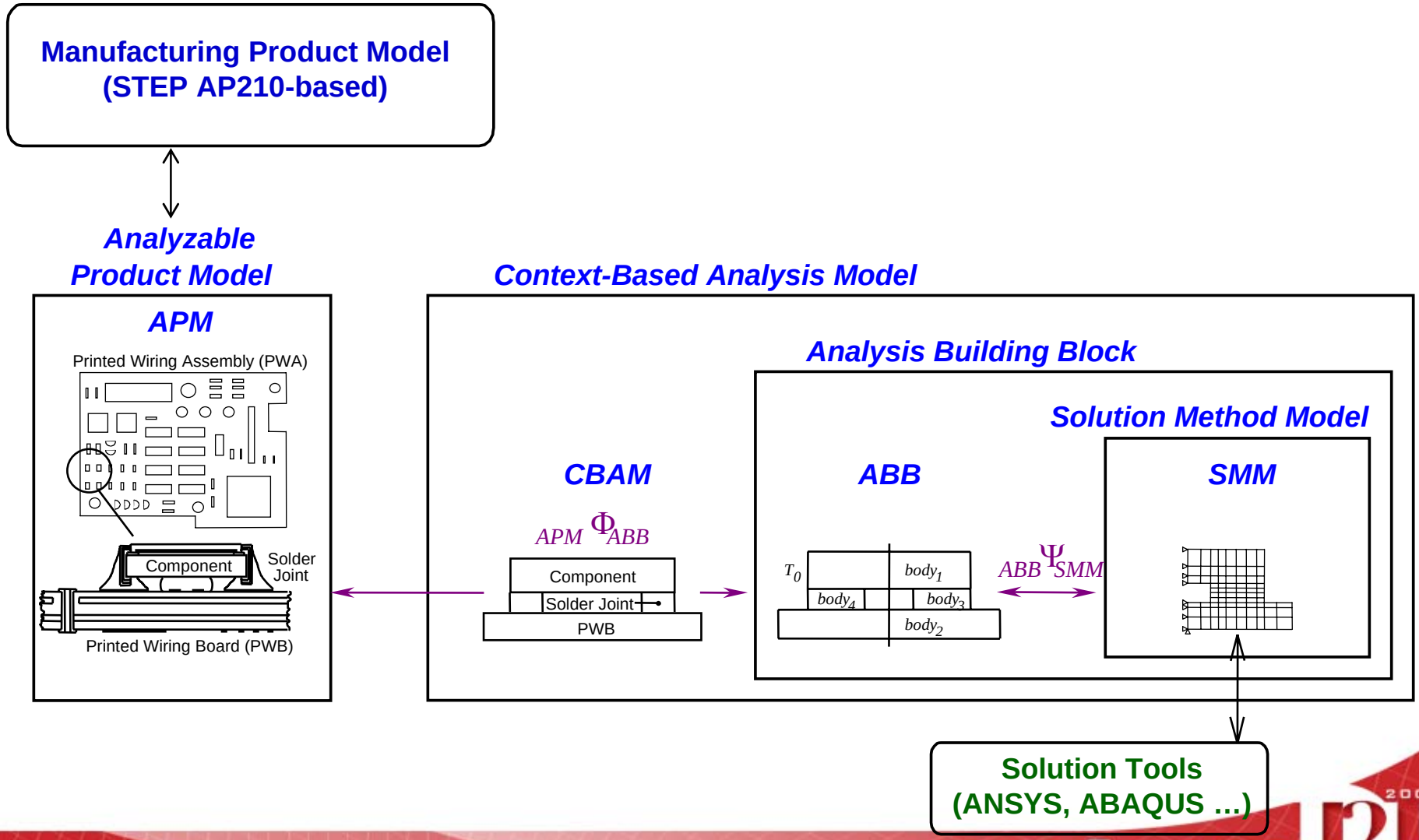
Context-Based Analysis Model

Analysis Building Blocks

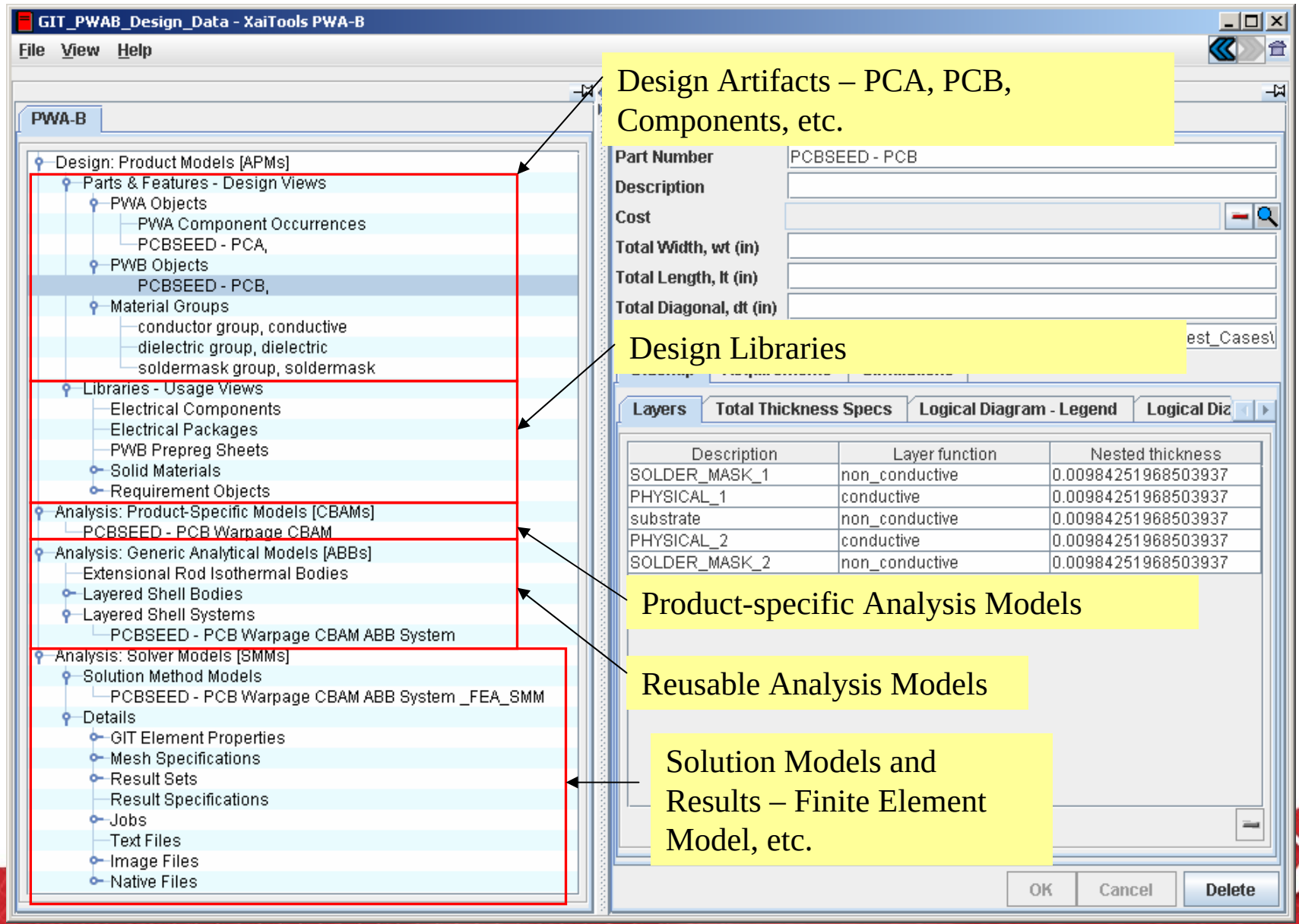
Solution Method Model

Multi-Representation Architecture (MRA) for Design Analysis Integration

Stepping-Stone Model View



MRA-based Model Browser



Status of Tools

- **STEP Book AP210 Pro v2.3 (LKSoft)**
  - **Import Mentor Board Station designs**
- **XaiTools PWA-B v2.0.b1 (Georgia Tech)**
  - **Stackup Editor**
  - **Bare Board Warpage Analysis**
- **XaiTools Electronics v1.0 Prototype (Georgia Tech)**
  - **PCA Warpage Analysis**

Invited Collaboration

- Collaboration Opportunities
  - Test Case Providers
  - Users of this service
  - Users of the tool
- Future Extensions
  - Bare board stackup design & warpage tool
    - Detailed stackup
  - PCA warpage tool
    - Alpha-level refinement

Summary

- Use of rich product models to drive high-fidelity analyses
- Stackup Design and Warpage Analysis
  - Bare board stackup design and warpage analysis
  - PCA warpage analysis
  - Initial validation
- Methodology and Tools
  - MRA-based design-analysis model management pattern
  - Beta level bare board stackup design and warpage tool
  - Early prototype PCA warpage analysis tool

NIST Disclaimer

This document may identify commercial product names and materials by other parties to describe certain procedures or to provide concrete examples (i.e., to help clarify abstract concepts via specific instances). In no case does product or material identification imply recommendation or endorsement by the authors or their organizations, nor does it imply that such items are necessarily the best available for the purpose. Company, product, or service names may be included that are trademarks or service marks of others.

USER2USER