Insights into the characterization of polymer-based organic thin-film transistors using capacitance-voltage analysis

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Frequency dependent capacitance-voltage characteristics of organic thin-film transistors based on poly(3-hexylthiophene) as the active polymer layer are investigated. The frequency response of the channel capacitance in accumulation is examined through an analytical transmission line model, with the effect of contact resistances included in the model to account for deviations from ideal behavior. The model provides an excellent fit to the data. Furthermore, we show that the technique can be used to extract device parameters such as the mobility and the contact resistance and quantitative information on the influence of charge trapping on transport. © *2008 American Institute of Physics.* [DOI: 10.1063/1.2917523]

Capacitance-voltage (C-V) measurements on semiconductor devices have played a critical role in advancing fundamental knowledge about semiconductor electronics and have helped enable their commercialization. This technique provides important information on the nature of the dielectric/semiconductor interface and charge transport within the semiconductor. In organic electronics, most of the work until now has been carried out on organic sandwich structures analogous to the metal-oxide-semiconductor (MOS) capacitors and was used to reveal the presence of traps at the insulator/semiconductor interface[1] or extract the dopant density[2,3] and bulk hole mobility[3] in these sandwich-type structures. Direct C-V measurements on bottom-gated, top-contact pentacene thin film transistors (TFTs) have been reported and used to extract charge carrier field-effect mobility and the fraction of mobile to fixed charges in the device.[4–6] However, a detailed analysis of the C-V data and the frequency response of the charge-accumulated channel of the transistor have yet to be presented.

In this paper, we report on the C-V characteristics of TFTs based on poly(3-hexylthiophene) (p3HT) as the semiconductor layer. A classical analytic treatment[7,8] based on the transmission line method of a distributed RC network is used to model the data. Excellent agreement between measured and modeled results is achieved once the effect of contact resistances is incorporated to account for deviations from ideal behavior. The importance of this technique and the modeling results becomes more apparent as they can be used to obtain quantitative information on contact and channel resistances, the channel mobility, and the effect of interface states at the semiconductor/oxide interface.

Devices are fabricated in a bottom-contact configuration on a degenerately doped n+ silicon wafer to be contacted as the gate electrode. The gate dielectric is thermally grown silicon dioxide (SiO_2) with a nominal thickness of (200 ± 5) nm. The Au source and drain electrodes were deposited by e-beam evaporation and patterned by photolithography and a lift-off process. The contacts have a nominal thickness of 40 nm. The p3HT films are cast from a 1.0 mg/mL solution in chloroform at room temperature at a rate of 500 rpm onto substrates rendered hydrophobic by immersion in a solution containing octadecyltrichlorosilane (OTS). Prior to OTS treatment, the Au electrodes are functionalized by immersing the substrates in a 10^{-2} mol/l pentaflurobenzenethiol solution in ethanol for 30 min to improve the injection properties of the contacts.[9] All processing and device characterization are carried out in an argon-ambient glovebox.

The active area of the device is isolated from the rest of the chip by carefully scribing the polymer film around the perimeter of the source and drain electrodes using a probe tip. The C-V characteristics are measured in the frequency range from 100 Hz to 100 kHz with an HP 4284a *LCR* meter.[10] The source and drain contacts are electrically shorted together and connected to the low terminals of the *LCR*, and the gate electrode is connected to the high terminals to measure the device capacitance C_{FET} (see inset of Fig. 2). A dc bias voltage in the range of −40–+40 V is applied through this terminal, along with a small ac probe signal of 0.1 V. The capacitance-frequency C-f data are collected by keeping the gate voltage (V_G) fixed and sweeping the frequency. No significant drift in the I-V or C-V characteristics of the devices was observed in the short span (typically less than 2 min) of the frequency sweeps. dc current-voltage characteristics of the TFTs are collected prior to C-V measurements.

Figure 2 shows a plot of C_{FET} as a function of V_G for several frequencies for a device with channel length/channel width (L/W) of 80/800 μm. Focusing on the C-V data at 100 Hz for the moment, we see that at $V_G > +10$ V the de-

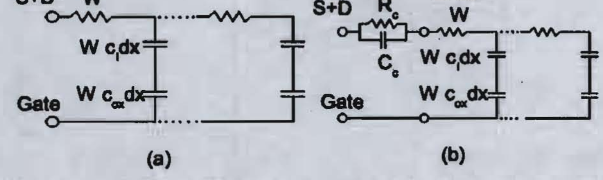

FIG. 1. (a) Equivalent circuit used for the distributed RC network model of the transistor channel to fit the data. (b) Equivalent circuit for the distributed RC network, taking into account the contact effects.

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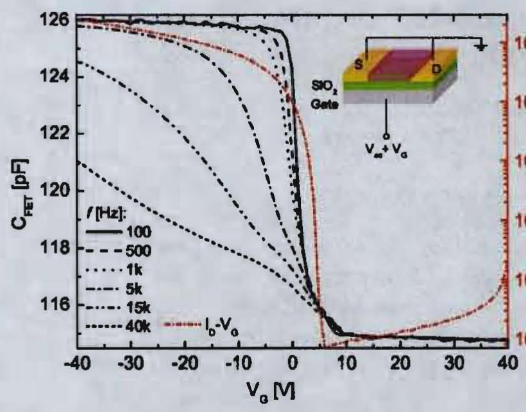

FIG. 2. (Color online) Plot of C_{FET} vs V_G for several frequencies. The transfer characteristics at V_D=−0.5 V is also plotted on the right axis (dotted line). Inset: cross section of the OTFT used for this experiment and cabling diagram for measurement setup.

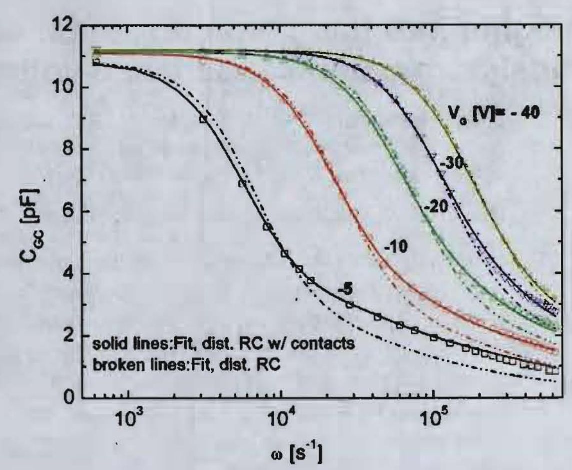

FIG. 3. (Color online) Plot of the gate to channel capacitance C_{GC} vs ω for several gate voltages and fits to the data based on the distributed *RC* network model, with [Fig. 1(c)] and without [Fig. 1(b)] contact effects.

vice is depleted of mobile charge carriers and, therefore, the capacitance measured is the combined capacitance of the source and drain electrodes with respect to the gate ($\approx$115 pF). At $V_G<10$ V, the channel is accumulated with holes injected from both electrodes, and C increases by $\Delta C = c_{ox}WL$, where c_{ox} (lower case) is the capacitance per unit area of the gate dielectric (approximately 1.62×10^{-4} F/m^2). The change in capacitance is rather abrupt and agrees well with the sharp turn on of the current in the device as obtained from the drain current versus gate voltage characteristics measured under dc conditions, also plotted in Fig. 2. Dispersion appears in the C-V plots at higher frequencies, the origin of which is discussed below.

In order to understand the C-V results presented in Fig. 2, we adopt a modified analytic model based on a transmission line *RC* network developed for MOS transistors[7] and polycrystalline Si TFTs.[8] The equivalent circuit model is shown in Fig. 1(a). The transistor channel is divided up into elements of length dx, with the resistance given by $dR = (r/W)dx$ and the capacitance given by $c'Wdx$. Here, we define r to be the sheet resistance, and c' is the series sum of c_{ox} and the interfacial capacitance (c_I), more precisely $c' = c_{ox}c_I/(c_{ox}+c_I)$. In accumulation, $c_I\rightarrow\infty$ and $c'\sim c_{ox}$, and, when fully depleted, $c'\sim 0$. The equivalent circuit in Fig. 1(a) can be solved analytically for the current i flowing into the channel, and the result is given by[7]

$$i = j\omega WLc'\frac{\tanh\lambda}{\lambda}v_0, \tag{1}$$

where j is the imaginary unit, ω is the angular frequency given by $2\pi f$, and v_0 is the amplitude of the probe signal. The term λ is given by

$$\lambda = \left(\frac{j\omega c' rL^2}{4}\right)^{1/2}. \tag{2}$$

The capacitance measured at the terminal is given by

$$C = \mathrm{Im}\left(\frac{i}{\omega v_0}\right). \tag{3}$$

After substituting Eq. (1) in Eq. (3), we obtain

$$C = c'WL\,\mathrm{Re}\left(\frac{\tanh\lambda}{\lambda}\right). \tag{4}$$

IM and RE refer to the imaginary and real parts of the expressions in the parenthesis, respectively. The dependence of C on V_G is implicit in the sheet resistance r. Ignoring parasitic contact resistances for the moment $r=R_{tot}W/L$, where R_{tot} is the total device resistance. Equation (4) predicts an explicit frequency dispersion for C, like that shown in Fig. 2. At higher frequencies, the charge carriers (originating from the source/drain contacts) cannot respond to the signal due to the finite *RC* time constant associated with the gate to channel response. We plot in Fig. 3 C_{GC} versus ω, at several gate voltages along with the results of the modeling based on Eq. (4). Here, we have subtracted the combined capacitance of the source and drain electrodes with respect to the gate from the total field-effect transistor (FET) capacitance to consider only the channel response C_{GC}. The broken lines in this figure are best fits to the data. At the highest gate voltages, a small deviation can be seen in the high frequency tail. As V_G is lowered, the deviation becomes more apparent, and the R_{tot} values used to fit the data (see Table I) significantly deviate from those obtained from the I_D-V_G plot.

Thus far, we have ignored the possible effects of contact resistances on the C-V results. However, the contact resistances have been shown to play an important role in bottom-contact organic TFTs.[11,12] For the study of contact effects, a gated transfer line method (TLM) has frequently been used to discern contact and channel resistances in organic TFTs.[12] Initially, we performed a gated TLM analysis (at a small V_D=−0.5 V) on a few devices with different L on the same chip to see whether contact effects are significant.[11] We found that, at high negative V_G, the contact resistance R_C for the L=80 μm device is at least an order of magnitude smaller than the channel resistance R_{ch}. We will show that the C-V measurement, however, is extremely sensitive to minute contact effects.

Here, we propose a modified version of the *RC* transmission line network. A contact component, consisting of a resistance element R_c in parallel with a contact capacitance element C_c is added to the model. The equivalent circuit is shown in Fig. 1(b). The impedance Z_c of this additional contact component is

TABLE I. Parameters used to model the C-f data shown in Fig. 3.

V_G (V)	R_{tot}[a] (MΩ) (±5%)	R_{ch}[b] (MΩ) (±5%)	R_c[b] (MΩ) (±5%)	C_c[b] (pF)	C_I[b,a] (pF)	C_{ox}[b,a] (pF)	R_{ch} Gated TLM (MΩ)	R_c Gated TLM (MΩ)	R_{tot} I-V (MΩ)
−40	4.4	3.0	0.13	17	2000	11.25	3.1	0.21 ± 0.11	4
−30	7.2	4.2	0.24	17	2000	11.25	4.35	0.21 ± 0.15	5.6
−20	12	6.4	0.52	13	1000	11.25	6.58	0.20 ± 0.23	8.5
−10	35	13	1.9	8	800	11.25	12.1	0.11 ± 0.43	15.7
−5	130	35	9	6	300	11.25	20.5	···	25

[a]Parameters used only in the distributed RC model without contacts.
[b]Parameters used in the distributed RC model with contacts.

$$Z_c = \frac{jR_c}{j - C_c R_c \omega}, \tag{5}$$

and the current flowing through the device is now given by

$$i = j\omega W L c' \frac{\tanh \lambda}{\lambda}(v_0 - iZ_c). \tag{6}$$

The sheet resistance r is now given by $r = R_{\text{ch}} W/L$, where R_{ch} is the channel resistance and is related to the total device resistance by $R_{\text{tot}} = R_{\text{ch}} + R_c$.

Solid lines in Fig. 3 show the best fit to the data using Eqs. (3) and (6). The parameters used for all the modeling are shown in Table I. Our modified RC model with the contacts produces excellent fits to the data over the entire frequency range, and the resistance values used in the model agree well with the contact and channel resistance extracted from gated TLM analysis, as well as the total device resistance.

The addition of the contact capacitance term C_c to the model is essential, enabling the model to produce an excellent fit at the high frequency tail of the C-ω data. The origin of this capacitance is most probably due to the formation of a small depletion region near the metal/organic contact.

The model parameter C_I has traditionally been associated with interfacial traps or, in the case of bulk MOSFETs, it is the parallel sum of the trap and the depletion capacitances. In organic semiconductors, the distribution of electronic states are considered to be energetically disordered;[13] therefore, it is more relevant to view C_I as the capacitance associated with moving the Fermi level through a distribution of tail states as V_G goes from accumulation to depletion. Since the number of accessible states in the tail of this distribution as well as conduction between such states is reduced when V_G becomes more positive, the value of C_I drops.

To further demonstrate the utility of C-V measurements, we return to the low frequency C-V data from Fig. 2. As has been previously reported in pentacene TFTs, one can calculate the accumulated mobile charge in the channel by integrating the area under the C-V curve up to a certain V_G.[5,6] Since there is very little dispersion in the C-f plots below the frequency of 1 kHz, we can use any set of C-V curves collected up to this frequency value. Integrating under the 100 Hz C-V plot from +40 to −40 V gives a sheet charge density of 0.0072 C/m^2. Using this value to calculate the mobility from the transfer characteristics, we arrive at a low-field mobility value of 0.035 $\text{cm}^2/\text{V s}$. This favorably compares with the mobility of 0.036 $\text{cm}^2/\text{V s}$ extracted in the linear regime from the transconductance.[12] The close agreement in results provides evidence that the majority of charge carriers are mobile, and that the mobility extracted by using equations describing the I-V characteristics of MOSFETS is a reasonably accurate value.

In conclusion, we have performed capacitance-voltage measurements on bottom-contact organic transistors based on p3HT. A modified analytical technique based on a distributed transmission line model was used to produce excellent fits to the data. Importantly, our ability to analyze the C-V data of comparatively low-mobility polymer TFTs within a framework developed for classical semiconductors such as Si has important implications for advancing the fundamental understanding of electronic structure in these systems and the nature of charge transport.

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