NISTIR 7513

Semiconductor Microelectronics and Nanoelectronics Programs

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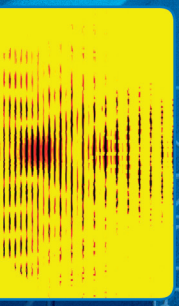
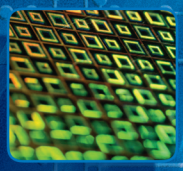
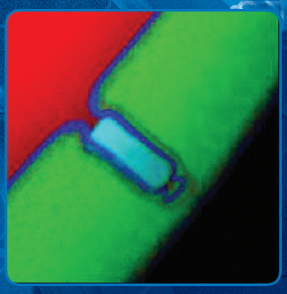
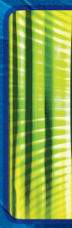
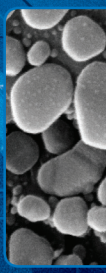
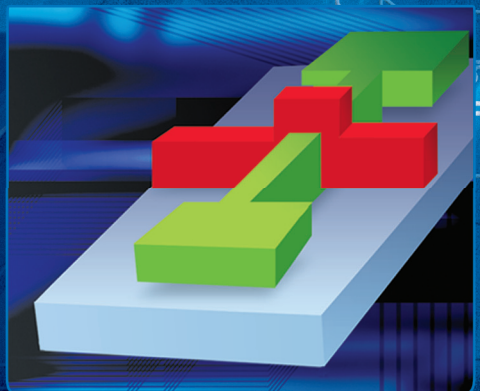
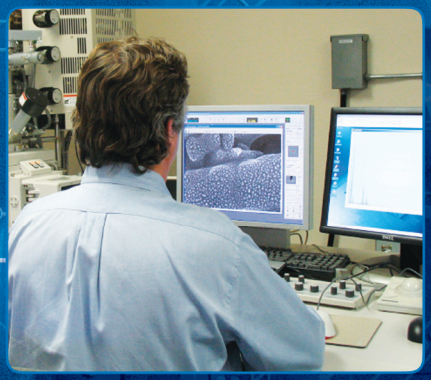
July 2008

NIST
National Institute of Standards and Technology
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On the cover (top left to right):

CD-SAX data of a FINFET test pattern from Jim Price of SEMATECH. Work initiated in late-2007.
Circuits on a wafer.
Scanning Electron Microscope (SEM) image of gold on carbon.
Energy filtered Transmission Electron Microscopy (TEM) image of FinFET cross section.
Another part of the CD-SAX data of a FINFET test pattern from Jim Price of SEMATECH.

Bottom left to right:

A double-gate FinFET device.
STAR Cryoelectronics Microcalorimeter X-ray Spectrometer.
Helium Ion Microscope (HIM)image of gold-on-carbon.

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July 2008

U.S. DEPARTMENT OF COMMERCE
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Disclaimer

Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the International Technology Roadmap for Semiconductors (ITRS) apply to the most recent edition, dated 2007.

Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors, 2007 edition.* SEMATECH: Austin, TX, 2007.

These documents are available on-line at: http://www.itrs.net for downloading.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

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Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the U.S. Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of 60 with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the U.S. Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which is providing a $12 million budget in fiscal year 2008.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, SEMATECH and its subsidiary, International SEMATECH Manufacturing Initiative (ISMI), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP and NIST Laboratories represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS), as well as on numerous SRC Technical Advisory Boards. NIST staff is also active in the International National Electronics Manufacturers Initiative (iNEMI), the EIA, the International Organization for Standardization (ISO),

and Semiconductor Equipment and Materials International (SEMI). NIST supports the United States National Committee Technical Advisory Group for the International Electrotechnical Commission Technical Committee TC113 on Nanotechnology Standardization for Electrical and Electronic Products and Systems (Technical Advisor, USNC TAG for IEC TC 113 on nanotechnology) by funding the Technical Advisor to that organization.

Learn More About Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact:

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Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The workhorse tools at this point operate at 193 nm. In order to further shrink dimensions liquid immersion tools with water as the immersion fluid have been introduced. Further size reduction through the use of high index fluids, lens materials and photoresist for 193 nm tools are under intense exploration for even higher numerical aperture systems. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. At least three alpha tools were shipped to development consortia in 2006. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials and immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.

Metrology Supporting Deep Ultraviolet Lithography

Goals

Develop solutions to key optical metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of DUV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs

Increasing information technology requirements have created a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate optical measurements at DUV laser wavelengths.

193 nm immersion lithography, with water as an immersion fluid, is now being commercially implemented with numerical apertures (NA) near 1.3. The industry is exploring the possibility of extending this technology to higher NAs using higher-index immersion fluids and by incorporating a high-index material as the last lens element. Design and development of this extension technology requires finding appropriate high-index fluids and lens materials, and accurate measurements of their index properties.

To support these efforts, the National Institute of Standards and Technology (NIST), with

SEMATECH, has developed a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential challenges for lithographic development are discussed in the 2007 International Technology Roadmap for Semiconductors. Page 1 of the Lithography section states: "Significant technical challenges exist in extending optical projection lithography at 193 nm wavelength using high-index immersion lenses…." The need for advancing metrology in lithography is discussed on page 1 of the Metrology section: "Metrology continues to enable research, development, and manufacture of integrated circuits. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability."

Technical Strategy

High-accuracy measurements of the index properties of UV materials are required for the design of DUV lithography systems. NIST has been providing absolute index measurements at 193 nm and 157 nm with an accuracy of about 5 ppm to the industry using its DUV minimum-deviation-angle refractometer. To improve on this absolute accuracy, NIST has constructed a new state-of-the-art minimum-deviation system and separately developed another system based on a vacuum ultraviolet (VUV) FT spectrometer and synchrotron radiation as a continuum source (see Fig. 1). Both of these systems enable measurements to an accuracy of 1 ppm, and are used to characterize high-index lens materials and immersion fluids for 193 nm lithography systems.

DELIVERABLES:

- Measurement of the refractive index of fused silica, CaF2, and water, as well as high-index fluids and high-index lens materials, with an accuracy of 1 ppm. Ongoing.

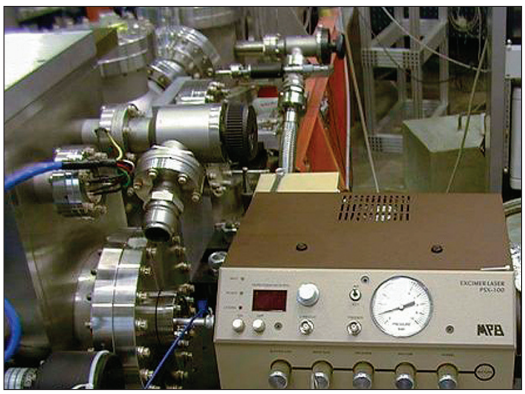

Figure 1. Facility for detector VUV radiation damage study using synchrotron radiation from SURF and a 157 nm excimer laser.

Technical Contacts:
J. H. Burnett
M. Dowell

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild,
Massachusetts Institute
of Technology's
Lincoln Laboratory

Taking full advantage of the potential resolution gain with immersion lithography may require using high-index materials for the last lens element, though as yet no such material has been demonstrated at 193 nm. To address this need we have, with the support of SEMATECH, undertaken and completed a survey of candidate materials. As a result of this work, we have identified two very promising materials, ceramic spinel and lutetium aluminum garnet (LuAG). Both materials have indices near 2.0 at 193 nm and have the potential for high optical quality at this wavelength. In addition, the intrinsic birefringence is low for LuAG and negligible for ceramic spinel. We are now characterizing the complete UV optical properties of these materials. Since high-NA immersion lithography requires polarized illumination, a further high-index candidate material becomes possible, namely sapphire, a uniaxial crystal. Though a naturally birefringent material, selectively polarized illumination enables a restriction to the isotropic ordinary rays, and low-aberration optics becomes possible. To assess this candidate's feasibility, we are now characterizing its complete optical properties, including any spatial-dispersion-induced anisotropy effects.

DELIVERABLES:

- Fully characterize the 193 nm optical properties of LuAG, ceramic spinel, and sapphire: 4Q 2008.

An absolute light source in the DUV range based on synchrotron radiation using NIST's Synchrotron Ultraviolet Radiation Facility (SURF III) has been established using a dedicated beamline at SURF III. The flux of the DUV radiation at this beamline can be known to very high accuracy through the well established equations governing the behavior of the synchrotron radiation. The beamline is designed for customer calibration of a variety of DUV instruments to assist the development of the DUV lithography such as monochromators, discharge lamps, and irradiance meters. The spectral range covers all of the current important wavelengths for semiconductor industry such at 248 nm, 193 nm, 157 nm, down to 13 nm. The uncertainty of such calibration is better than 1 % in the case of deuterium lamp calibration.

DELIVERABLES:

- Provide customer DUV calibration for discharge lamps, monochromators, and irradiance meters using SURF III source-based beamline with highest accuracy. Ongoing

Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, and specifically KrF (248 nm) and ArF (193 nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 nm, 248 nm, and 157 nm. Figure 2 shows the excimer laser calibration facility.

Figure 2. Laboratory for excimer laser energy and power meter calibrations, with measurement systems for 248 nm, 193 nm, and 157 nm. The excimer lasers are along the top right and the enclosures for nitrogen gas purging are in the foreground.

DELIVERABLES:

- Proven high-quality calibration services, and supporting measurements for excimer laser power and energy meters to the Semiconductor Industry at 248 nm, 193 nm, and 157 nm. Ongoing

Accomplishments

■ We have used our Hilger-Chance refractometer system to assist the industry in the search for appropriate high-index fluids (with n greater than water, 1.4366 at 193 nm) for possible use in immersion lithography resolution extension. Several promising fluids have been developed by industry, and we have characterized their UV optical properties. Recently we have worked with the suppliers to demonstrate that several of these candidate fluids have stable optical properties over multiple exposure runs.

As a result of our high-index materials survey, we have identified two very promising high-index 193 nm transmitting materials, that can potentially enable immersion lithography extension. These candidates are ceramic spinel and lutetium aluminum garnet (LuAG). We have demonstrated that both materials have good 193 nm optical properties, including sufficiently low spatial-dispersion-induced ("intrinsic") birefringence (see Fig. 3). Due to the results of our measurements, LuAG and ceramic spinel are now being developed by the industry for this application.

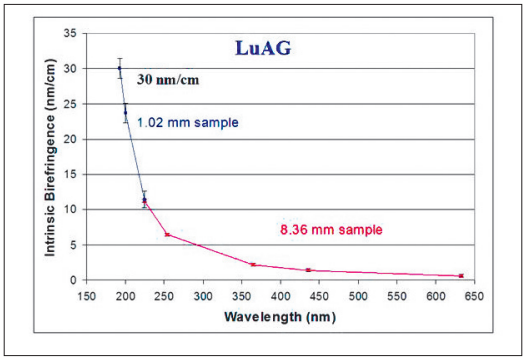

Figure 3. Measurement of the intrinsic birefringence of LuAG vs. wavelength.

■ We have constructed a radiometric facility tailored for the DUV range using a beamline at NIST's SURF III with the radiation measurement scale derived from a high-accuracy cryogenic radiometer. The beamline is designed for general-purpose high-accuracy measurements. We have used this facility to measure DUV material properties such as transmission and reflectance. Examples of such measurements include DUV mirrors, windows, filters, and also the transmission and absorption of liquids that could be used for immersion lithography. On the detector side, we have calibrated and characterized a variety of DUV detectors such as solid state photodetectors, solar-blind detectors, photoconductive detectors, and pyroelectric detectors. We also performed irradiance calibrations for DUV irradiance meters.

■ We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation (see Fig. 4) and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of integrated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total dose from an F2 excimer laser operating at 157 nm. Different changes were seen in different diodes depending on the total excimer irradiation dose which included changes in spectral responsivity well. This provides important information about the mechanism responsible for the degradation of the photodiodes. For example, we have determined that for silicon photodiodes under irradiation with a 157 nm excimer laser, an important mechanism for degradation is the formation of trap states at the interface of the silicon-silicon dioxide induced by the damaging radiation. These trap states act as recombination centers and reduce the yield of electric current generated by incident radiation. A model was developed to simulate the change in response for photodiodes irradiated by 157 nm radiation.

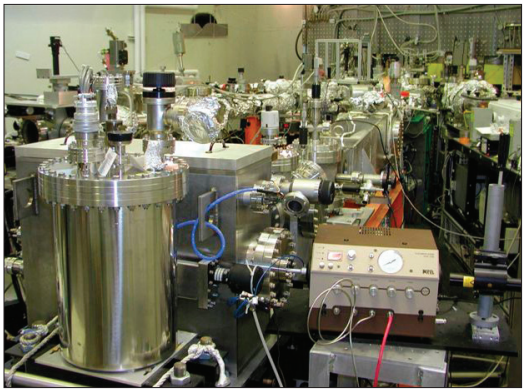

Figure 4. Measurement system for detector damage study by a 157 nm pulsed excimer laser.

■ During the last 15 years we have developed a suite of laser calorimeter standards for 248 nm, 193 nm, and 157 nm excimer laser energy and power measurements traceable to SI units. The 248 nm and 193 nm calorimeters use a specially designed absorbing cavity with a volume absorbing glass to reduce potential damage to the cavity by the high peak power in the UV laser pulses. The 157 nm calorimeter is a fundamentally new type of laser calorimeter standard that uses a thin-walled SiC absorbing cavity, which is designed to completely absorb and spread the incoming laser energy through multiple reflections. All of these calorimeters are calibrated using an imbed-

ded electrical heater that allows for traceability to SI units through electrical standards of resistance and voltage. Calibrations for industry customers are accomplished for each wavelength with appropriate measurement systems that involve purging of oxygen to eliminate atmospheric absorption of the laser radiation.

■ As a further extension of our excimer laser services we have developed the capability to directly measure UV irradiance or "dose" at 248 nm and 193 nm, which involves homogenizing the beam profile and measuring the energy transmitted through a calibrated aperture. This capability can improve accuracy for customers who need to measure the energy absorbed at a surface such as the wafer plane.

■ We have also developed the capability to characterize the nonlinear response of 193 nm and 248 nm excimer laser detectors based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. Using this system, one can easily discover problems such as those due to the incident pulse energy, range discontinuities associated with detector gain, and detector background noise (see Fig. 5).

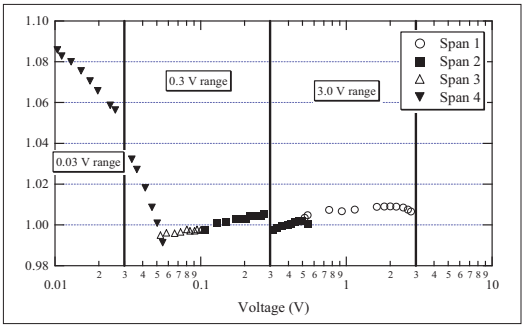

Figure 5. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

We completed the first internal comparison of the NIST UV excimer laser calorimeters. This work includes measurements taken over the course of a two-year period in which the performance of the NIST 157 nm, 193 nm, and 248 nm excimer laser calorimeters was monitored at the design wavelengths as well as at the other excimer laser wavelengths. The results show good agreement among the transfer standards and excellent stability over time. From these data, we determined that the responsivity of the NIST UV laser calorimeters all agree within their stated uncertainties. In all but one case, the calorimeters' responsivities agree to better than 0.3 %. The comparison between the DUV (193 nm) and UV (248 nm) calorimeters at 248 nm uncovered a 1 percent difference between the calorimeters' responsivities. This difference is due to partial transmission of the 248 nm radiation through the absorbing glass of the DUV calorimeter which, reduces the calorimeter's absorptance and alters its response.

Collaborations

DuPont, Roger French, immersion photolithography fluid development. Schott Lithotec, Lutz Partier, high index lithography materials development.

Publications

S. G. Kaplan and J. H. Burnett, *"Optical properties of fluids for 248 nm and 193 nm immersion photolithography,"* Applied Optics 45, 1721 (2006).

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S. Yang, D. A. Keenan, M. L. Dowell, *"Nonlinearity Measurements of the Response of Silicon Photodiodes at 193 nm,"* Council for Optical Radiation Measurement (CORM) 2005, May 10-12, 2005, Boulder, Colorado, (Approved by NIST for publication).

H. Laabs, D. A. Keenan, S. Yang, M. L. Dowell, *"Measurement of detector nonlinearity at 193 nm,"* Appl. Opt., Vol. 44, No. 6, pp.841-848 (20-FEB-2005).

Metrology Supporting Extreme Ultraviolet Lithography

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C. Tarrio
S. Grantham
S. Hill
R. Vest

Goals

Provide leading-edge metrology for the development and characterization of sources, optical components, and dosimeters used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

An intense international effort is presently underway to install EUVL into commercial production in 2012 at the 32 nm node. ASML has delivered two alpha-generation steppers for initial testing, one to SEMATECH in Albany and one to IMEC in Belgium.

Several significant challenges to commercialization of EUVL remain, including source power, optics lifetime, and optics and mask fabrication. The associated metrological challenges include the development of: (1) highly precise extreme ultraviolet (EUV) reflectometry; (2) accurate EUV radiometry for source comparisons, wafer-plane dosimetry, and resist characterization; and (3) predictors of EUV optics lifetimes.

Technical Strategy

1. Precise EUV Reflectometry

The NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics up to 40 cm in diameter and 40 kg in mass. The facility has a demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.001 nm, with plans underway to improve each in the near future.

The Facility serves the EUVL community by providing accurate measurements of multilayer mirror reflectivities and radiometric measurements on fully assembled instruments. Among the recent activities in support of EUVL is the reflectivity map made of the very large condenser mirror for a leading source manufacturer, the radiometric calibration of the "Flying Circus II" and "E-Mon" radiometers used for the comparison of source outputs, and reflectivity measurements made to determine the reflectivity loss due to resist outgassing. The reflectivity of a typical mirror designed for use in a EUVL stepper is shown in Fig. 1.

DELIVERABLES:

- Full reflectivity maps of EUV mirrors up to 40 cm in diameter and 45 kg in mass on an as needed basis for the EUVL community. Many other types of EUV measurements including

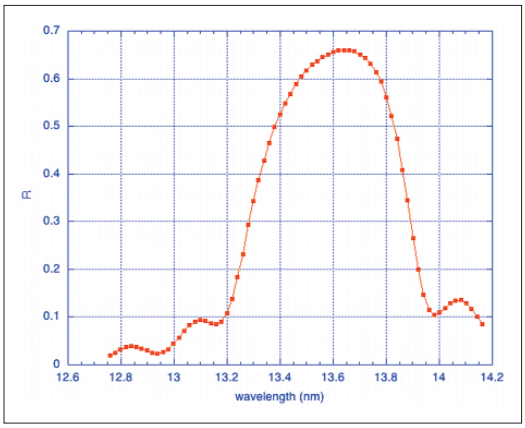

Figure 1. Reflectivity vs. wavelength of a typical MoSi multilayer mirror. The measurement was made at 5° from normal incidence.

  EUV filter transmission and cw radiometric calibrations of fully assembled filter radiometers used in source comparisons.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. The Photon Physics Group is responsible for maintaining the spectral responsivity standards in the far- and extreme-ultraviolet spectral regions, including 13.5 nm, the EUVL wavelength of interest. We operate several beamlines at the SURF III synchrotron radiation facility, a quasi-cw source, as well as a laser-produced plasma source that is pulsed with a 10-ns pulse length. With these facilities, we can calibrate EUV detectors and dosimeter packages under either cw or pulsed conditions.

NIST has recently added the capability to measure the absolute sensitivity of EUV photoresists. Until recently, EUV photoresist sensitivity was referenced to a "standard" photoresist whose sensitivity had last been measured in the 1990s. Late in 2007, scientists at the Advanced Light Source in Berkeley, CA used a NIST-calibrated EUV photodetector to validate this resist-based transfer

standard method. Their detector-based measurements indicated that the sensitivity of a modern resist was about twice that previously measured using the resist-based calibrations. Subsequently NIST established the capability for the accurate measurement of EUV resist sensitivity to independently validate these surprising results and to provide similar detector-based measurements for future resist evaluations. A team has been created with members of the Electron and Optical Physics Division, the Polymers Division, and the Center for Nanoscale Science and Technology (CNST) to use the new special instrumentation at the NIST SURF III Synchrotron Ultraviolet Radiation Facility to conduct EUV exposure measurements and to provide for the tightly controlled pre- and post-exposure processing of the resist. The NIST measurements confirmed the findings of the much higher resist sensitivity made in Berkeley thus showing the resist-based standard method to be erroneous.

DELIVERABLES:

- Photodiodes and other EUV radiometric devices as needed basised on customer requests
- Radiometric calibrations as needed basised on customer requests
- Resist dose to clear Eo measurements on customer as needed basised requests

3. Study of Factors Affecting EUV Optics Lifetime

One of the potential showstoppers for commercialization of EUVL is the degradation of the multilayer-mirror stepper optics. The mirrors lose reflectivity because adsorbed contaminant gases such as hydrocarbons and water are cracked by the energetic (13.5 nm) photons. This leads to growth of an amorphous carbon layer on the optics surfaces or to oxidation. The former effect is largely reversible; however, the latter is not. Unfortunately, these ambient contaminants cannot be eliminated by baking because the alignment of the mirror stack must be maintained to submicron tolerances and because of the presence of the outgassing from the resist coated wafer as it is being exposed.

The oxidation and carbonization are actually competing processes, and preliminary demonstrations have shown that the addition of a hydrocarbon can result in the deposition of a sacrificial layer of carbon that inhibits the oxidation of the cap layer that is used to protect the optic. The present strategy by the stepper manufacturers is to attempt to find a point in the oxidation-carbonization balance that leaves an oxidation-resistant cap layer, such as ruthenium, undamaged.

To study the effectiveness of such a strategy and to better understand the underlying processes responsible for mirror degradation, NIST has installed two beamlines at the Synchrotron Ultraviolet Radiation Facility (SURF III) that can expose capped-multilayer samples to ≈ 6 mW/mm2 of 13.5 nm radiation in an environment of controlled water or hydrocarbon partial pressures up to 6.7×10-4 Pa. To date the most oxidation-resistant capping layers available have been ~ 2 nm of ruthenium or ~ 2 nm of titanium dioxide. Our exposure facility has demonstrated that multilayers with these capping layer suffer approximately one-tenth the reflectivity loss of bare Si-capped multilayers when exposed for ≈ 100 h under rather aggressive oxidation conditions of 1×10-4 Pa of water vapor. In addition to measuring the reflectivity loss of exposed multilayers, the photon-induced chemistry on the mirrors is characterized using a range of surface analysis techniques including micro XPS.

The dominant mechanism of reflectivity loss of optics observed in pre-production tools has been carbon deposition. As shown in figure 2, high-dose exposures performed in our facilities have revealed very different rates of carbonization for different gases and a distinctly non-linear dependence of these rates on partial pressure. Similar logarithmic pressure dependence has been observed during exposures in benzene as well. This behavior can be explained in terms of a well known adsorption dynamic based on interactions between adsorbed and ambient gas molecules. If ongoing work demonstrates that this logarithmic trend is present for very-low-dose exposures as well, it could help define acceptable limits of background gases.

Each of the various organic molecules emitted by an irradiated resist or other material in the stepper vacuum will have a different effect on the optics. NIST has devised two new methods in an attempt to identify and quantify both the organic species in a stepper vacuum and those emanating from an irradiated resist. The first uses a vacuum cryotrap

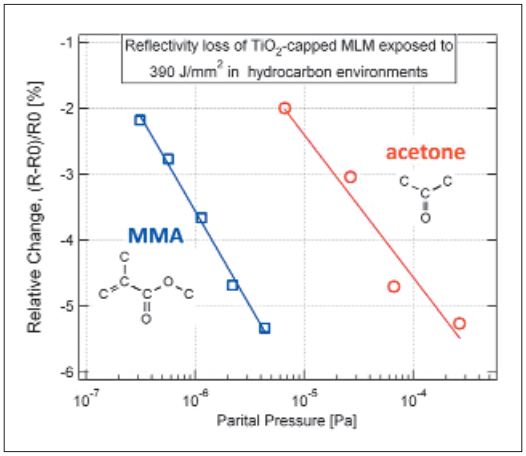

Figure 2. Reflectivity loss of a TiO2-capped multilayer mirror plotted as a function of the partial pressure of MMA (blue) and acetone (red). Note that the reflectivity loss depends on the logarithm of the pressure in the ranges studied for both species.

to obtain a sample from a stepper vacuum which is later subjected to Gas Chromatography followed by Mass Spectrometry (GC/MS) analysis in a specially equipped gas chromatograph, and the second uses a special chamber that can be hooked up to an EUV source to irradiate a 4-inch wafer, collect the outgas, and measure the total outgas per unit area by the pressure rise method and sample and analyze the collected outgas with the same cryo-trapping plus GC/MS technique as for the stepper vacuum.

In addition to expanding our facilities, we have also established very fruitful collaborations with experts in surface science both within and outside the NIST community.

DELIVERABLES:

Identify and quantify EUV resist outgas for resist manufacturers, tool makers, and tool users on an as needed basis.

Rank reflectivity loss as a function of organic species and the presence of mitigating oxidative species according to industry needs.

Collaborations

VNL at Lawrence Livermore National Laboratory, Saša Bajt, EUV Multilayer Development and Coating Team.

Publications

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Polymer Photoresist Fundamentals for Next-Generation Lithography

Goals

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. This program provides a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 50 nm structures. The unique measurement methods we apply include specular and off-specular X-ray and neutron reflectivity (XR, NR), small-angle neutron scattering (SANS), near-edge X-ray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), solid state nuclear magnetic resonance (NMR), atomic force microscopy (AFM), infrared variable angle spectroscopic ellipsometry (IR-VASE), and polarization-modulation infrared reflectance spectroscopy (PMIRRAS). Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the photoresist architecture and polymer conformation within sub 50 nm structures; (2) the spatial segregation and distribution of critical photoresist components; (3) the transport and kinetics of photoresist components, and the deprotection reaction interface over nanometer distances; (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process; (5) the polymer physics of the developer solution and the dissolution process; and (6) influence of moisture on the thermo-physical properties of interfaces as applicable to immersion lithography. These data are needed to meet the future lithographic requirements of sub 50 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility for development in an aqueous base solution. These reaction-diffusion and development processes must be understood and controlled at the nanometer length scale to fabricate integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 50 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 50 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths, 193 nm or extreme-ultraviolet (EUV), require photoresist films nearing 100 nm thickness to ensure optical transparency and uniform illumination. In these ultrathin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, component distribution, or transport properties. Furthermore, the required resolution for a sub 50 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these photoresist films. Additionally, the material sources of fea-

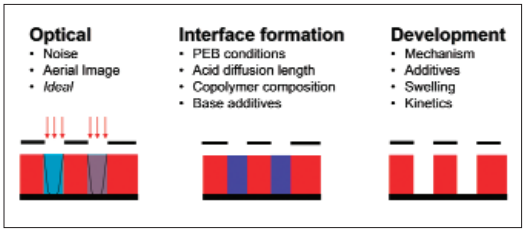

Figure 1. Key lithographic process steps studied for materials fundamentals.

Technical Contacts:
V. M. Prabhu
E. K. Lin
W. L. Wu

"[This team has] made seminal contributions to the field of lithography in elucidating the effects that contribute to line edge roughness using the unique technical capabilities and know-how of NIST. Their successful cooperation with industry partners and research organizations has been both scientifically outstanding as well as a model of how to implement such joint research efforts."

Mordechai Rothschild,
Massachusetts Institute
of Technology's
Lincoln Laboratory

"[This team has] made ground breaking contributions to the fundamental understanding of resist line edge roughness —a technological bottleneck that threatens to derail the continuing miniaturization of the semiconductor devices."

Qinghuang Lin, IBM

"… I just finished a presentation for AMD on your work. Every time I look at it, the framework that has been established seems more and more valuable for future work. … AMD is a huge proponent of what you have done."

Karen Turnquest, AMD, SEMATECH, Lithography

ture resolution (line-edge roughness (LER) and line-width roughness (LWR)) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the 2007 International Technology Roadmaps for Semiconductors on page 10, Lithography Section. Table LITH2 on "Lithography Difficult Challenges" for resist materials at < 32 nm indicates three issues (1) Resist and antireflective coating materials composed of alternatives to PFAS compounds, (2) Limits of chemically amplified resist sensitivity for < 32 nm half-pitch due to acid diffusion length, and (3) materials with improved dimensional and LWR control.

Technical Strategy

In this project, we use model photoresist materials to validate the new measurement methods. Model photoresist materials (applicable to 193 nm and EUV lithography) have been used to address several important fundamental questions including the thermal properties of ultra-thin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultra-thin films, the surface concentration of PAGs, the diffusion and the deprotection reaction kinetics, and the physics of the development process. These results provide a basis for understanding the material property changes that may effect the development of lithography for sub-50 nm structures using thin photoresist imaging layers. The interaction between model photoresists and BARC materials also requires detailed experimental investigation to optimize the materials factors impacting lithographic performance. Each process step requires an interdisciplinary array of experimental techniques to measure the polymer chemistry and physics in thin films as shown in Fig. 1.

DELIVERABLES:

- Develop reaction kinetics models to analyze experimental data for model and commercial EUV photoresists as a function of dose, PEB time, and component concentration. 1Q2008
- Publish the effect of salt valence on the spatial extent of the residual swelling fraction by neutron reflectivity. 3Q 2008
- Develop polarization-modulation infrared reflectance absorption spectroscopy for photoresist characterization. 2Q2008
- Publish methods to analyze the depth profiling of deprotection by variable-angle spectroscopic ellipsometry (IR-VASE). 2Q2008
- Assess development effects on LER using the EUV exposure tool at the Advanced Light Source, Lawrence Berkeley National Laboratory. 2Q2008
- Characterize latent image by AFM and CD SEM data and correlate to LER. 4Q2008
- Advance solid state NMR characterization of photoresist/photoacid generator dispersion to thin films using unique substrates. 2Q2008
- Determine molecular glass / photoacid generator dispersion extent by solid state NMR. 4Q2008

Accomplishments

■ EUV photoresist polymers are expected for imaging at the 22 nm node and smaller, however, resists are challenged to meet simultaneously resolution, dose sensitivity, and LER requirements. Similar to 193 nm (dry and immersion) lithography, the deprotection reaction front profile at the interface between exposed and unexposed resist is a critical factor. However, EUV photoresists in particular use high PAG loading and expect to use lower EUV doses. The effect of architecture or "pixel size" may also play a crucial role to achieve higher fidelity imaging. The fundamentals of critical additives, such as photodegradable bases, photoacid generator (PAG) structure, and contrasting architecture, shown in Fig. 2, are investigated.

■ The deprotection reaction front profile was measured with nanometer resolution by combining neutron reflectivity and Fourier transform infrared (FTIR) spectroscopy on a bilayer structure that mimics the lithographic line-edge (Fig. 3) prepared with model EUV and 193 nm photoresists. The upper layer of the structure is loaded with the photoacid generator. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group partially leaves the film, quantified by FTIR, upon reaction. The contrast to neutrons results from the reaction allowing for measurement of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales. We find that the reaction front broadens with

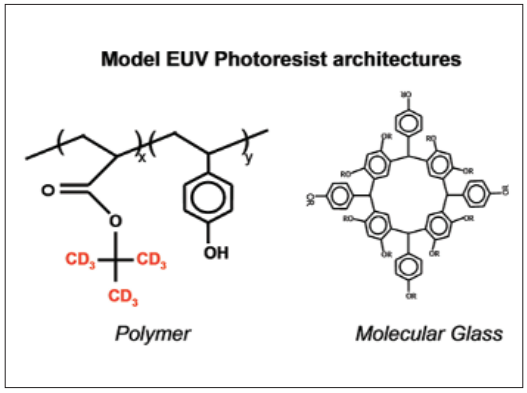

Figure 2. Two contrasting architectures of photoresist materials, but with similar chemistry: molecular glass and polymeric chemically amplified resist.

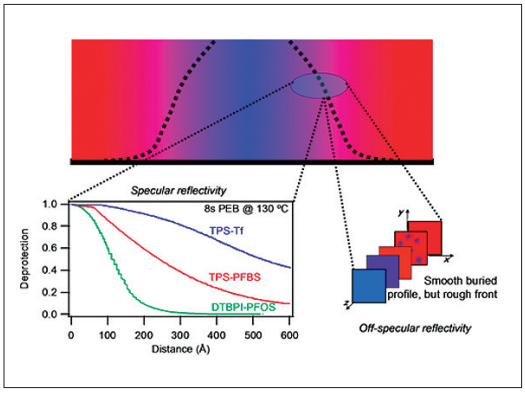

Figure 3. Specular neutron reflectivity results of the nanometer scale deprotection profile shape dependence on photoacid generator size: TPS-Tf < TPS-PFBS < DTBPI-PFOS; Highlight of the buried chemical heterogeneity measured at the reaction-front by off-specular reflectivity. These high-resolution experimental data help verify current advanced reaction-diffusion models.

time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that the reaction front width is dependent upon resist chemistry and PAG size as shown in Fig. 3. Neutron reflectivity was demonstrated to have sufficient chemical sensitivity and spatial resolution to measure the interfacial structure on sub-nm length scales.

■ A combination of specular and off-specular neutron reflectivity was used to measure the buried lateral roughness of the reaction-diffusion front in a model EUV photoresist. Compositional heterogeneities at the latent reaction-diffusion front have been proposed as a major cause of LER in photolithographic features. We measured the longitudinal and lateral compositional heterogeneities of a latent image, revealing the buried lateral length scale as well as the amplitude of inhomogeneity at the reaction-diffusion front. These measurements aid in determining the origins of LER formation, while exploring the material limits of the current chemically amplified photoresists. These unique measurement methods aide in determining the specific influence of photoresist components, resist chemistry, and the reaction-diffusion process.

■ In addition to applying depth profiling methods, the kinetics of the deprotection reaction was studied as a function of copolymer composition with FTIR spectroscopy. Three methacrylate-based terpolymers with varying compositions of acid-labile and non-reactive (lactone) monomers were studied. A mathematical model was developed to analyze the acid catalyzed deprotection kinetics with respect to coupled reaction rate and acid-diffusion processes. The first order reaction rate constant decreases as the non-reactive comonomer content is increased. Additionally, the extent of reaction appears self-limiting as verified by a slowing down necessitating an acid-trapping chemical equation to model the data. An example is shown in Fig. 4 (next page). This composition-dependent reaction constant indicates a strong interaction of the acid with the increasing polar resist matrix that drastically reduces the acid transport rate. The reduced acid transport is consistent with hydrogen bonding between photoacid and methacrylic acid product. These results demonstrate a correlation between polymer microstructure and acid catalyzed kinetics. These are necessary measurements for analysis of coupled reaction-diffusion processes. Finally, the models were applied to understand the limiting spatial extent of photoacid diffusion at the model line edge determined by neutron reflectivity. These measurement methods have been successfully applied to commercial EUV photoresist materials to predict the acid diffusion length.

■ The chemical latent image determines the nanoscale regions of resist that are soluble in the aqueous base developer solution that produces the final pattern. As these feature dimensions approach sub-32 nm, however, a possible trade-off among process variables may limit photoresists from achieving less than 2 nm LWR design criteria. A central assumption in these resolution limit models is a direct transfer of the chemical latent

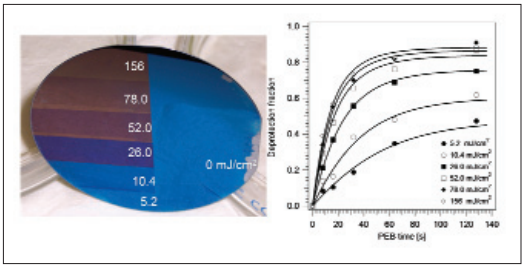

Figure 4. Wafer after exposure to varied DUV dose and fixed baking time. The color change represents slight changes in film thickness with extent of reaction. Quantification of the extent of reaction (deprotection fraction) versus post-exposure bake time for model 193 nm resist for varying dose.

image heterogeneity on the feature quality. Insight into the mechanism of development, rinse, and drying at a gradient line edge was achieved by neutron reflectivity with nm resolution. Direct measurements of the highly swollen photoresist polymer, deuterium labeled developer (d-TMA+) and aqueous solvent profiles at the developed line-edge clearly highlights a residual swelling fraction with spatial dimensions that exceed the radius of gyration (Rg) of the photoresist polymer (Fig.5).

■ The final surface roughness is formed by the collapse of this highly associated phase during the drying process. However, an ideal collapse and complete elimination of surface roughness was not observed in agreement with lithographic studies. A mechanism of a simple transfer of roughness from the latent image to the developed image is challenged by these data. Future simulations and models should include both percolation and penetration of developer and an associative polymer behavior due to the heterogeneity and large chemical mismatch of resist components. Extending these concepts to previous latent image analysis imply the minimization of the residual fraction provides the lowest roughness. This can be achieved through resist and optical design to provide the highest latent image profile slope. Quartz crystal microbalance measurements, a transferable measurement method, provides an added capability to measure the kinetics of swelling and collapse, however, the profile and chemical specificity are exclusively obtained with NR.

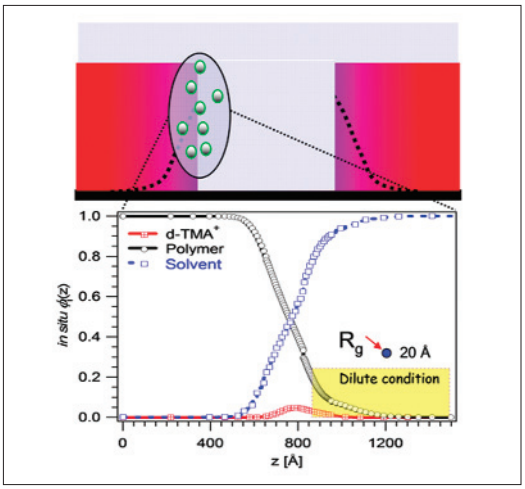

Figure 5. Neutron reflectivity results of the in situ composition profiles of resist, developer ions, and solvent at the model line-edge highlighting a residual swelling fraction.

■ NEXAFS measurements were used to measure the surface concentration and depth profile of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment. The instrument located at Brookhaven National Laboratory beamline U7A as shown in Fig. 6. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge X-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer chemistry and PAG size. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport and interactions enable detailed analysis of potential mechanisms leading to loss of profile control. UV exposure, post-exposure bake, and a novel atmosphere controlled chamber have been developed to test environmental stability against model airborne contaminants and influence on in situ processing.

■ NEXAFS measurements were used to measure the surface concentration and depth profile of

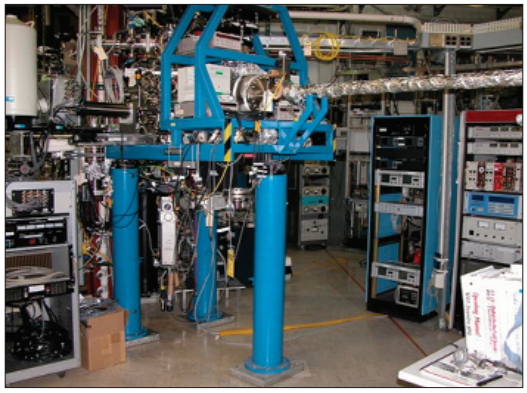

Figure 6. NEXAFS instrument at the U7A beam line, Brookhaven National Laboratory, National Synchrotron Light Source. Image courtesy of Dr. Daniel Fischer

photoacid generators for advanced 193 nm photoresist materials for immersion lithography. These measurements quantify the influence of water immersion on surface composition and loss of these critical components. NEXAFS on-wafer analysis combined with liquid chromatography/mass spectrometry (LC/MS) demonstrate that equilibrium water solubility of photoacid generators with varying perfluoroalkyl length does not serve as the appropriate selection criteria for immersion lithography; rather the segregation of photoacid generators to the top few nanometers provides the majority of leaching as shown in Fig. 7. Additionally, the effects of critical top coats are also investigated to understand the segregation and retention of additives.

■ Characterization of local bulk scale mixing is necessary for understanding future photoresist materials as feature dimensions are reduced to sub-32 nm. The intimacy of mixing of PAG and model polymer and molecular glass photoresist was probed by solid state proton NMR methods based on inversion-recovery, solid-echo-spin-diffusion, and chemical-shift-based-spin-diffusion pulse sequences. The effect of resist architecture for EUV lithography was investigated as a function of molecular glass core structures (see Fig. 8). The PAG miscibility in several protected and deprotected versions has been discovered with these new classes of resist materials. Phase separation of the PAG into enriched-domains was never seen; the PAG was always finely distributed. A maximum diameter for any PAG clustered into spherical domains was estimated to be 3.8 nm, which is too small to reflect thermodynamic incompatibility as the driving force during relatively slow removal of solvent. Hence, PAG blended samples are deduced to be thermodynamically compatible, with differential solubility in the preparation solvent the most likely candidate for producing the significant inhomogeneities in PAG concentration observed in a few samples. For one of the unprotected crystalline calix[4]resorcinarene materials, N-methyl 2-pyrrolidinone formed a solid adduct with a 1:1 molecular ratio. Only the unprotected materials display crystallinity implying that the mixing of the PAG with any protected MG is not restricted by crystallization before the post-exposure bake step. Lastly, very strong hydrogen bonds exist in unprotected materials which is reduced or eliminated upon partial protection with t-BOC.

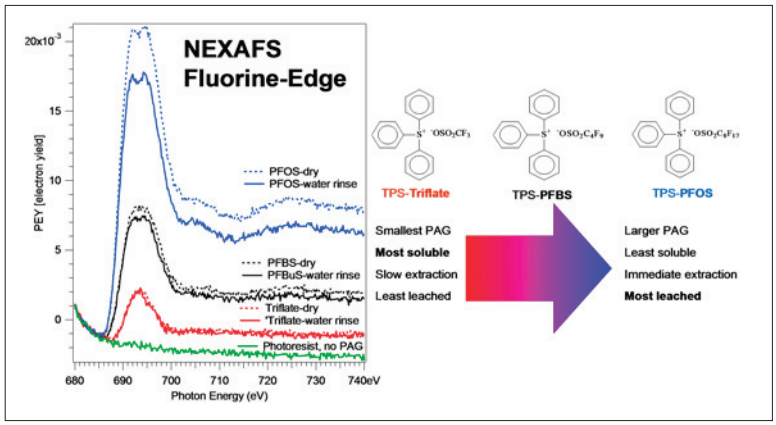

Figure 7. NEXAFS fluorine-edge results that quantify the PAG leaching from the surface due to water immersion. The series of PAGs tested for immersion lithography is shown as a function of equilibrium water solubility, extraction from thin films, and NEXAFS surface composition analysis.

■ Current EUV photoresist materials do not yet meet requirements on exposure-dose sensitivity, line-width roughness, and resolution. Fundamental studies are required to quantify the trade-offs in materials properties and processing steps for EUV photoresist-specific problems such as high photoacid generator loadings and the use of very thin films. Furthermore, new processing strategies such as changes in the developer strength and composition may enable increased resolution. In this work, model photoresists are formulated without base quenchers are

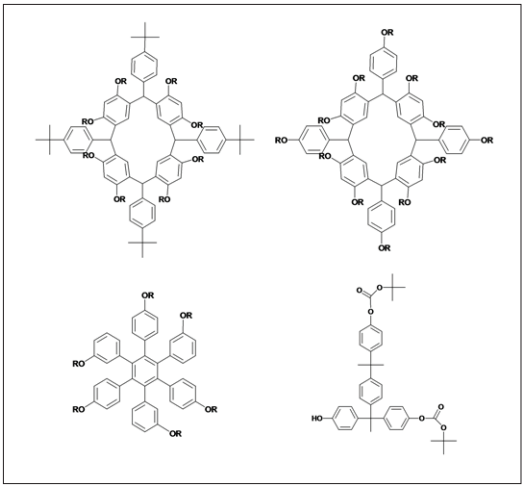

Figure 8. Model molecular glass with three different core architectures studied for intimacy of PAG mixing by NMR methods.

used to investigate the influence of photoacid generator loading and developer strength on EUV lithographically printed images performed at the Advanced Light Source of Lawrence Berkeley National Laboratory. Measurements of line-width roughness (LWR) and developed line-space patterns highlight a combined PAG loading and developer strength dependence that reduce LWR in a non-optimized photoresist.

■ Further, in collaboration with the Optical Technology Division, we have investigations of correlations between the latent image and developed image in EUV exposed line/space features. The latent images of isolated lines produced by EUV lithography are characterized by atomic force microscopy through the features in topology caused by change in film thickness that occurs upon deprotection. The resulting latent-image deprotection gradient (DGL), based on line cross-sections, and latent-image linewidth roughness (LWRL) provide metrics and insight into ways to optimize the lithographic process. The results from a model poly(hydroxystyrene-co-tert-butylacrylate) resist and a model calix[4]resorcinarene molecular glass type resist show the general applicability of the metric before development as shown in Fig. 9.

Collaborations

Polymers Division, NIST – Shuhui Kang, Kristopher Lavery, David VanderHart, Christopher Soles

Intel – Kwang-Woo Choi (Assignee to NIST), George Thompson, Michael Leeson, Todd Younkin

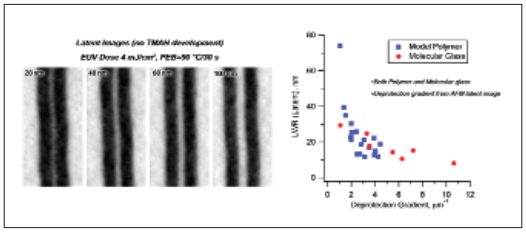

Figure 9. AFM latent images after tip deconvolution of dark field isolated lines in the model polymer resist. Nominal critical dimension appears in each image. While all lines are resolved in the latent image, only the 60 nm and wider lines remain after development at this dose: EUV exposure of 4 mJ/cm2 and PEB was 90 °C for 30 s. Images are 1 micron by 2 microns with a 20 nm black to white z-scale. Analysis of the latent-image LWR versus deprotection gradient for contrasting resists.

Ceramics Division, NIST – Daniel A. Fischer

Center for Neutron Research, NIST – Sushil K. Satija

Optical Technology Division, NIST – John Woodward

Cornell University – Christopher Ober

SEMATECH – Karen Turnquest

IBM Almaden Research Center – Hiroshi Ito, Robert D. Allen, William D. Hinsberg

AZ Electronics – Ralph Dammel, Frank Houlihan

DuPont Electronic Polymers L.P. – Jim Sounik, Michael T. Sheehan

Intel – CRADA 1893 (Polymers Division) and CRADA 1892 (Optical Technology Division)

SEMATECH – Agreement 309841 OF (completed 11/06)

Publications

D.L. VanderHart, A. De Silva, N. Felix, V.M. Prabhu, and C.K. Ober, *"The effect of EUV molecular glass architecture on the bulk dispersion of a photo-acid generator"* Proc. SPIE 6923, 69231M (2008).

K. A. Lavery, V.M.Prabhu, E.K. Lin, W.-l. Wu, S.K. Satija, K.-W. Choi, and M. Wormington. *"Lateral length scales of latent image roughness as determined by off-specular neutron reflectivity*" Applied Physics Letters, 92(1)064106(2008).

S. Kang, K. Lavery, K.-W. Choi, V.M. Prabhu, W.-l. Wu, E.K. Lin, A. De Silva, N. Felix, and C. Ober, *"A comparison*

of the reaction-diffusion kinetics between model-EUV polymer and molecular-glass photoresists" Proc. SPIE 6923, 692317 (2008).

J.T. Woodward, K.-W. Choi, V.M. Prabhu, S. Kang, K.L. Lavery, W.-l. Wu, M. Leeson, A. De Silva, N.M. Felix, and C.K. Ober, *"Characterization of the latent image to developed image in model EUV photoresists,"* Proc. SPIE 6923, 69232B (2008).

S. Kang, W.-l. Wu, V.M. Prabhu, B.D. Vogt, E.K. Lin, K. Turnquest, *"Evaluation of the 3D compositional heterogeneity effect on line-edge-roughness,"* Proc. SPIE, 6519, 65193V (2007).

K.-W. Choi, V. M. Prabhu, K. Lavery, E. K. Lin, W.-l. Wu, J. T. Woodward, M. J. Leeson, H. B. Cao, M. Chandhok, G. Thompson, *"Effect of photoacid generator concentration and developer strength on the patterning capabilities of a model EUV photoresist,"* Proc. of SPIE, 6519, 651943 (2007).

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B. D. Vogt, S.Kang, V. M. Prabhu, A. Rao, E. K. Lin, W.-l. Wu, S. K. Satija, and K. Turnquest, *"Influence of base additives on the reaction diffusion front of model chemically amplified photoresists,"* Journal of Vacuum Science and Technology B, 25,175-182 (2007).

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B. D. Vogt, S. Kang, V. M. Prabhu, E. K. Lin, S. K. Satija, K. Turnquest, and W. Wu, *"Measurements of the reaction-diffusion front of model chemically amplified photoresists with varying photoacid size,"* Macromolecules 39, 8311-8317 (2006).

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V. M. Prabhu, S. Sambasivan, D. A. Fischer, L. Sundberg, and R. D. Allen, *"Quantitative depth profiling of photoacid generators in photoresist materials by near-edge X-ray absorption fine structure spectroscopy,"* Applied Surface Science 253(2), 1010-1014 (2006).

Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, critical dimension and overlay measurement improvements have barely kept up with lithography capabilities. To maintain cost effectiveness, continued advances need to be made.

Wafer-level And Mask Critical Dimension Metrology

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason, the project is presented in a number of sub-sections, each focusing on a single technology.

These are:

- Model-Based Linewidth Metrology
- Scanning Electron and Ion-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Optical-Based Photomask Dimensional Metrology
- Scatterometry-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Grazing Incident X-Ray Scattering-Based Dimensional Metrology
- Atom-Based Dimensional Metrology
- Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Model-Based Linewidth Metrology

Technical Contacts:
J. Villarrubia

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth and line edge roughness metrology with uncertainties on the order of 1 nm as required by the industry roadmap.

Customer Needs

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, with worldwide sales of $255.6 billion in 2007 [Semiconductor Industry Association projection, Feb. 1, 2008]. As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with linewidth or CMOS gate leng.

To support present and future semiconductor technologies, industry needs to measure gate electrode widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of approximately 1 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level. In addition to measuring linewidths, the semiconductor industry has needs for measuring linewidth variation, that is, linewidth roughness (LWR). LWR in transistor gates has been linked to increased off-state leakage current and to threshold voltage variation. The 2007 ITRS specifies that LWR, measured as three standard deviations of the CD, must be less than 1.8 nm in 2008 and be measured with better than 0.4 nm uncertainty.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, divergence of inadequately quantified methods, and ignorance of best measurement practices. Barriers to accurate LWR measurement include random errors due to noise or sampling and poorly understood measurement artifacts such as measurement bias that comes from treating random edge assignment errors as a component of roughness (a false "noise roughness").

Technical Strategy

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have developed a model-based library method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works by describing edge geometry with a set of parameters (e.g., sidewall angle, corner radius, edge positions). The expected images for a range of parameter choices are calculated using a Monte Carlo algorithm (called JMONSEL) that simulates electron trajectories. The resulting actual shape/calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match (Fig.

"Stack materials, surface condition, line shape, and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD SEM measurements."

International Technology Roadmap for Semiconductors, Metrology Section, p. 10 (2007)

"A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2007)

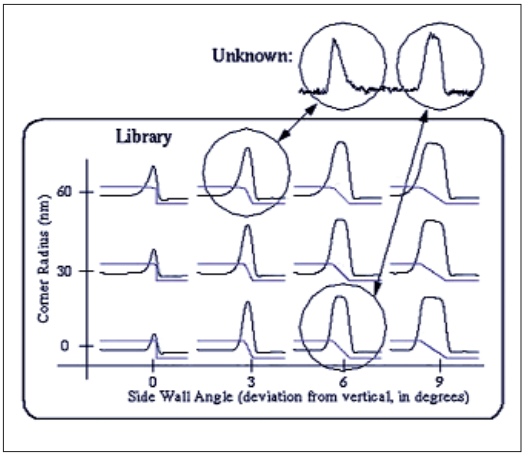

Figure. 1. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

1). The corresponding line shape is assigned to the unknown. In practice there may be more than two parameters, and the library is interpolated.

We have reported encouraging results for this method in recent years. These prior results establish a direct link between the quality of SEM models and the accuracy of metrology that can be performed using them. This has brought renewed focus on the quality of the models. Our original MONSEL model was restricted to samples that fell within well-defined and restricted classes, for example lines of uniform cross section on a layered substrate. Many samples of industrial interest did not comply with these restrictions. In 2007, we translated MONSEL to Java (renaming it JMONSEL), and substantially revised the method of geometrical descriptions, thereby extending the capabilities to permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, lines with a footing, and FinFETs (e.g., see Fig. 2).

DELIVERABLES:

- Complete implementation in JMONSEL of a scattering model that extends Mott inelastic scattering to the case of moving target electrons. 4Q 2007
- Develop a secondary electron generation model based upon the many-body dielectric theory of David Penn. 2Q 2008
- Implement the many-body model in JMONSEL. 3Q 2008

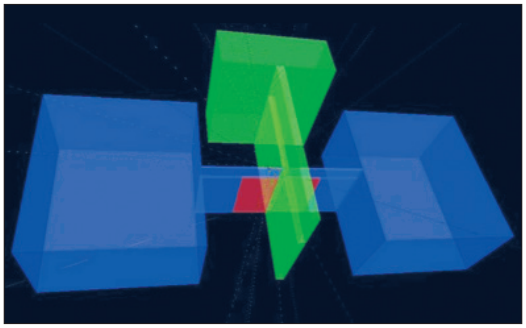

Figure. 2. An overview of a FinFET model showing Si source and drain (left and right boxes), a thin connecting Si fin with HfO_2 gate oxide, and a metal (TiN) gate electrode with a crossing fin-like contact. The substrate (not shown, but coincident with the bottom of the pictured structures) is Si.

- Run test simulations of the new models. Compare results to NIST Standard Reference Database 71 (Electron Inelastic Mean Free Path) and other available measurement data. 3Q 2008

In Atomic Force Microscopy (AFM) the issues with width determination are similar, and an analogous solution using models of the tip/sample interaction to reconstruct the sample shape is possible. We made considerable progress on this a number of years ago, developing a mathematical morphological description of the sample/probe interaction in terms of dilation, and of sample reconstruction in terms of erosion. These previous developments were limited to samples, images, and tips that could be described by single-valued surfaces (e.g., images in the form of grayscale height maps). Although dilation and erosion similarly described image formation and sample reconstruction for re-entrant surfaces (e.g., undercut lines) we were unable to perform calculations for such surfaces because of limitations in our software implementation. We recently overcame that limitation by development of a "dexel" (depth element) representation to replace the pixel representation for images of such objects. This permits image simulation and sample reconstruction even for reentrant samples or tips (Fig. 3). We continue the development this year, in collaboration with the Illinois Institute of Technology and Veeco Instruments, by extending the dexel method to "blind reconstruction." Blind reconstruction permits reconstruction of an outer bound on tip shapes from images of tip characterizer samples, the geometry of which need not be known in advance.

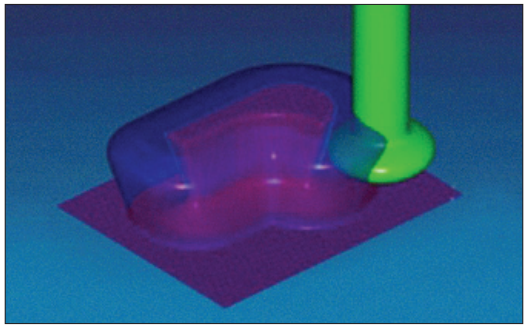

Figure. 3. "Dexels" are a representation for arbitrarily complex 3D structures that is also amenable to mathematical morphology operations like dilation and erosion, which are used to simulate the imaging process and to remove tip distortions from a measured image.

DELIVERABLES:

- Give an invited presentation on mathematical morphology techniques for dexel-represented objects at SCANNING 2008 meeting. 2Q 2008
- In collaboration with Prof. X. Qian, implement blind reconstruction for dexel-represented objects. 3Q 2008

Accomplishments

■ The 3-D Monte Carlo SEM simulator was completed and verified by comparison with the older simulator to produce the same results for samples within both their repertoires. This was in accord with the plan to extend sample geometry without initially changing the physics model employed by the simulator, in this way to verify that no unintended changes were accidentally introduced.

■ Following the above demonstration that no unintentional changes had been made to the models, improved physics models for barrier penetration and electron stopping power were introduced. We generalized Möller's theory of impact ionization, originally developed for the case of unbound electrons at rest, to the case when the target electron is moving.

■ The SEM work has generated considerable interest in semiconductor and nanotechnology applications areas, leading to an invited presentation at the SPIE Advanced Lithography Symposium and a colloquium at SUNY Albany's College of Nanoscale Science and Engineering.

■ We applied AFM image simulation and sample reconstruction methods for reentrant samples and tips to samples of industrial interest and reported these results at the SPIE Advanced Lithography Symposium.

Collaborations

International SEMATECH, Benjamin Bunday, Michael Bishop.

Hitachi, Ltd., Maki Tanaka.

Applied Materials, R. Katz, C. D. Chase, R. Kris, R. Peltinov.

Illinois Institute of Technology, Prof. Xiaoping Qian.

Intel Corp.

Recent Publications

X. Qian and J. S. Villarrubia, *"General Three-Dimensional Image Simulation and Surface Reconstruction in Scanning Probe Microscopy using a Dexel Representation,"* Ultramicroscopy, 2007.

J. S. Villarrubia, N. W. M. Ritchie, and J. R. Lowney, *"Monte Carlo modeling of secondary electron imaging in three dimensions,"* J. Proc. SPIE 6518 (2007).

X. Qian, J. S. Villarrubia, F. Tian, and R. Dixson, *"Image Simulation and Surface Reconstruction of Undercut Features in Atomic Force Microscopy,"* submitted to Proc. SPIE 6518 (February 2007).

R. L. Jones, C. Wang, E. K. Lin, W. Wu, J. S. Villarrubia, K. Choi, J. S. Clarke, and B. D. Bunday, *"Line-edge roughness and cross-sectional characterization of sub-50 nm structures using CD-SAXS,"* submitted to Proc. SPIE 6518 (February 2007).

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M. Tanaka, J. S. Villarrubia, and A. E. Vladár, *"Influence of Focus Variation on Linewidth Measurements,"* Proc. SPIE 5752, p. 144 (2005).

"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2007)

Scanning Electron and Ion-Based Dimensional Metrology

Technical Contacts:
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J. S. Villarrubia
M. T. Postek

"Scanning Electron Microscopy (SEM) – continues to provide at-line and in-line imaging … and CD measurements. Improvements are needed … at or beyond the 45 nm generation … Determination of the real 3-D shape…will require continuing advances in existing microscopy …"

International Technology Roadmap for Semiconductors, 2007

Goals

Provide the microelectronics industry with highly accurate scanning electron microscope (SEM) measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron and ion optical system, detection, sample stage, and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to addresskey metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors (2007) states that "Scanning Electron Microscopy continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and critical dimension (CD) measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 45 nm generation." The semiconductor industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research of the signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 65 nm or less with a very high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of the minimum feature size, known as CD, are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is key microscopic technique used for this sub-100 nm metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project, a multidimensional project, is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). Conventional optical lithography provides a chance for a large number of good quality samples to be produced inexpensively. Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm. In order to make this artifact available (while the final certification details are being completed)

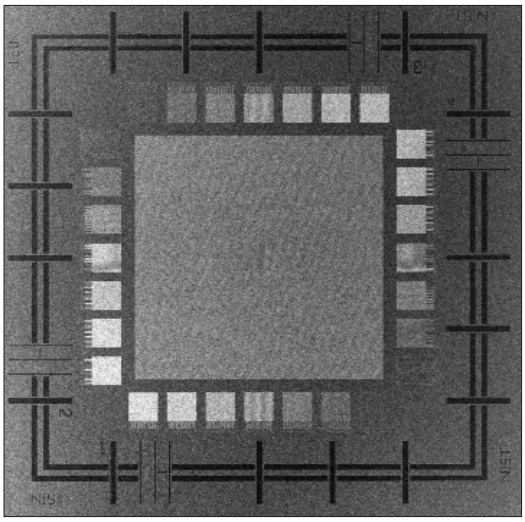

Figure 1. SEM image of the complete RM 8820 Magnification calibration standard reference material.

the artifact is now released as Reference Material (RM) 8820.

DELIVERABLES:

- Development of a new metrology SEM based on a variable pressure instrument. This instrument will be able to work with full size wafers and photomask. 4Q 2008
- Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples. 4Q 2008
- Upon availability of suitable quality samples, completion of calibration and delivery of a batch of SRM 2120 samples. 4Q 2008

2. SEM Performance Measurement Artifacts and Software Solutions: This effort included the development of the Reference Material 8091 (Fig. 2.) and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. Currently we are working with ISO to develop robust software solutions that will allow for resolution performance tracking of SEMs. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. As a part of this effort the NIST SEM Resolution Measurement Reference Image Set was worked out to test the resolution measurement software themselves. This Reference Image Set contains a large number of artificial images that were made by taking onto account the amount and type of defocusing, noise, vibration and drift and electron landing energies. Suitable samples are being sought to further improve this type of metrology (Fig. 3). Several samples have been purchased

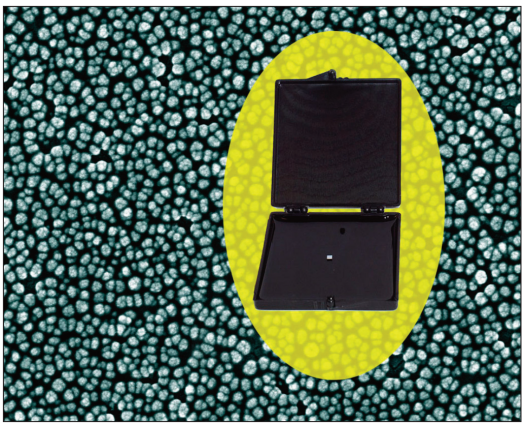

Figure 2. The RM 9081 Sharpness Reference Material.

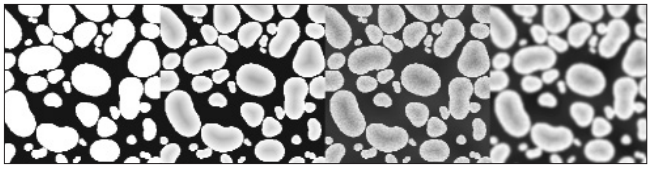

Figure 3. Images that illustrate the image simulation steps for the NIST SEM Resolution Measurement Reference Image Set.

by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were, and are, in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time, the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with a few nm of accuracy. In several publications, NIST demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 1 mm to down to 50 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

A new effort is underway that is aimed at the development of two new Reference SEMs. One with full-size wafer and mask capability is based on an environmental SEM (ESEM), which is very advantageous with samples that charge such as quartz masks. The other Reference instrument

based on a dual-beam SEM, and will be capable to work with mask- and smaller size samples. Both microscopes will use the same type of 38 pm resolution laser interferometry, which provides traceability and it allows for the compensation for stage drift and vibration at the nm level.

DELIVERABLES:

- Design and preparation of line width metrology immersion lithographic artifact suitable for calibration on NIST and external measuring systems for certification of wafer format line width samples. 3Q 2008
- Completion of preliminary measurements on immerse litho samples made by SEMATECH with the new "NISTMAG" metrology mask. 4Q 2008

4. Helium Ion Microscopy - a Promising New Technique for Semiconductor Metrology: The Helium Ion Microscope (HIM) offers a new, potentially disruptive technique for nanometrology. This methodology presents an approach to measurements for nanotechnology and nano-manufacturing which has several potential advantages over the traditional SEM currently in use in integrated circuit research and manufacturing facilities across the world. Due to the very small, essentially one atom size, very high brightness source, and the shorter wavelength of the helium ions, it is theoretically possible to focus the ion beam into a smaller probe size relative to that of an electron beam of current SEMs. Hence higher resolution is theoretically achievable. In contrast to the SEM, when the helium ion beam interacts with the sample, it generates significantly smaller excitation volume and thus the image collected is more surface sensitive. Similarly to the SEM, the HIM also produces topographic, material, crystallographic, and potential contrast, and offers ways for investigating new properties of the sample through the use of various detectors. Compared to an SEM, the secondary electron yield is quite high, allowing for imaging at very low beam currents, thus resulting in less sample damage. Additionally, due to the low mass of the helium ion, the He beam does not mill the sample at as high rate as gallium ions that are regularly used for ion milling, but with larger beam currents can be used for finer milling and cutting.

DELIVERABLES:

- Completion of measurements and quality assessment of the imaging capability of the HIM with immersion lithographic techniques amorphous Si litho samples made by SEMATECH and phase shifting photomasks. 4Q 2008

ACCOMPLISHMENTS

■ **SEM Magnification Calibration Artifacts** – Samples for Reference Material 8820 have been made in the past once successfully, but later several attempts with e-beam lithography yielded no further useful samples. We delivered to NIST Standart Reference Materials office 100 pieces of RM 8820, which were fabricated at International SEMATECH using 193 nm UV light lithography. The finest features are 100 nm wide with a 200 nm pitch. The largest pitch is 1500 µm. There are a large number of 250 nm wide crosses and grids for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from amorphous Si material. These samples give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. With the arrival of the new metrology SEM and its laser interferometer sample stage these will be calibrated.

■ **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). There have been 75 samples delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public, and many of them are already in use. There is a new ISO standard under development that is introducing a method to reliably measure the resolution performance of SEMs; this method is also working well with RM 8091 samples.

■ **Contamination Specification for Dimensional Metrology SEMs** – Electron beam-induced contamination is one of the most bothersome problems encountered in the use of the SEM. Even in "clean-vacuum" instruments it is possible that the image gradually darkens because a polymerized hydrocarbon layer with low secondary electron yield is deposited. This contamination layer can get so thick that it noticeably changes the size and

shape of the small structures of current and future state-of-the art integrated circuits (ICs). Contamination greatly disturbs or hinders the measurement process and the erroneous results can lead to wrong process control decisions. NIST has developed cleaning procedures and a contamination specification that offer an effective and viable solution for this problem. By the acceptance, implementation and regular use of these methods it is possible to get rid of electron beam induced contamination.

■ **SEM Linewidth Measurement Artifacts** – For correct linewidth measurements accurate modeling methods are indispensable. The exist-

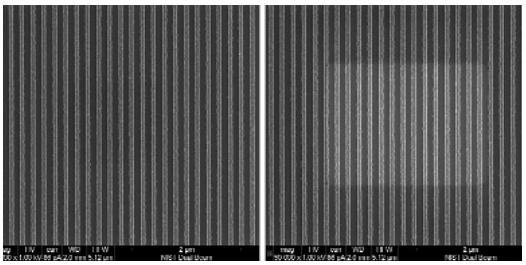

Figure 4. Contamination-free SEM operation. 1 kV, 86 pA SEM images of amorphous Si patterns at the beginning of the test (left) and after 10 minutes (left) of continuous electron beam bombardment. Actual cleaning and more signal are observable. There are 5 µm field-of-view images.

ing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view and using our high-accuracy modeling and fitting methods, a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for a linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation, and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of the SEMATECH/NIST mask have been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All of these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2008 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

■ **Development of High Accuracy Laser Interferometer Sample Stage for SEMs** – The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.04 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 5 illustrates the short-term motion of the sample stage, the left side of the figure depicts the location of the stage and the right side is the density distribution of the location of the stage during 1 minute of dwell time. The field-of-views are 2 nm for all images. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality. Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and the characterization of various settings and fine tuning of the sample stage, which is critical for high-resolution work.

■ **Development of Line Edge Roughness Metrology for Integrated Circuit Technology**

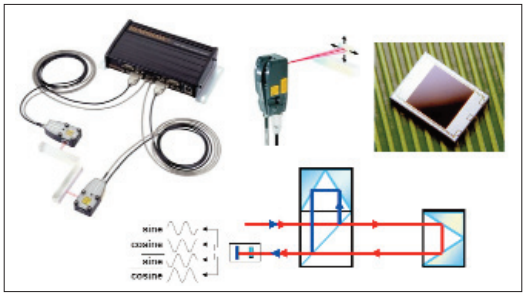

Figure 5. Laser interferometer system of the NIST Reference SEMs. Fiber-based beam delivery system (upper left corner) Differential interferometer (upper center) Phase sensitive detector (upper right) and the detection scheme (bottom). (Courtesy of Renishaw Plc.)

– The measurement of line-edge roughness (LER) has become an important topic in the metrology needed for the semiconductor industry. NIST has successfully developed various LER metrics and methods to make reliable and statically sound LER measurements. The findings have impact on the ITRS as they call for longer lengths for LER evaluation and on LER metrology in general because the new methods offer significantly better metrology than what was available previously. The final report of a year-long study was delivered on time to SEMATECH.

■ Development of Ultra-High Resolution He Ion Microscope – The HIM technology is not yet as optimized, developed or as mature as the SEM. As a new technique, HIM (Fig. 6) is just beginning to show promise and the plethora of potentially advantageous applications for integrated circuit and nanotechnology have yet to be exploited. Now that commercial instrumentation is available, further work can be done on the fundamental science of helium ion beam generation, helium ion beam-specimen interactions, and the signal generation and contrast mechanisms defining the image.

In addition to these areas of work, modeling needs to be developed to correctly interpret the signal generation mechanisms and to understand the imaging mechanisms. These are indispensable for accurate nanometer-level metrology. HIM and SEM have some overlapping territory, but they remain complementary techniques. Helium ion beam microscopy is forging into new scientific and technology territories, and this new and innovative technology will develop new science and contribute to the progress in integrated circuit and nanotechnology.

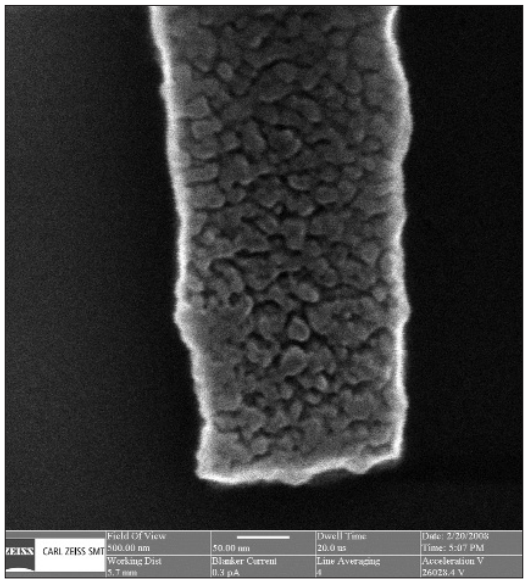

Figure 6. Alis/Zeiss He ion microscope image of a Cr on quartz photomask. 500 nm field-of-view.

Collaborations

International SEMATECH, Advanced Metrology Advisory Group.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

Zeiss/ALIS Corp.

FEI Co.

ISO.

E. Fjeld Co.

Recent Publications

A. E. Vladár, K. P. Purushotham and M. T. Postek *"Contamination Specification for Dimensional Metrology SEMs,"* SPIE Microlithography 2008.

M. T. Postek, A. E. Vladár *"The Potentials of Helium Ion Microscopy for Semiconductor Process Metrology,"* SPIE Microlithography 2008.

A. E. Vladár, J. S. Villarrubia, P. Cizmar, M. Oral and M. T. Postek *"Accurate and Traceable Dimensional Metrology with a Reference CD-SEM,"* SPIE Microlithography 2008.

M. T. Postek, A. E. Vladar, J. Kramar, W. Ward, L. A. Stern, J. Notte and S. McVey, *"Helium Ion Microscopy: a New Technique for Semiconductor Metrology and Nanotechnology,"* Scanning 2007.

M. T. Postek, A. E. Vladar, J. A. Kramar, L. A. Stern, J. Notte, S. McVey, *"The Helium Ion Microscope: A New Tool for Nanotechnology and Nanomanufacturing,"* SPIE 2007.

M. T. Postek, A. E. Vladar, J. A. Kramar, L. A. Stern, J. Notte, S. McVey, *"Helium Ion Microscopy: A New Technique for Semiconductor Metrology and Nanotechnology,"* International Conference on Frontiers of Characterization and Metrology for Nanoelectronics 2007.

Cizmar, A. E. Vladar, B. Ming, M. T. Postek, *"Simulated SEM Images for Resolution Measurement"* Scanning 2007.

Scanning Probe Microscope-Based Dimensional Metrology

Technical Contacts:
R. Dixson
G. Orji
J. Fu

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in scanning probe microscope-based measurements. *The International Technology Roadmap for Semiconductors* (ITRS) identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2007 update, the goal in 2008 for critical dimension (CD) measurement precision for isolated lines was ± 0.46 nm; this demand tightens to ± 0.27 nm by 2012.

Although most in-line metrology is performed using bySEM and scatterometry, these instruments are not presently capable of first-principles accuracy. That is, they must be calibrated using reference measurements from a tool or combination of tools which is capable of intrinsic accuracy. Such a tool is now referred to as a reference measurement system (RMS), and the 2007 update of the *ITRS* highlights the growing importance of an RMS. The use of AFM and TEM cross measurements section for this purpose – often in combination – is now a fairly common practice in the industry.

The technical focus of this project, development and implementation of scanning probe microscope instrumentation for traceable dimensional metrology, is thus driven by the anticipated industry needs for reduced measurement uncertainty for in-line metrology tools such as the SEM and scatterometer – since these in turn rely on reduced measurement uncertainty for techniques such as AFM that are often implemented as an RMS.

Customer Needs

The SEM is still the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. Scatterometry or optical critical dimension (OCD) metrology is also rapidly gaining acceptance as an in-line process metrology tool. Scanning probe microscopes (SPMs) possess unique capabilities, which may significantly enhance the performance of SEMs for in-line CD measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, the availability of traceable pitch, height, and width standards in this regime is limited.

Technical Strategy

The SPM dimensional metrology program consists of three inter-related thrusts: The first two thrusts address SPM dimensional metrology with two in-house research instruments at NIST, and the third thrust involves a partnership with SEMATECH to maintain traceability on a commercially available in-line SPM housed in the manufacturing facility at SEMATECH. The two instruments housed at NIST are a calibrated atomic force microscope (C-AFM) for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of line width.

The C-AFM is a custom built instrument that has metrology traceable to the wavelength of light for all three axes of motion, and it has provided calibrated pitch and height measurements for a variety of nano-scale applications. Pitch measurements in the micrometer regime and below can currently be performed with relative standard uncertainties as low as 5×10^{-4}, and step height measurements up to several hundred nanometers can be performed with a relative standard uncertainty approaching 1×10^{-3}. The C-AFM has participated in two international comparisons of sub-micrometer pitch measurements and one comparison of step height measurements.

DELIVERABLES:

- Compared CD-AFM reference metrology on trial photomask with electrical metrology developed at the University of Edinburgh – and coauthored a paper on the results for the international confer-

ence on microelectronic test structures ICMTS. 4Q2007 and 2Q 2008

- Presented paper on AFM metrology of photomasks at SPIE/BACUS conference on photomask technology. 4Q 2007
- Coauthored paper with IBM on use of SCCDRM to calibrated z-axis scale of a CD-AFM – presented at SPIE Advanced Lithography Meeting. 2Q 2008
- Organized, hosted, and ran an evening panel discussion on reference metrology. 2Q 2008
- Perform initial re-measurement of SRM 2059 photomask master standard using traceable CD-AFM at NIST. 3Q 2008
- Participate in joint NIST-SEMATECH workshop on OCD standards – in regard to traceability and AFM reference metrology – at SEMICON West. 3Q 2008
- Co-lead international comparison of photomask linewidth measurements (Nano 1) and perform CD-AFM reference measurements to support the project. 4Q 2008

The second and third thrusts involve the most commonly used AFM-based method of linewidth metrology in industry: CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. The SXM320 is a prior generation commercially available CD-AFM. Initially, this instrument was used to implement the CD-AFM/RMS at SEMATECH during the tenure of Ronald Dixson as the first NIST Guest Scientist there. Now that the instrument is housed at NIST, the uncertainties have been further refined. Currently, pitch measurements can be performed with a relative standard uncertainty of approximately 2×10^{-3}. Step height measurements have a relative standard uncertainty 4×10^{-3}, and linewidth measurements can have standard uncertainties as low as 1 nm. This is a result of the most current release of NIST single crystal critical dimension reference materials (SCCDRM) that was completed in 2005.

The third thrust involves collaboration with SEMATECH to maintain a traceable CD-AFM (RMS) in the manufacturing facility there. This thrust is currently overseen by George Orji who is now the second NIST Guest Scientist at SEMATECH. A current generation CD-AFM, the Veeco Dimension X3D, is now being used to implement the RMS. As is true for the SXM at NIST, the SCCDRM project has resulted in the ability to perform linewidth measurements with a standard uncertainty of 1 nm. The relative uncertainties in pitch and height measurements have been recently reduced to 1×10^{-3} and 2×10^{-3}, respectively.

DELIVERABLES:

- Presented a paper on the uncertainty of sidewall angle measurement using the CD-AFM/RMS at SEMATECH at SPIE Advanced Lithography Meeting. 2Q 2008
- Co-authored paper with SEMATECH on the use of the CD-AFM/RMS to improve accuracy and modeling of resist shrinkage under e-beam exposure during SEM inspection. 2Q 2008
- Complete a report on the refinements and extensions of the CD-AFM RMS for SEMATECH. 2Q 2008

Accomplishments

■ The NIST/SEMATECH partnership in advancing AFM metrology in semiconductor manufacturing continues. George Orji is now in the fourth year of his tenure as the second NIST Guest Scientist at SEMATECH, following a three year tenure of Ronald Dixson as the first NIST Guest Scientist. George has continued the NIST engagement with SEMATECH by supporting their SEM and scatterometer benchmarking activities with the RMS, and he has overseen the reduction of pitch and height uncertainties by approximately a factor of two.

■ We are collaborating with other NIST researchers and external partners such as SEMATECH, Intel, and IBM to develop linewidth

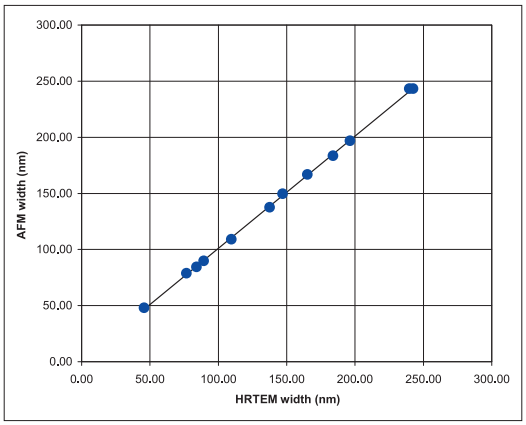

Figure 1. Regression of CD-AFM width values on HRTEM values. The observed slope is consistent with unity – indicating that the two methods have consistent scale calibration. The average offset between the results was used to provide the tip width calibration.

standards and CD reference metrology. A major component of this effort has been the single crystal critical dimension reference materials (SCCDRM) project initiated by NIST researchers in EEEL (Cresswell and Allen). In late 2004, we completed a release of SCCDRMs to SEMATECH and its member companies, and CD-AFM dimensional metrology played a central role. The measurements on the SCCDRM samples were performed by NIST scientist Ronald Dixson using the X3D at SEMATECH which had been implemented as a CD-AFM reference measurement system (RMS) for traceable measurements of pitch, height, and width. High resolution transmission electron microscopy (HRTEM) was used as an indirect method of tip width calibration for the SCCDRM samples. The AFM and HRTEM results that were used for the tip calibration are shown in Fig. 1. Features on the distributed samples ranged in width from approximately 50 nm to 250 nm with expanded uncertainties of about 2 nm ($k = 2$) on most features.

■ As a result of this project, CD-AFM linewidth measurements can now be performed with a 1 nm (k = 1) standard uncertainty. This standard for width calibration is now being used on both the X3D and the SXM at NIST. An image of an SCCDRM taken on the SXM320 is shown in Fig. 2. In 2005, we launched the "next generation" of the SCCDRM project and are currently performing a series of designed experiments to further improve the performance characteristics of the SCCDRMs – including linewidth uniformity. In the first phase of these experiments, we have observed feature widths as low as 20 nm with uniformity at the 1 nm level.

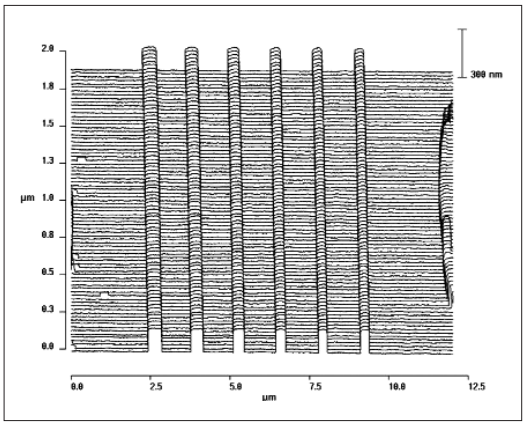

Figure 2. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration. Measurements performed by R. Dixson, sample developed by M. Cresswell and R. Allen.

■ We have used the C-AFM to participate in a series of International Supplementary Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of traceable measurements of dimensional quantities important to the semiconductor industry. We have previously participated in comparisons of step height and one dimensional pitch measurements. The results of these comparisons have now been published under the Mutual Recognition Arrangement (MRA) through which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. During 2005, we participated in a comparison of two dimensional pitch measurements: the C-AFM was used to measure both a 300 nm and 1000 nm grating. An example of a C-AFM image on the 1000 nm grating is shown in Fig. 3. A similar comparison of linewidth measurements is currently being planned and will be led by NIST.

■ Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2004 we developed a draft standard for AFM z-calibration using the single atom steps for the ASTM Subcommittee E42.14 on STM/AFM. This draft standard is still being revised and undergoing review within the subcommittee.

We are also developing a technique for AFM linewidth metrology based on image stitching. This involves the acquisition of paired images using a carbon nanotube probe. The nanotube tip enables data acquisition at high resolution on one

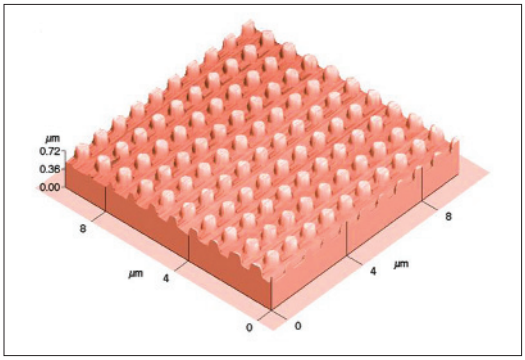

Figure 3. An image of a 1000 nm pitch grating array taken using the C-AFM as part of an international comparison of two dimensional pitch measurements.

side of the line in each image, and the specimen is rotated 180 degrees between the two measurements. Stitching these two images into a composite offers the potential of accurate linewidth metrology. We have completed two generations of an experiment in which the stitching result is compared with CD-AFM. The composite image used in one of our published comparisons between image stitching and CD-AFM is shown in Fig. 4. Currently, we are assessing the uncertainties and continuing to develop this approach.

■ We continue to refine the CD-AFM RMS at SEMATECH and bring its traceable measurement capabilities to bear on semiconductor manufacturing applications. During the tenure of both NIST Guest Scientists at SEMATECH, we have used this RMS system to provide reference metrology for both SEM and scatterometer benchmarking, measurements of SEM-induced shrinkage of 193 nm photoresist, and to provide reference metrology for evaluation of several new optical methods for measurement of photomasks.

■ In the SEM benchmarking applications, our basic methodology is to perform both CD-AFM and SEM measurements on a series of features on a focus exposure matrix that spans a process window. This approach means that both tools see features that have a range of widths as well as secondary characteristics such as sidewall angle and corner rounding. A regression of the AFM/SEM data allows the SEM to be checked for bias, scale calibration, and linearity of response across the FEM. An example of a SEM/AFM regression using measurements of isolated polysilicon lines is shown in Fig. 5. SEMATECH and its members place high value on SEMATECH's tool benchmarking activities and the support these activities receive from the NIST-supported CD-AFM RMS.

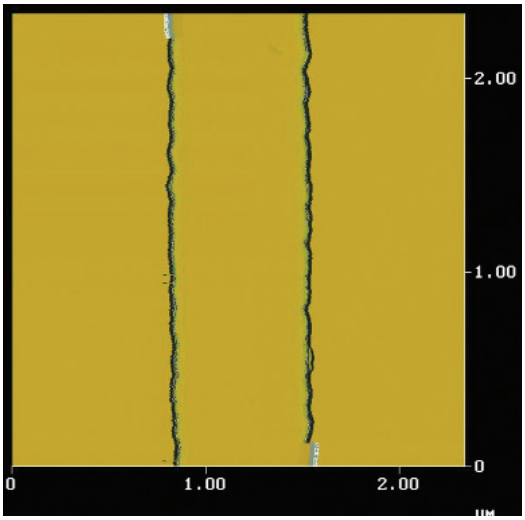

Figure 4. Stitched composite slope image from two images of a linewidth sample taken with a carbon nanotube tip. Measurements performed by J. Fu; sample developed by M. Cresswell and R. Allen; probe developed by C. Nguyen of ELORET/NASA Ames.

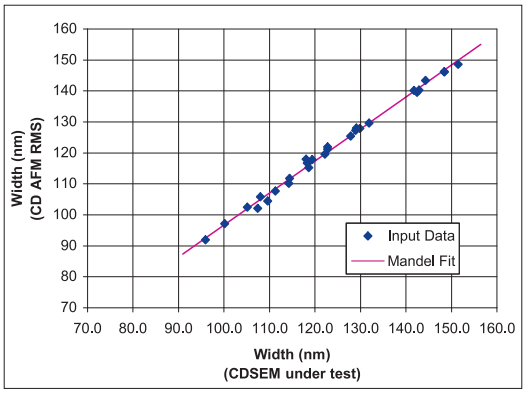

Figure 5. An example of an AFM/SEM regression performed as part of a SEMATECH benchmarking activity during the tenure of Ronald Dixson as the first NIST Guest Scientist at SEMATECH. The measurements were performed on isolated etched polysilicon lines that spanned a wide process-window focus-exposure matrix. The Mandel regression allows for uncertainty in both variables and is the most appropriate way to compare a tool under test with the reference measurement system. In this example, the SEM performance is very good and exhibits a bias of only 3 nm and linearity within the uncertainties of the comparison.

Collaborations

Intel Mask Operations, Santa Clara, CA.

Intel, Hilllsboro, OR.

Intel, Santa Clara, CA.

SEMATECH, Austin, TX.

Veeco Metrology, Santa Barbara, CA.

IBM Burlington, VT.

IBM Almaden Research Center, San Jose, CA.

ELORET Corp./NASA Ames Research Center, Moffett Field, CA.

Departments of Mechanical Engineering and Chemistry, University of North Carolina, Charlotte, NC.

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China.

Recent Publications

J. Robert, B. Banke, R. Dixson, C. Strocchia-Rivera, *"Traceable Calibration of AFM Step Height Measurements for Integrated Circuit Manufacturing,"* SPIE Proceedings Vol. 6922 (2008).

N. G. Orji, R. G. Dixson, B. D. Bunday, J. A. Allgair, *"Towards Accurate Feature Shape Metrology,"* SPIE Proceedings Vol. 6922 (2008).

R. M. Silver, B. Barnes, A. Heckert, R. Attota, R. G. Dixson, J. Jun, *"Angle Resolved Optical Metrology,"* SPIE Proceedings Vol. 6922 (2008).

R. Attota, R. Silver, R. Dixson, *"Linewidth measurement technique using through-focus optical images,"* Applied Optics Vol. 47, 495-503 (2008).

H. J. Patrick, R. Attota, B. Barnes, T. A. Germer, R. G. Dixson, M. T. Stocker, R. M. Silver, M. R. Bishop, *"Optical critical dimension measurement of silicon grating targets using back focal plane scatterfield microscopy,"* J. Micro/Nanolith. MEMS MOEMS Vol. 7, 013012-1-11 (2008).

M. W. Cresswell, R. A. Allen, W. F. Guthrie, C. E. Murabito, R. G. Dixson, A. Hunt, *"Comparison of SEM and HRTEM CD Measurements Extracted from Test-Structures Having Feature Linewidths from 40 nm to 240 nm,"* IEEE Trans. Instrum. Meas. Vol. 57, 100-109 (2008).

Ronald Dixson, Ndubuisi G. Orji, James Potzick, Joseph Fu, Richard A. Allen, Michael Cresswell, Stewart Smith, Anthony J. Walton, Andreas Tsiamis, *"Photomask Applications of Traceable Atomic Force Microscope Dimensional Metrology at NIST,"* SPIE Proceedings Vol. 6730, 67303D-1-13 (2007).

N. G. Orji, R. G. Dixson, *"Higher Order Tip Effects in Traceable CD-AFM Based Linewidth Measurements,"* Meas. Sci. and Technol. Vol. 18, 448-455 (2007).

N. G. Orji, R. Dixson, B. D. Bunday, J. A. Allgair, *"TEM Calibration Methods for Critical Dimension Standards,"* SPIE Proceedings Vol. 6518, 651810 (2007).

B. Bunday, J. Allgair, E. Soleck, C. Archie, N. G. Orji, J. Beach, O. Adan, R. Peltinov, M. Bar-zvi, J. Swyers, "*The coming of age of tilt CD-SEM,"* SPIE Proceedings Vol. 6518, 65181S (2007).

R. Dixson and N. G. Orji, *"Comparison and uncertainties of standards for critical dimension atomic force microscope tip width calibration,"* SPIE Proceedings Vol. 6518, 651816 (2007).

R. Dixson, W. F. Guthrie, M. W. Cresswell, R. A. Allen, Ndubuisi G. Orji, *"Single crystal critical dimension reference materials (SCCDRM): process optimization for the next generation of standards,"* SPIE Proceedings Vol. 6518, 651815 (2007).

B. C. Park, J. Choi, S. J. Ahn, D-H Kim, J. Lyou, R. Dixson, N. G. Orji, J. Fu, T. V. Vorburger, *"Application of carbon nanotube probes in a critical dimension atomic force microscope,"* SPIE Proceedings Vol. 6518, 651819 (2007).

R. Dixson, N.G. Orji, J. Fu, M. Cresswell, R. Allen, W. Guthrie, *"Traceable Atomic Force Microscope Dimensional Metrology at NIST,"* SPIE Proceedings Vol. 6152, 61520P-1-11 (2006).

N. Orji, A. Martinez, R. Dixson, J. Allgair, *"Progress on Implementation of a CD-AFM based Reference Measurement System,"* SPIE Proceedings Vol. 6152, 61520O-1-12 (2006).

Optical-Based Photomask Dimensional Metrology

Technical Contacts:
Y. Li

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements.

Accurate feature size metrology on binary photomasks (constituting 85% of current mask production) becomes increasingly difficult as critical features shrink and their optical proximity correction cousins proliferate. Phase shift and EUV masks present additional challenges.

Improved photomask CD metrology and two-dimensional overlay measurement techniques and standards are needed for measuring and controlling feature size and placement on the wafer and on the photomasks. Overlay control is listed in multiple sections of Tables Met 3a and b of the 2007 SIA ITRS as a difficult challenge for <45 nm node processes. In fact, the table shows that there are no known measurement solutions with acceptable uncertainty for image placement and overlay control beyond the 65 nm node. As shown in Tables *MET4a* and *b*, the problems are more acute for long term photomask CD metrology where the industry will soon be encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are two main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to provide photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. NIST's current chrome-on-quartz photomask linewidth standard, SRM 2059, (Fig. 2, next page) contains isolated linewidth and spacewidth features in the range of 0.25 µm to 32 µm, whose widths have been measured and certified to an uncertainty of ≈20 nm at the 95% confidence level.

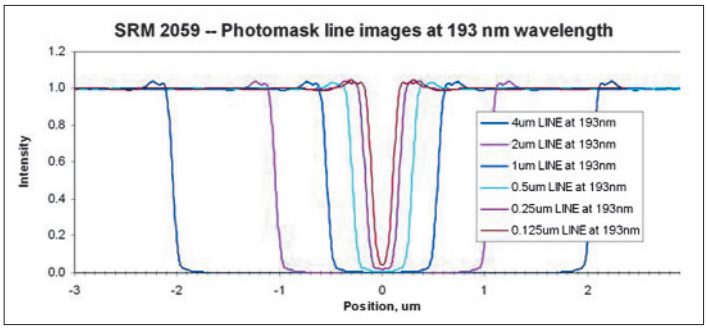

Figure 1. Modeling results for isolated binary photomask lines from 4µm to 0.125µm.

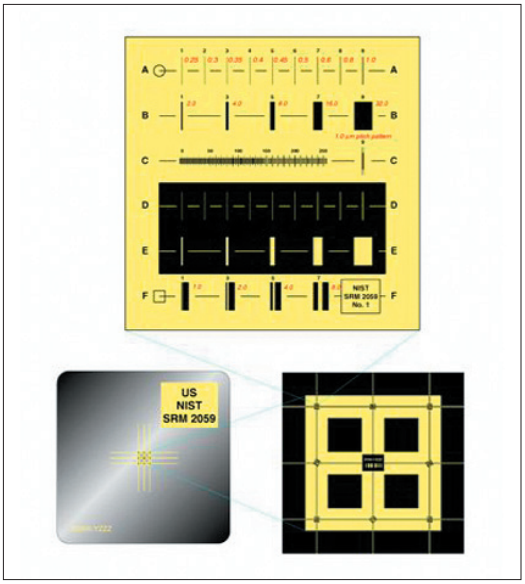

Figure 2. NIST SRM 2059 Photomask Linewidth Standard. Isolated linewidths and spacewidths range from 0.250 um to 312 um.

In response to customers' needs for more accurate photomask feature size measurements, NIST has worked extensively to improve mask metrology through optical image modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. In response to these problems, NIST introduced the Neolithography concept 1997: Modeling or emulating the effects of all of the relevant feature properties in both the mask metrology process and the wafer exposure and development processes, using existing and new software tools, can improve feature-size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes. This concept (at least in part) can be seen today in the design for manufacturing (DFM) sector of the industry.

DELIVERABLES:

- Compare and improve the accuracy of the NIST optical scattering code (developed by Egon Marx) with new scattering models developed by Spectel and others for use in transmission. Ongoing, through 4Q 2008
- Re-evaulate the parametric uncertainty in optical linewidth measurements, using new techniques to remove the small-linewidth overemphasis in the previously described metric. Present results at Microscopy and Microanalysis, 4Q 2008

2. The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are addressing the challenges of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which is now available as a NIST Standard Reference Material, #5001. The artifact can be used by the semiconductor industry to standardize 2-D feature placement measurements. The SRM 5001 was developed as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements.

A new generation of grids for the SRMs have been fabricated and measurements have been completed. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on the new Nikon 5i two-dimensional metrology tool at NIST. The Nikon 5i has been fully characterized and is now a calibration tool for grid calibrations. In response to industry needs, this tool is now under development for use as a wafer calibration tool for large distance position-to-position wafer calibration.

We have delivered all of the SRM 5001 grid plates, to the Standard Reference Material program. We

are now planning the next generation. From the detailed uncertainty budget for SRM 5001 the scale measurements are the largest component and the largest component of the Linescale Interferometer uncertainty budget is the wavelength correction for the index of refraction of the air.

The refractive index depends on the air pressure, temperature, relative humidity, CO^2 concentration, and the presence of small polarizable molecules like hydrocarbons (ethanol, methanol, and other cleaning agents). The correction for air pressure, temperature and relative humidity are made routinely, but the uncertainty from these three is currently at the state of the art and a significant reduction in the uncertainty is unlikely. CO^2 and other molecules are difficult to quantify, and are generally ignored.

Dr. Jack Stone of the Precision Engineering Division has worked on direct measurements of the refractive index over the last few years, and believes that absolute refractometers can be made to lower the uncertainty from the wavelength correction substantially. The method is based on variable-length Fabry-Perot refractometers in either back-to-back or side-by-side configurations. In a sense, the measurement scheme is doubly differential, which in this document we refer to as "VLDFP" (variable-length differential FP).

The VLDFP can be used to calibrate a simple fixed-length cavity near atmospheric pressure. The fixed-length cavity will then provide substantially improved pressure measurements relative to current state-of-art down to about 1 Pa. It will also work well at atmospheric pressure, not as an absolute device but as an excellent transfer standard that will be more robust, portable, and much easier to maintain than the VLDFP. At present it is difficult to say what would be a required re-calibration interval for the fixed-length cavity, but there are no known aging mechanisms of significance: needed recalibration intervals are more likely to be order-of decades rather than years.

The VLDFP-- or a simple fixed-length cavity calibrated with the VLDFP-- will also be the most accurate device in the world for measuring refractive index of air, which is a limiting step in practical realization of the meter. The capability of the device can be convincingly verified at an uncertainty that is orders of magnitude better than current state-of-art for refractive index measurement.

DELIVERABLES:

- The old cavities were made with fused silica mirror substrates optically contacted to zerodur spacers.

  The choice of materials gave rise to several problems, including poor temporal stability. We have purchased ULE rods to replace the zerodur in our new system and will use ULE for the mirror substrates to avoid thermally induced stress. 4Q 2008

- We are upgrading to Pound-Drever Hall (PDH) locking so as to alleviate a number of servolocking problems. This work is underway: we have the optical components in place and are currently building electronics for detecting the PDH signal and adjusting the laser frequency with a double-pass AOM (acousto-optic modulator). The new system will be completed and tested against previous performance. 4Q 2008

3. To strengthen the foundation of NIST's linewidth measurement traceability and to support the Bureau International des Poids et Mesures (BIPM) Mutual Recognition Arrangement, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements, Nano1. National metrology institutes in nine countries around the world are participating. PTB (Physikalisch Technische Bundesanstalt, Germany) has offered to supply two masks manufactured at the Advanced Mask Technology Center GmbH Co. KG (AMTC, Dresden) for the multilateral comparison Nano1 and a bilateral comparison between NIST and PTB. Since Nano1 will take several years (allowing 2-3 months for each laboratory plus overhead), the bilateral comparison is designed to provide more timely data to the AMTC. This bilateral comparison and Nano1 are to be kept as separate and independent as possible. A publication describing this bilateral comparison is planned for BACUS 2008.

DELIVERABLES:

- Upon delivery of the masks from PTB, they will be measured by AFM (Ron Dixson) and optically in the UV microscope. The Nano1 protocol will be revised to incorporate the AMTC mask. Upon acceptance of the protocol by participating laboratories, Nano1 will commence. 4Q 2008

Accomplishments

■ SRM 2800 Microscope Magnification Standard is a standard-size microscope slide with calibrated pitch features ranging from 1 μm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for

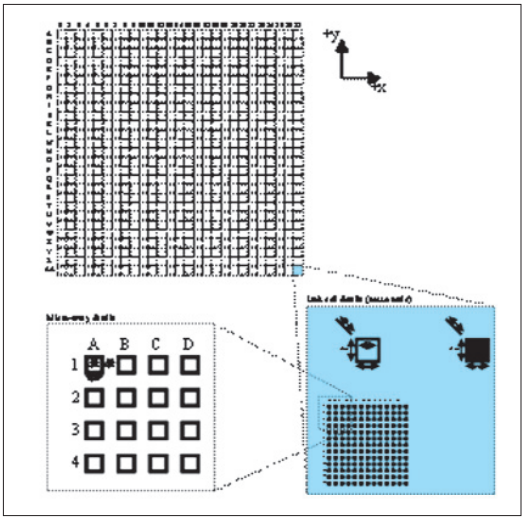

Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock has been sold.

■ The first set of two-dimensional grid artifacts, known as SRM 5001, were delivered to the SRM office and are selling well. These 152.4 mm (6 inch) photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. A second set of re-designed 152.4 mm (6 inch) feature placement standards has now been measured and fully calibrated in the close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4). The uncertainty budget for grid measurements and all documentation has been delivered to the SRM office and the second set of calibrated photomask grids will now be made available as a calibrated SRM.

■ In close collaboration with SEMATECH, we have completed a comprehensive report using optical methods for the calibration of phase shifting photomasks. This includes modeling and measurements in transmission and reflection. This document is available through SEMATECH as a tech transfer document.

■ A comprehensive suite of two-dimensional calibration methods for the calibration of optical systems and illumination systems is being developed based on the SRM 5001 grid calibration methodology. Some of these results were recently published at SPIE Microlithography. These methods are enabling a substantially improved optical calibration and alignment sequence as well as improved modeling inputs for more accurate linewidth measurements.

■ Completed a new set of comparator algorithms that enabled the SRM 5001 calibrations to be completed with the Nikon 5i tool in collaboration with the industry Ipro system. Completed the comprehensive analysis capabilities for centerline and edge detection methods with a complete uncertainty statement and remaining reticles delivered to the SRM office. Implemented the standard scale correction and new mapping software for the Nikon 5i system. Measured the set of two-dimensional calibration grids with a complete uncertainty analysis.

Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

Dr. Mark Davidson, Spectel Research Corp.

PTB (Physikalisch Technische Bundesanstalt, Germany).

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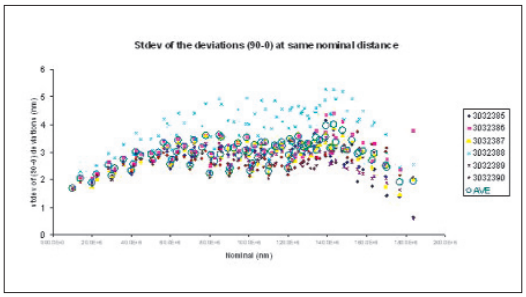

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Scatterometry-Based Dimensional Metrology

Goals

Our goals are to: (1) increase the effectiveness of scatterometry and other optical critical dimension (OCD) methods by providing industry with new measurement techniques, improved modeling, and standards; (2) provide assessments of accuracy and sensitivity of various OCD methods; and (3) develop facilities to accurately assess OCD targets. Develop improved OCD methods for assessing critical dimension and overlay.

Customer Needs

Scatterometry is increasingly becoming a preferred method for online critical dimension (CD) metrology. The method relies upon measurements of the reflectance or diffraction of small test grating structures as functions of angle, wavelengths, and/or polarization. By comparing measurement results with an extensive library of theoretical simulations or by performing a real-time regression analysis, tools can extract such line profile parameters as critical dimension, sidewall angle, and height, as well as more detailed descriptions of the sidewall shape.

While scatterometry has gained significant acceptance, it is continuing to grow in utility. However, there are many issues that remain that prevent it from having fundamental traceability. For example, the effects of finite illumination, finite target array size, line-edge and line-width roughness, uncertainties in the optical properties of the materials in the structure, neglect of surface oxides or other layers, radiometric accuracy, and the integrity of the theoretical model all contribute to the final measurement uncertainty in ways that are at this time poorly understood.

Ultimately, the industry needs reference artifacts that can test the validity of the results obtained by scatterometry tools. Such an artifact might consist of a set of gratings that have been characterized by a variety of techniques, including scatterometry, scanning electron microscopy (CD-SEM), atomic force microscopy (CD-AFM), and transmission electron microscopy (TEM). Scatterometry provides an method independent of the others, and if a comprehensive uncertainty budget were developed for the method, it would substantially improve the overall state of dimensional metrology.

Technical Strategy

There are three major strategies for improving the effectiveness of scatterometry. One strategy is to develop efficient models for the diffraction of light by structures on surfaces, so that NIST has state-of-the-art capabilities to perform scatterometry measurements and analysis as well as to provide standard data for a variety of model structures. The second strategy is to assess the sensitivity and accuracy of scatterometry methods to different structures, to provide industry with an understanding of what determines the ultimate sensitivity and accuracy of the methods. Finally, the third strategy is to develop in-house measurement capabilities with the long-term goal to perform scatterometry measurements on reference materials, to perform inter-laboratory comparisons, and to further develop the scatterometry technique.

Specific project elements are defined below:

1. **Theoretical Scatterometry Modeling** – Rigorous coupled wave (RCW) based theories are the most common methods used to analyze scatterometry data. We have developed in-house capability to perform RCW calculations for arbitrary one-dimensionally and two-dimensionally periodic structures. These codes are being used to generate libraries for profile extraction as well as for test calculations that assess the sensitivity of scatterometry to changes in model parameters or to non-ideal target profiles. We are using these codes to assess the effects of line-edge and line-width roughness, material anisotropy, as well as to perform RCW calculations on three-dimensional structures, such as contact holes. Building upon the SCATMECH library of codes that have been made available on the web for diffuse scattering calculations, we have published the RCW code for one-dimensionally periodic structures and will publish the code for two-dimensionally period structures in the future.

DELIVERABLES:

- Publication of theory for anisotropic lines. 3Q 2008
- Publication of RCW code for two-dimensionally periodic structures in the SCATMECH library. 3Q 2009

Technical Contacts:
T. Germer

2. Assessment of Accuracy and Precision of Scatterometry – Scatterometry relies heavily on prior knowledge of the specific structure being examined. For example, optical properties of all incorporated materials are required for the simulations. Reasonable parameterization of sidewall profiles are required to yield meaningful profiles. The effects of line-edge or line-width roughness are usually ignored. In this program element, we are assessing the impact that each model parameter has on the outcome of the measurement. The goal is to establish an independent uncertainty budget that includes all sources of random and systematic uncertainties. Furthermore, we are assessing the sensitivity limits of scatterometry, to determine how far into the future scatterometry tools can provide critical dimension metrology. A computer program, OCDSense, was written and provided to ISMI member companies to help determine the sensitivity and uncertainty of scatterometry for an arbitrary one-dimensionally periodic grating in any given tool.

DELIVERABLES:

- Provide initial sensitivity report to ISMI for sensitivity of scatterometry to contact holes. 4Q 2008
- Extend and deliver to ISMI a version of OCDSense for two-dimensionally periodic structures. 2Q 2009

3. Scatterometry Measurements – We have recently upgraded our laser-based Goniometric Optical Scatter Instrument (GOSI), Fig. 1, used for diffuse scatter measurements, to perform scatterometry measurements on industry-relevant targets on 300 mm wafers. The measurement capabilities include angle-scanned scatterometry at a number of discrete laser wavelengths. This instrument has the capability to perform conical scatterometry measurements and will be used to perform traditional measurements as well as measurements of higher-order, non-specular diffraction and diffuse scatter. A long term goal is to develop reference scatterometry targets, measure them with this instrument, provide accurate determinations of their dimensions and profiles, and have an uncertainty placed on the results. Another long term goal is to develop novel measurement modalities that improve the utility of scatterometry. One method we have demonstrated is microscope-based scatterometry using back focal plane imaging. This technique enables collection of multiple diffraction order scatterometry signatures in a single image, can be configured for both dense and isolated targets,

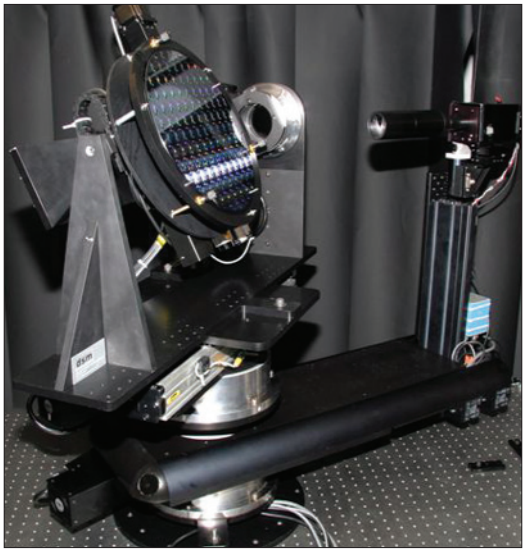

Figure 1. The new Goniometric Optical Scatter Instrument (GOSI) is a reference reflectometer for diffuse and specular scattering measurements having 300 mm sample capability.

and allows scatterometry and image-based metrology to be performed on the same tool. Future projects will include the development of spectroscopic scatterometry instruments.

DELIVERABLES:

- Perform time-sequenced measurements of nanoimprint polymer gratings during heating. 1Q 2008
- Construction of a spectroscopic scatterometry capability at NIST. 1Q 2009

Accomplishments

■ We have developed efficient rigorous coupled wave (RCW) software for one- and two-dimensionally periodic structures (arrays of two- and three-dimensional features). Results of the in-house code have been compared with finite difference time domain, surface integral equation, and other RCW implementations. This software is also configured to run on a large cluster computer, so that library generation is possible. The code for one-dimensionally periodic structures has also been extended to allow for anisotropic materials in the structure.

■ As part of our effort in assessing the precision and accuracy of scatterometry, we have performed a study of the sensitivity of scatterometry to CD and sidewall angle for a large number of different measurement modalities, including angle-scanned and wavelength-scanned reflectometry and ellipsometry, for amorphous silicon gate and gate-resist struc-

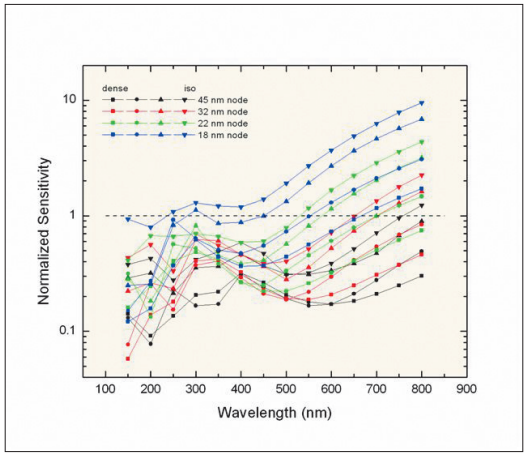

Figure 2. Estimated bottom dimension sensitivity, normalized by the 2% of bottom dimension specification, calculated for gate gratings measured by angle scans of the reflected Stokes parameters with angles less than 70°.

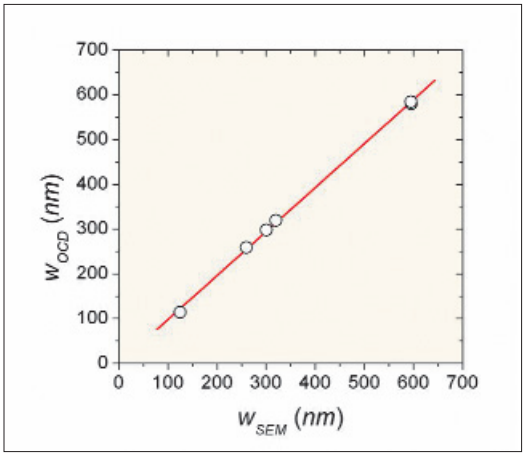

Figure 3. CD linewidth extracted from OCD, wOCD, versus linewidth measured by SEM, wSEM, for six targets on an SCCDRM chip.

tures. This study included parameters appropriate from the 45 nm half-pitch node to the 18 nm half-pitch node. The results (see Fig. 2) demonstrated that scatterometry can achieve the necessary sensitivity to measure dense gratings at these nodes. Future work, however, will be necessary to achieve sufficient sensitivity to isolated features.

■ In the area of scatterometry-based optical critical dimension (OCD) measurement, we have recently measured OCD linewidth of lines in grating targets fabricated using the single-crystal critical dimension reference materials (SCCDRM) process. The SCCDRM implementation, developed by a multi-laboratory collaboration at NIST, provides lines with known geometries – typically vertical sidewalls – defined by the silicon lattice, and has led to development of a prototype linewidth standard for isolated lines designed for use in AFM calibration. We have shown that the linewidth obtained from the OCD technique for these targets is linearly related to linewidth obtained from SEM, with a slope near unity and zero offset. Continuing efforts to reduce linewidth roughness of the target, to analyze uncertainties in the OCD measurement, and to evaluate the suitability of these targets for OCD reference materials, are ongoing.

■ We have also extracted OCD linewidth from scatterometry signatures of silicon-on-silicon gratings obtained using back-focal-plane imaging in a microscope. We investigated targets with only specular reflectance (grating pitch 300 nm) and those with both specular and higher-order diffraction (grating pitch 600 nm). Linewidths of 131 nm to 140 nm were obtained, with the back-focal-plane signatures demonstrating nanometer-level sensitivity to linewidth, and a linear relationship of linewidth obtained from scatterfield microscopy to linewidth measured by SEM was shown.

Collaborations

International Sematech Manufacturing Initiative, Benjamin Bunday, Limits of Scatterometry Study.

Department of Electrical Engineering, Texas A&M University, Professor Krzysztof Michalski, Modeling of Scattering by Lines Having Anisotropic Optical Properties.

Recent Publications

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Small Angle X-Ray Scattering

Technical Contacts:
R. L. Jones
W. L. Wu

Goals

To develop a transmission geometry small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, linewidth fluctuations, and line edge roughness, and statistical deviations across large areas in dense high aspect ratio patterns. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. Further, the wavelengths utilized by SAXS based measurements well complement current metrology tools based on optical scatterometry, SEM, and AFM.

Customer Needs

The drive to reduce feature sizes to sub-50 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the calibration of standards for current industrial solutions such as CD-SEM.

Technical Strategy

1. Advancements in lithography have enabled the sub-50 nm patterning by 2009, at this node and beyond the control of CD on the level of nanometers and in some cases sub-nanometer becomes necessary. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of Angstrom level precision in critical dimension evaluation over large (50 μm x 50 μm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission using a sub-Angstrom wavelength. The high energy of the X-ray source allows the beam to pass through a production quality silicon wafer, and could become amenable to process line characterization. The measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors are sufficient to implement a laboratory scale device capable of high precision measurements. NIST has designed and installed the world's first laboratory scale CD-SAXS device (see Fig. 2). This year, the lab

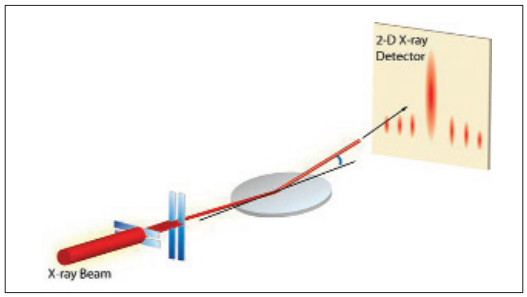

Figure 1. Schematic of the Critical Dimension Small Angle X-ray Scattering (CD-SAXS) configuration. Shown is the collimated high energy X-ray beam passing in transmission through a silicon wafer and scattering from the test pattern on the surface. The scattered X-rays are measured on a 2-dimensional X-ray detector. Cross sectional information is obtained by measuring the sample at varying sample rotation angles as depicted.

Figure 2. The world's first laboratory scale CD-SAXS prototype constructed on the NIST campus. Shown is the rotating anode molybdenum source (left side) used to generate high energy X-rays for transmission measurements on samples measured at varying angles of incidence on a 2-dimensional detector (back right).

scale prototype has become an integral part of measurements, providing the first quantitative measurement of FinFET structures.

DELIVERABLES:

- Publish evaluation results from laboratory scale CD-SAXS instrument. 1Q 2008
- Complete and publish cross-sectional measurements using laboratory scale CD-SAXS instrument on patterns produced with EUV lithography as part of round-robin study with SEMATECH and Intel. 2Q 2008

2. CD-SAXS has been extended for LER measurements. Our approach is to provide metrology of sidewall roughness, which is defined as deviations from the average sidewall plane on length scales smaller than the CD. In collaboration with the Advanced Metrology Working Group at SEMATECH, NIST has designed a series of structures to model different types of roughness. This year, NIST has completed the second round robin measurements of LER in collaboration with SEMATECH and Intel to provide the first comparisons of CD-SEM and CD-SAXS (see Fig. 3). The results have been published and presented at the 2008 SPIE Advanced Lithography Meeting.

DELIVERABLES:

- Develop and publish refined models of line edge roughness scattering to fit second round of measurements of line edge roughness on model photoresist patterns produced by EUV lithography. 1Q 2008
- Complete and publish round-robin measurements involving Intel and SEMATECH to compare line edge roughness measurements between CD-SAXS and CD-SEM in oxide line/space patterns created by EUV lithography and pattern transfer, identifying key differences between measurable quantities. 4Q 2008

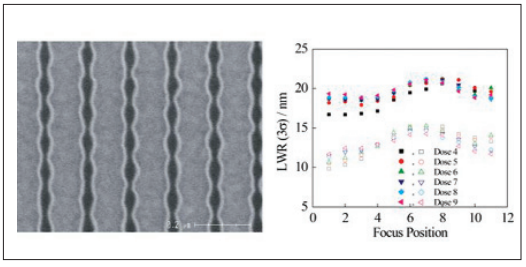

Figure 3. Top-down SEM of model line edge roughness structures (left) used as part of the round-robin LER measurements in collaboration with Intel and SEMATECH and the resulting CD-SAXS measurements of linewidth roughness (LWR) across a dose-exposure matrix. SEM results (open symbols) are consistently below these from CD-SAXS measurements (filled symbols).

3. Pattern shape metrology is facing new challenges as new 3D structures are emerging including FinFETs covered with nanometer thick layers of high k materials. Effective manufacturing requires characterization of the total pattern shape as well as the dimensions and relative positions of individual layers. CD-SAXS features a capability to non-destructively probe test patterns with multiple materials. These measurements utilize data taken at a series of angles of incidence to reconstruct the average cross-sectional line shape. Preliminary results from an array of model FinFET structures indicate an ability to measure these complex structures during different stages of processing, providing valuable data on next-generation manufacturing. Ongoing analysis and technique refinement will develop models to quantify with high precision line shape parameters needed for patterns with multiple, distinct layers to establish the limits of the technique in future technology nodes.

DELIVERABLES:

- Complete CD-SAXS measurements of model FinFET structures with thin conformal outer high k layers. 2Q 2008
- Develop and apply refined CD-SAXS models to incorporate the effects of multilayer coatings on line tops and sidewalls. 4Q 2008

Accomplishments

■ We have developed and demonstrated the capabilities of CD-SAXS to provide high precision measurements of pattern pitch, line width, line height, and sidewall angle. The first measurements of sidewall angle were made the Advanced Photon Source (Argonne National Laboratory) in collaboration with the IBM T. J. Watson Research Center (Q. Lin). The protocol involves measurements of the sample over a wide range of incident angles, and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle. The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as a T-topped line, will produce different scattering patterns. The protocol has been generalized to more arbitrary shapes, including patterns with rounded corners and sidewalls.

■ Our group has also demonstrated a capability to measure correlated fluctuations in line edge position as a measure of line edge roughness. CD-

SAXS measurements of a series of line/space patterns with model LER were produced using 193 nm lithography in collaboration with the Advanced Metrology Advisory Group (AMAG) coordinated by SEMATECH. This initial study provided key data on the sensitivity of CD-SAXS to LER, including the development of models for LER and LWR contributions, in lines possessing periodic sidewall roughness with amplitudes of 3 nm. In addition, a methodology and experimental data was published describing a route to use CD-SAXS as a measure of roughness propagating normal to the substrate. Samples of photoresist line/space patterns were provided by the IBM T. J. Watson Research Center (A. Mahorawala). This type of roughness is commonly observed in photoresists due to imprecise tuning of the underlying anti-reflective coating. Given the ability of CD-SAXS to extract the periodic component of roughness from non-periodic, the technique is capable of quantitatively extracting this component of roughness even when the amplitude is small compared to the random component.

■ NIST has completed the second round-robin measurements of LER in sub-50 nm line/space resist patterns using CD-SAXS. Samples were designed with controlled LER to be measured by CD-SEM and CD-SAXS in blind measurements. Samples were produced in collaboration with Intel and measured by optical scatterometry at Intel, by CD-SEM at SEMATECH, and CD-SAXS at NIST in blind measurements. The data was collected and summarized in a paper presented at the 2008 SPIE Advanced Lithography meeting.

■ Studies have also demonstrated the potential of CD-SAXS to detect and to quantify the extent of sidewall damage of nanoporous low-κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low-κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ, it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low-κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low-κ material, then backfilled the trenches with the same candidate low-κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays. These results indicate the potential of CD-SAXS to probe more complex structures such as FinFETs non-destructively for future manufacturing needs.

■ The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height, and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature (TG). Heating these patterns below TG does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above TG, the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

Collaborations

Polymers Division, MSEL, Chengqing Wang, Derek L. Ho, Christopher L. Soles.

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, Melissa Shell, sub-50 nm structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

Molecular Imprints, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

IBM Yorktown Heights, Qinghuan Lin, Development of pattern shape and sidewall angle metrology.

Recent Publications

D.L. Ho, C. Wang, E. K. Lin, R. L. Jones and W.-L. Wu, *"A Laboratory Scale Critical-Dimension Small-Angle X-ray Scattering Instrument"*, AIP Conference Proceedings, 931, 382, (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, B. J. Rice, K. Choi, G. M. Thompson, S. J. Weigand, D. T. Keane, *"Characterization of Correlated Line Edge Roughness of*

Nanoscale Line Gratings using Small Angle X-Ray Scattering," J. Appl. Phys. 102, 024901 (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, J. Leu, *"Standing Wave Roughness Characterization in Photoresists by Small Angle X-Ray Scattering,"* Appl. Phys. Lett. 90, 193122 (2007).

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R. L. Jones, C. L. Soles, E. K. Lin, W. Hu, R. M. Reano, S. W. Pang, *"Pattern Fidelity in Nanoimprinted Films using CD-SAXS,"* J. Microlith. Microfab. Microsyst. 05, 013001 (2006).

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H. W. Ro, Y. Ding, H. J. Lee, D. R. Hines, R. L. Jones, E. K. Lin, A. Karim, W.-L. Wu, C. L. Soles, *"The Role of Stress in Nanoimprint Lithography,"* Proc. SPIE 6151, 348 (2006).

R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, *"Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing,"* 6, 1723 (2006).

Grazing Incidence X-Ray Scattering-Based Dimensional Metrology

Technical Contacts:
W. L. Wu
R. L. Jones

Goals

To develop a grazing incidence small angle X-ray scattering (GI-SAXS)-based methodology to complement the normal incident or transmission SAXS for quantitatively and non-destructively measuring the critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, depth dependent composition, and statistical deviations across large areas in dense high aspect ratio patterns. In contrast to transmission, and small angle X-ray scattering GI-SAXS is performed in reflection, and this configuration results in both significant challenges in data interpretation and vast increases in signal-to-noise; therefore, it makes possible a reduction in measurement time. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. In comparison with transmission SAXS, a longer X-ray wavelength X-ray beam can be used for GI-SAXS; this will help relax some of the strict optical collimation requirements and help reach high flux at the sample.

Customer Needs

The drive to reduce feature sizes to sub-32 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the calibration of reference standards for current industrial solutions such as CD-SEM.

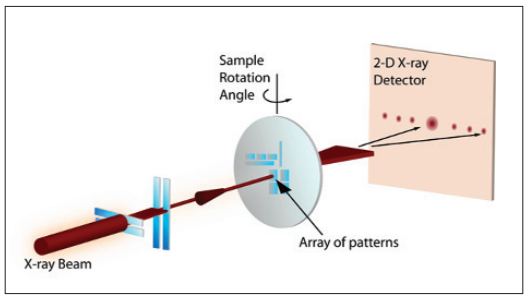

Figure 1. Schematic of the Grazing Incidence Small Angle X-ray Scattering (GI-SAXS) measurement configuration. Shown is the collimated sub-nm wavelength X-ray beam reflecting off the sample at a grazing angle, and the diffraction pattern measured on a 2-dimensional X-ray detector.

Technical Strategy

1. The emergence of viable lithography solutions for sub-32 nm patterning will require sub-nm precision control of CD and pattern shape built within multilayer structures. These requirements will challenge traditional measurement methods including CD-SEM and optical scatterometry. We are developing X-ray based dimensional metrology tools capable of Angstrom level precision in critical dimension evaluation over large (50 μm x 50 μm) arrays of periodic structures. As depicted in figure 1, Grazing Incidence Small Angle X-ray Scattering (GI-SAXS) is performed in reflection, using a configuration similar to current optical-based CD metrology tools. However, GI-SAXS utilizes a sub-nm wavelength to measure dimensions well within the diffraction limit. GI-SAXS as a measurement method has significant benefits associated with enhanced intensity at grazing incidence in the vicinity of the critical angle which is less than one degree. High precision measurements require the development of high precision sample stages suitable to align a highly collimated incident X-ray beam with small beam cross section on target pattern areas with dimensions on the order of 10s of μm. Previously, NIST has designed and installed the world's first laboratory scale CD-SAXS device for transmission measurements. This year, a new module will be designed and installed to allow for the development of grazing incidence measurements.

DELIVERABLES:

- Complete design of sample stage with alignment microscope and associated detector attachments to facilitate accurate alignment and measurement of GI-SAXS experiments on a lab-scale X-ray instrument. 1Q 2008

- Build and experimentally validate a high precision goniometer with linear beamstop for first grazing incidence measurements on a lab-scale prototype instrument. 2Q 2008

2. Quantitative modeling of grazing incidence scattering is required to enable characterization of pattern cross section. Models to describe the high degree of interaction of the X-ray beam with the sample at grazing incidence will require detailed measurements of instrumental coherence length, resolution functions, and wavelength distribution. In addition, experiments are required to determine the effects of dynamic diffraction. Preliminary measurements of test patterns demonstrate the simplicity of diffraction patterns measured in transmission CD-SAXS relative to the reflection scattering of GI-SAXS (see fig. 2). Our approach is to measure the structure of test patterns using both CD-SAXS and grazing incidence geometries. This two measurement approach will provide a unique capability to develop quantitative models to incorporate the effects of dynamic scattering effects characteristic of grazing incidence scattering but absent in transmission scattering. Test samples will leverage results from CD-SAXS studies developed and measured in cooperation with the Advanced Metrology Working Group at SEMATECH and Intel.

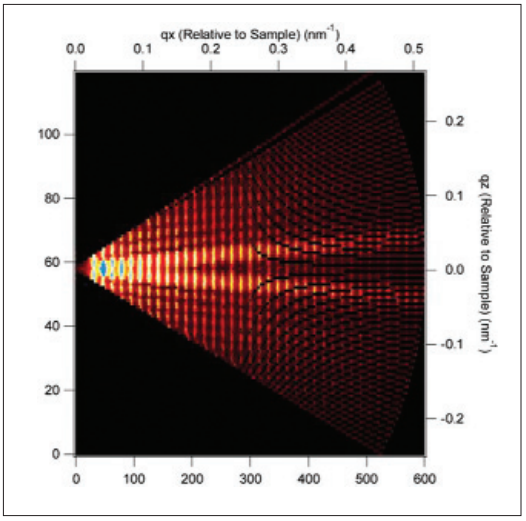

Figure 2. CD-SAXS data measured on a 400 nm pitch grating with 200 nm wide lines. The data are collected over an angular range of +/- 70 degrees from normal incidence and transformed into the Fourier space. The periodic fringes on the horizontal axis originate from the pitch and line width, while the V-shaped bright streaks indicate the sidewall angle.

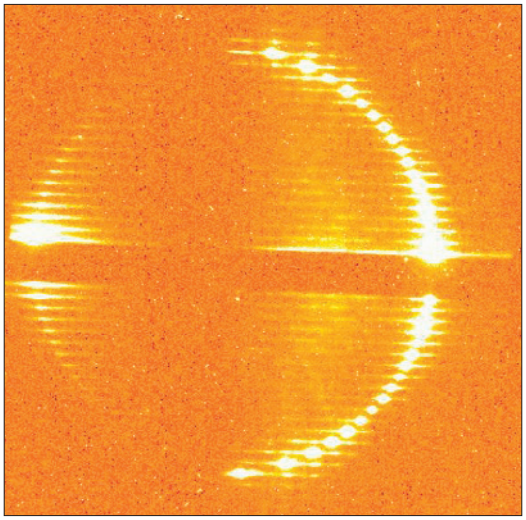

Figure 3. GI-SAXS data measured on a similar line/space pattern. The data shown as the hemisphere on the right half can be accounted for from a kinetic model - the intersection of the Ewald sphere with the diffraction rods. The hemisphere on the left is unexpected from the kinetic model and its origin is likely from the interaction between the reflection and scattering. A line-shaped beamstop prevents direct reflection of the beam into the detector.

DELIVERABLES:

- Complete CD-SAXS measurements of test patterns produced by optical lithography with high precision transmission scattering models. 2Q 2008
- Complete GI-SAXS measurements of the same test patterns used in CD-SAXS deliverable item listed above. 4Q 2008
- Evaluate the magnitude of the dynamic effects observed in GI-SAXS measurements and start to develop the theoretical framework for quantitative data analysis. 4Q 2008

Accomplishments

■ We have completed the construction and preliminary alignment tests of a sample stage with alignment microscope and detector accessories suitable for performing high precision GI-SAXS measurements. Initial measurements of a test sample in both transmission CD-SAXS geometry (see figure 2) and grazing incidence geometries (see figure 3) demonstrate the additional complexity and potential information content of grazing incidence measurements. Review of theoretical work capable of modeling the interaction between reflection and scattering is in progress.

Collaborations

Polymers Division, MSEL, R. Joseph Kline, Chengqing Wang, Derek L. Ho, Christopher L. Soles.

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, sub-50 nm test structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

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R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, *"Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing,"* 6, 1723 (2006).

Atom-Based Dimensional Metrology

Technical Contacts:
R. Silver

Goals

Provide technological leadership to semiconductor and nanoelectronics manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs for advanced lithography. One specific goal is to provide customers with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable and allow transfer to other measurement tools that can measure the artifacts with dimensions known on the nanometer scale.

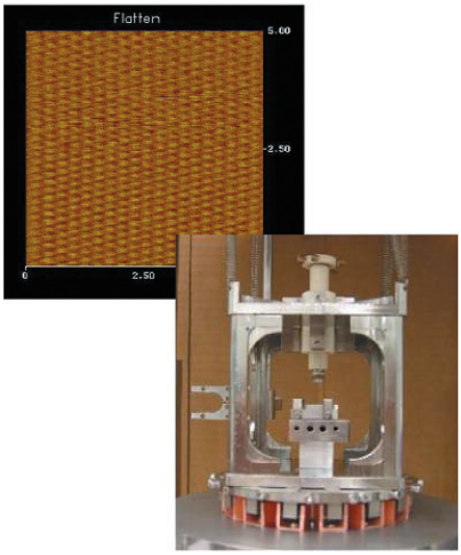

Figure 1. A new STM structure design has been implemented to improve the atomic scale imaging and structural characteristics. This system will provide improved nanometer scale interferometer-based imaging and measurement capabilities.

Customer Needs

This project responds to the U.S. industry need for length-intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and present a unique solution to meet the future measurement, test artifact, and calibration standards needs of the nanoelectronics industry. One important application of the high-resolution SPM methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a unique NIST-designed picometer resolution interferometer (Fig. 1).

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of dimensional metrology tools. We are also developing unique high-resolution interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions at the nanometer scale. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available commercially at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (see Fig. 2, next page). As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical CD tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed

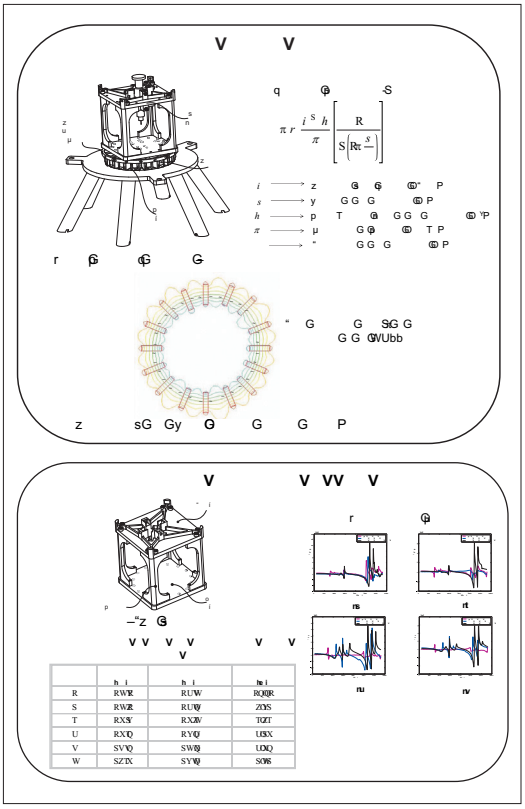

Figure 2. NIST SRM 2059 Photomask Linewidth Standard. Isolated linewidths and spacewidths range form 0.250 um to 312 um.

elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation make the concept of reference samples with known geometry and width essential. This project is developing samples of known geometry and atomic surface structure which yield well defined dimensional measurements. One goal is a measurement which results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the UHV environment and then stabilized and subsequently transferred to other instruments.

The methods of atom counting and high-resolution interferometry outlined in this project description are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare lithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order, which is commensurate with the underlying crystal lattice. This involves either using advanced photolithography methods, electron beam lithography, or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES:

- Write features in (100) silicon with critical dimensions smaller than 5 nm. Apply the pattern generation process and etch features for use as test structures using the Scanning Tunneling Microscope (STM). 1Q 2009
- Work with CNST and ISMT to develop improved methods for etching nanostructures written in silicon. Use Rapid Ion Etching (RIE) etching techniques to etch features with sub-5 nm dimensions in silicon. 3Q 2009

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We have and continue to develop SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W (111) tips and produce atomic resolution on Si (7x7) surfaces and 2x1 reconstructed Si (100) surfaces. These tips are also useful in SEM applications for use as nanotip SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES:

- Verify routine atomic resolution using W (111) single crystal tungsten tips. Determine the stability of these W tips for use in STM imaging. 4Q 2008

3. Development of artifacts that can be atom counted and subsequently measured in other metrology tools such as SEM and AFM. The in-

tegrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. This effort for linewidth artifacts is currently focused on developing Si (111) wet chemical processing methods with reduced process temperatures which yield atomically ordered surfaces. The use of wet chemical processing has been demonstrated on atomically ordered Si surfaces at significantly reduced temperatures. Current research utilizes in situ processing apparatus from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures.

DELIVERABLES:

- Use the UHV sample heating and tip preparation capabilities in the Omicron UHV STM system for atomic resolution imaging of Si (111) hydrogen terminated surfaces. Investigate atomic resolution imaging of chemically terminated Si samples and compare with UHV hydrogen terminated samples. Use the in situ prepared samples from the UHV preparation facility to evaluate improved Si imaging with alternative tip materials and atomic surface reconstructions. 2Q 2009

4. Develop the new UHV Omicron system and the in-house designed facility for improved robust atomic resolution imaging, (see Fig. 3). The new imaging capabilities are being developed and applied to etched silicon features provided by SEMATECH or NIST on Si (100) wafers. The intent is to provide atomically resolved and precisely imaged quantitative results on etched silicon substrates. These nano-meter-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples.

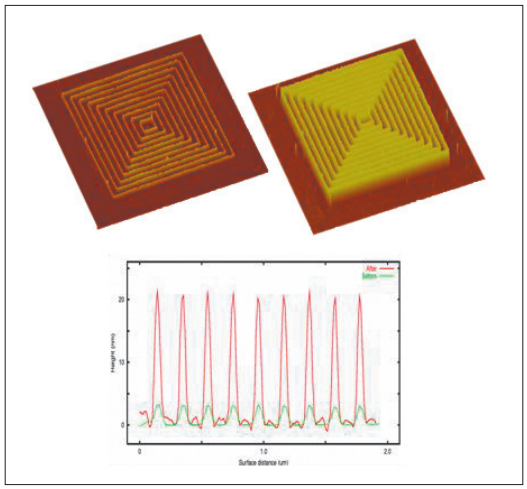

Figure 3. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.

Accomplishments

■ The atom-based dimensional metrology project has successfully agreed to a DARPA contract for a 3 phase 5 year funded effort to develop massively parallel arrayed tip nanofabrication techniques. This DARPA funded contract is a comprehensive collaborative effort between NIST, industry leader Zyvex, University of Illinois and the University of Texas and other partners. This represents a significant DARPA focus for advanced lithography and metrology on the atomic scale which is fully extendable to atomically precise patterning and metrology to support and enable arrayed tip fabrication at the atomic scale.

■ The ability to prepare atomically sharp tips in W (111) has been demonstrated. We are now implementing a robust methodology for repeatable UHV tip preparation. This is based on the new tip processing capability in the UHV STM system and will be developed to allow atomic tip preparation without the need for the field ion field electron microscope (FIFEM). We are working with industry and university leaders to evaluate the leading technologies for atomic resolution tip performance.

■ A workshop from the SPIE Nanotechnology Working Group on massively arrayed nanofabrication techniques for future semiconductor manufacturing was held at Microlithography 2008. The workshop was organized by Rick Silver and Chris Soles included presentations and a panel discussion involving several industry and University leaders. The Nanotechnology Working Group is chaired by Rick Silver and Chris Soles and has served as a forum for developing and applying nanotechnology related manufacturing and fabrication elements which will directly benefit the semiconductor manufacturing community.

■ In the continuing collaboration between the NIST atom-based dimensional metrology project and the Department of Mechanical Engineering at the George Washington University, an invited presentation was given at this years ASPE conference on dynamic analysis and eddy current damping effects in atomic resolution imaging instruments. The work was based on solid model Pro E and Pro Mechanica modeling of structures for use in high resolution imaging tools such as the UHV STM. The actual instrument modeled is located in the AML and the mechanical structure used for this measurement instrument was based directly on the

modeling results. The modeling results were further verified by using accelerometer measurements to match the theoretical modeling to experiment. The publication focused on this quantitative comparison including a full modal analysis. Atomic resolution imaging performance was verified using the new design implementation.

■ An in-depth paper was published in the Journal of Physical Chemistry. The paper is a comprehensive set of experimental and theoretical analyses of the preparation of silicon surfaces. This work was carried out in large part by Post Doc Hui Zhou and in collaboration with the University of Maryland, Department of Physics. This paper follows on a paper published in late 2005 in the Journal of Physical Chemistry titled "The Influence of defects on the morphology of Si (111) Etched in NHF". In this new paper we have extended the kinetic Monte-Carlo simulation method to study the etching dynamics of Si (111) surfaces in NH4F in a time-resolved basis. We have examined the step-flow dynamics of Si (111) etching using various simulation window sizes for variety of miscut angles and miscut orientations as well as those parameters which affect the formation of etch pits. The simulation results have been compared with published experimental data to derive an absolute time scale.

■ We have prepared atomically flat surfaces and obtained atomic order on Si (100) surfaces. The routine imaging of these surfaces on the atomic scale is a new focus to both move the silicon processing to the more widely used Si (100) surfaces and to use more controlled UHV processing techniques. These results are a substantial step forward in repeatable silicon surface preparation for atomic scale metrology and are now being carried out in collaboration with DARPA and several industry/university researchers. The results, seen in Fig. 4, show the recent progress in atomic resolution imaging and preparation of the Si (100) surfaces and are a primary direction for the DARPA funded research

■ The silicon etching process has been developed and demonstrated for patterns written on silicon. Patterns with features as small as 10 nm have been written in hydrogen-terminated silicon surfaces with subsequent pattern transfer into the silicon substrates. A publication recently appeared on this material. The importance of etching structures in Si (111) is now being supported

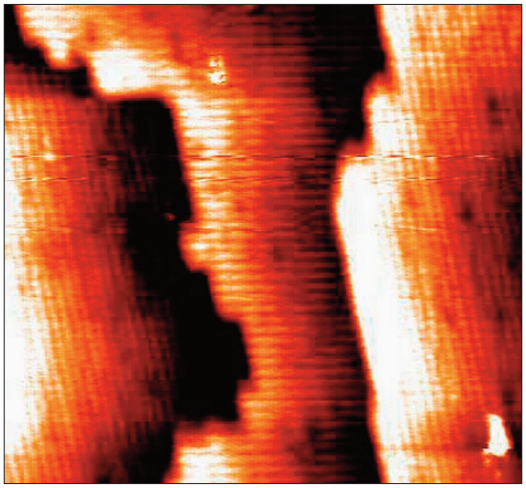

Figure 4. Atomic resolution image of a Si (100) surface prepared in vacuum. Current research within the DARPA funded effort is focused on atomic scale fabrication and measurements of these widely used substrates that are based on the intrinsic crystal lattice.

by SEMATECH and a recent collaboration between NIST and SEMATECH to develop lithography methods and plasma-etch methods at SEMATECH's fab is now under way.

■ A paper was presented to the ASPE special topics conference by Summanth Chikkamaranahalli, a graduate student from the George Washington University. The paper is an excellent analysis of damping and precision structures for use in STMs and atomic scale imaging. The analysis and modeling have been used in the development of the NIST STM for the atom-based dimensional metrology project. The tool has recently taken very nice high resolution atomic scale images. The scanning tunneling microscope was designed by the NIST team in collaboration with Prof. Vallance at the George Washington University. The finite-element analysis (FEA), static and dynamics analysis using Promechanica packages gave the researchers quantitative tools to evaluate and develop the STM imaging head, and larger mechanical structure.

■ We have used the field ion microscope (FIM) techniques to analyze W (111) tips for use in atomic resolution imaging. The single crystal W tips were directly characterized for use as SPM tips with dimensional analysis on the atomic scale. We are now using these tips for significantly more robust atomic resolution imaging.

Collaborations

DAROPA, Zyvex, University of Illinois, University of Texas, Sematech, IBM, University of Maryland, Dept. of Physics, George Washington University, Dept. of Mech. Eng.

Publications

H. Zhou, J. Fu, and R. M. Silver, *"A Time-resolved Kinetic Monte-carlo Simulation Study on Si (111) Etching,"* Journal of Physical Chemistry C, Vol. 111, p. 3566 (2007).

S. Chikkamaranahalli, R. Vallance, B. Damazo, and R. M. Silver, *"Damping Mechanisms for Precision Applications in UHV Environment,"* Proc. ASPE Conf., Pitts. PA (2006).

S. Chikkamaranahalli, R. Vallance, B. Damazo, R. M. Silver, and J. Gilsinn, *"Dynamic Modeling and Vibration Analysis of a UHV Scanning Tunneling Microscope,"* Proc. ASPE Conf., Norfolk VA (Oct. 2005).

H. Zhou J. Fu, and R. M. Silver *"The Influence of Defects on the Morphology of Si (111) Etched in NH4F,"* J Chemical Physics B, 109, 23386 (2005).

Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Technical Contacts:
M. W. Cresswell

Goals

The goal of this project is to develop test-structure-based reference materials with emphasis on supplying road-map-compliant physical standards for critical-dimension (CD) metrology-tool development and calibration. The specific near-term goal is fabricating, and supplying to the NIST SRM (Standard Reference Material) office for distribution, a quantity of CD reference-features with nominal CDs in the range 20 nm to 160 nm and having 2σ (expanded uncertainties) of less than 1.1 nm by September 2009. The motivating application is primarily AFM-tip calibration but other possible applications that have emerged, since the research was begun, include the monitoring of CD SEM and optical CD metrology (OCD) tools. The technology that this project has developed for fabricating CD reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation. It is now clear that the SCCDRM format could also be advantageously applied to the development of related nano-artifacts such as step-height standards. An over-arching goal is to fabricate and calibrate a selection of SCCDRM-based artifacts that will be made available to industry and academic users through the NIST SRM Program. This goal will be well-served by the Project's ongoing uncertainty-reduction program which will take advantage of unique and diverse expertise at NIST in alternative primary- and transfer-metrologies such as SAXS (Small-Angle X-Ray Scattering) and angle-resolved optical scatterometry.

Customer Needs

The Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS) 2007 p.39 under "Reference Materials" Section in the Metrology Volume, states that it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials- and process-equipment development. This project is concerned specifically with ensuring a source of such reference materials to satisfy the stated need throughout the near-term years.

Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The roadmap projects the decrease of microprocessor unit (MPU) physical gate lengths used in state-of-the-art IC manufacturing from present levels of 28 nm to 13 nm during the near-term years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding specifications for these applications. It is widely believed that the situation can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

Customers' needs to replace the carrier-wafer with a monolithic implementation is that the former is vulnerable to contamination originating during post-assembly cleaning. Ordinarily this is not a leading concern in AFM-tip calibration, although it cannot be dismissed for SCCDRM use in ultra-clean facilities. Otherwise, tip calibration is becoming widely recognized as an application for which SCCDRM reference materials are well suited.. However, an emerging application of interest in the industry is SEM tool calibration. In this application, regular reference-material feature-cleaning is necessary due to the nature of the metrology.

The emerging metrology known as optical-CD (OCD) scatterometry translates broadband light, diffracted from an on-wafer grating patterned into the resist or film, into accurate profiles of the grating's features from which key parameters, such as CD, can be extracted. Whereas currently favored metrology tools such as CD scanning electron microscopes and AFMs require a vacuum wafer environment, OCD metrology does not, and is fast and non-invasive. The possibilities of OCD extend to characterizing the sidewall angle and height of critical features. Until physical standards are available, the full promise of OCD control scatterometry may not be met.

Further details of customer needs that have been identified since the SCCDRM distribution to SE-

MATECH Member Companies in January 2005, and now impact the project's responding technical strategy, are described in the next section.

Technical Strategy

The fundamental SCCDRM technical strategy is to pattern Silicon on Insulator (SOI) device layers with lattice-plane selective etches of the kind used in silicon micro-machining, which provides reference features with quasi-atomically-planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if sidewall nano-planarity can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the implementation include starting silicon SOI wafers with the device layer having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micromachining. However, the difficulty of obtaining satisfactory SOI material in larger diameters has driven us towards parallel evaluation of a bulk-wafer starting-material strategy. The roadmap states that measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. The traceability path for dimensional certification of the project's SCCDRMs is responsive to this requirement and originates with measurement of a selection of reference-feature CDs with both Atomic-Force Microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM) imaging. The former technique is highly repeatable and of manageable cost while the latter enables a lattice-plane count that allows expression of the each CD in terms of a traceable distance, which is the periodicity of silicon (111) lattice planes. However, HRTEM is totally destructive and thus is not useful for supplying reference features to end users. The project's traceability strategy thus features state-of-the-art AFM as a transfer metrology to deal with this constraint. Transfer metrology relates CDs extracted by AFM to be traced to SI units through the construction of a so-called calibration curve. An example of such a curve is shown in Fig. 1 (next page). To maintain maximum possible accuracy in the transfer-metrology operation, an elaborate reference-feature selection protocol has been established to identify reference features that qualify by virtue of their CD uniformity, as contributors to the construction of the calibration curve, or for delivery to end users. Multiple reference features on a large set of as-patterned test chips are identified initially by high-power optical inspection. This procedure checks primarily for continuity, cosmetics, and apparent uniformity of the narrowest-drawn sets of six features that are incorporated into test structures, which are called HRTEM targets. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to etched CDs of between 50 nm and 300 nm. The "best" 10 % of the AFM targets passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20 K magnification to narrow the selection process further. Digitized profiles of the CDs of top-down SEM images are then extracted at 25nm intervals. The measurements are transferred to a database, which is then interrogated to identify chips, and AFM targets on them, that have more uniform SEM-CD profiles at the narrower CDs — typically less than 150 nm. Candidate AFM targets so identified on each chip are then CD-profiled by AFM. Chips having AFM targets with all six features having superior uniformity are then partitioned into a calibration sub-set and a product subset. All six features of the selected targets on the chips on the calibration sub-set are then subjected to HRTEM imaging. These are the chips whose designated AFM targets are to be used as contributors to the calibration curve. The design of all HRTEM targets enables the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve spanning a 150 nm range. However, the logistics described above make the CD-traceability path very costly to implement, and hinder the pace of necessary technology advancement. A central problem is that adequate facilities for both HRTEM and AFM tend to have limited availability. Cost becomes substantial when operator/engineering skills, maintenance, down time, etc., are accounted for. For these reasons we have proposed evaluation of two alternative traceability approaches the first is to identify technically and economically acceptable replacements for either or both the current primary and transfer metrologies, and the second is to eliminate the need for transfer metrology altogether by calibrating with a single traceable metrology on a 100% basis. As far as replacing HRTEM as the primary metrology is concerned,

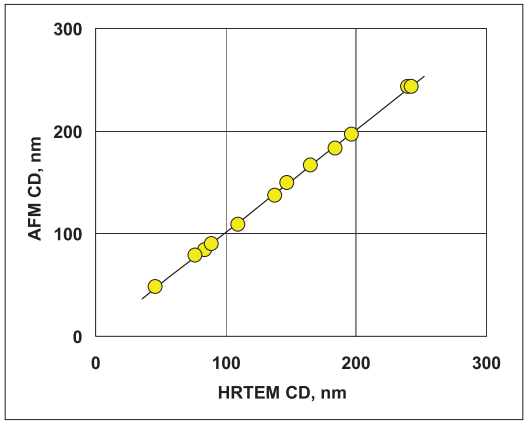

Figure 1. Transfer metrology relates CDs extracted by AFM to be traced to values SI units through the construction of a so-called calibration curve.

we have observed that both SAXS and OCD could provide competitive accuracy for the average CD of features of an SCCDRM grating. Of course, it follows that the uncertainty of a local CD within the grating is then driven by the uniformity of the grating's features. A possible AFM transfer-metrology replacement is CD-SEM. Its superior repeatability for a transfer-metrology application is very attractive while its generally unproven accuracy is inconsequential for this application. Whereas a novel approach to generating a calibration curve for a HRTEM/CD-SEM primary/secondary-metrology implementation has been proposed, the CD-SEM tool's tendency to deposit hydro-carbon contamination remains a central issue. Clearly, verifiable contamination-removal procedures have to be implemented. It appears that scatterometry-based OCD metrology is also feasible as a single traceable metrology for calibration because it is relatively inexpensive and, unlike HRTEM, is non-destructive to apply. However, the issue that the uncertainty of a local reference CD within the grating would be driven by the uniformity of the grating's features needs to be addressed by fabrication-process engineering. While it is not clear that CD-SEM metrology is ready to perform as a primary metrology for the subject application, it appears to be the only possibility for eliminating transfer metrology for the calibration of isolated lines. On the other hand, this project has proposed a test-structure innovation that would allow transfer a measurement of the average CD of a grating metrology to an isolated line. However, the proposed method has not yet been evaluated in the laboratory. Because 200 mm (110) starting material until recently has been unobtainable at an acceptable cost, this project's technical strategy has so far been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips. The scheme is shown in Fig. 2. The result is that finished units can be delivered at an acceptable cost. The Project's technical strategy is now evolving towards a monolithic-wafer implementation in response to industry pressure to make SCCDRMs more compatible with automated wafer-handling systems and related end-user requirements. These measures include:

- replacing the carrier-wafer with a monolithic 200-mm wafer implementation evolved from initial development with smaller diameter whole wafers,

- replacing the buried oxide of SOI wafers with a buried boron diffusion having an epitaxial silicon layer deposited over it or a heavy deep boron implantation prior to wafer etch,

- using electron-beam direct-write patterning of a silicon-nitride hard-mask film deposited on bulk-silicon wafers for pattern transfer from database to facilitate CD reduction to 20 nm

- adopting additional measures to further reduce the uncertainties of calibrated CDs to less than 1.0 nm,

- demonstrate SEM-deposited hydro-carbon contamination management by the implementation of verifiable contamination-removal procedures,

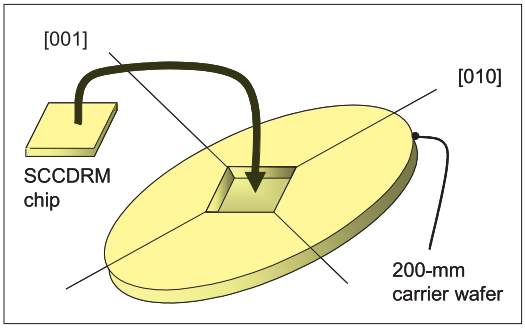

Figure 2. The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

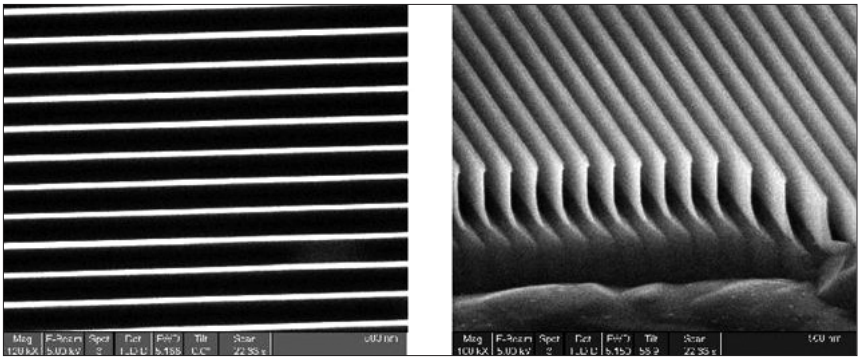

Figure 3. OCD grating section fabricated with SCCDRM technology which exhibits 36-nm lines at 180-nm pitch and having a height of 430 nm. The lithography was performed by collaborating UT-Austin staff using their direct-write e-Beam system.

- improving the reference feature's CD uniformity to enable certifying the CD of an extended length of reference feature,
- improved on-wafer navigation for end-user convenience,
- calibrating a selection of OCD gratings that are replicated at the same time as the isolated lines,
- improved management of the organic residues that sometimes impair the cosmetic appearance of the reference features and their environment on the wafer and to some extent adversely affect the uncertainty values of the delivered product, and
- evaluate a novel test structure concept to allow the extraction of isolated-line CDs from grating-based CD-metrology.

Implementing these aggressive strategic elements will continue to benefit from innovative teaming with other laboratories. Our strategy takes a page from the roadmap that explicitly states that standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials (ITRS) 2005 p. 36 under "Reference Materials." Likewise, the roadmap states that metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials (ITRS) 2007 p. 2 under "Scope". In response to this mandate, we have developed a unique relationship with the Microelectronics Research Center (MRC) at the University of Texas in Austin.

One of the products of our collaboration is the extraordinary OCD grating section shown in Fig. 3 which exhibits 36 nm lines at 180 nm pitch and having a height of 430 nm. The lithography in this case was done by with MRC'sJEOL direct-write e-Beam system.

DELIVERABLES:

- Apply electron-beam direct-write patterning of hard-mask films on whole wafers to enable replicated-CD reductions to 20 nm. 4Q 2008
- Evaluate buried boron-diffusion etch-stops or depositing an epitaxial film over a heavily deep-boron implanted silicon for enhancing the quality of SCCDRM reference features. 2Q 2009
- Repeat and refine the screening experiment to establish the optimum selection of combinations of pattern-transfer factors, including, for example, etch concentration and temperature, for driving down reference-feature uncertainties through CD-uniformity enhancement. 3Q 2009
- Design, fabricate, and evaluate innovative SCCDRM-based test structures that enable tracing the CDs of isolated lines from whole-grating measurements by OCD or SAXS, for example. 4Q 2009
- Document an appropriate scheme to manage hydro-carbon contamination which CD-SEM tools are observed to deposit. 4Q 2009,
- Implement and evaluate software to provide CD-roughness profiles and average CD from multiple-feature images to facilitate selection of isolated lines having superior qualities for use as reference features, 1Q 2009
- Investigate contribution of factors such as the roughness of the linewidths of hard-mask features to the quality of features replicated in SCCDRM processes. 3Q 2009

Accomplishments

■ The project thrust to fabricate reference features on whole wafers has produced first silicon. A hard mask film of 230 nm of silicon nitride was deposited by LPCVD on a selection of (110) wafers. After resist application, three were exposed in the NIST CNST E-beam system, two with a "rosette" pattern to enable identification of <112> vectors in the wafer surface, and one with a sub-100-nm reference-feature pattern. After hard-mask etch and resist strip, the hard-mask pattern was transferred to substrate silicon in a KOH solution to a depth of approximately 250 nm. Optical inspection of the rosette patterns successfully identified the alignment of the lattice <112> direction in the wafer surface to the wafer flats. These directions were readily evident in the two rosette

wafers through comparison of the flat-bottom trench width in silicon with the nitride trench widths. This information will ensure correct orientation of the reference-feature patterns relative to the flats on other wafers from the same ingot.

■ Although we are winding down the fabrication of SOI-chip-based SCCDRMs mounted in carrier wafers, some further effort has successfully been applied to the elimination of a troublesome process defect. This defect manifests itself as staining of the exposed buried-oxide field surfaces, which is bad enough in itself. Unfortunately, it is always accompanied by deterioration of the quality of replicated reference features, which often isn't apparent until quite late in the process cycle. The occurrence of the staining problem has always appeared unrelated to the process conditions. However, very recently we have discovered that a major factor is the length of time that the KOH solution is retained in the quartz reflux system. No adverse effects are observed for up to approximately two weeks, regardless of the usage of the solution. After that time elapses, the staining symptoms and the accompanying deterioration of the reference features becomes very evident. We have simply done an end-run around the issue by mixing a fresh KOH solution at least once a week. Since we started doing this, we have observed an unexpected benefit in a higher etch-survival rate of sub-30-nm features and also an indication of less CD-roughness.

■ Throughout this report, the importance of reducing the residual line-width roughness of SCCDRM features replicated in (110) silicon substrates has been stressed. We now believe that a major contributor to residual line-width roughness is the line-edge roughness of the corresponding hard-mask features. Therefore we have arranged for several chips to have extensive AFM metrology performed on their oxide hard-mask features. At the 50-nm average-CD level, the oxide-feature line-widths certainly exhibit CD variations amounting up to 20 nm more. It is highly likely that this hard-mask roughness is at least partially transferred to the replicated silicon reference features, the extent to which can be ascertained after KOH etching. If transference is found to occur, at least some effort will be diverted into hard-mask-feature CD-roughness control.

■ A new project thrust is collaboration with the Optical Physics Group at NIST responds to industry expressions of interest in acquiring SCCDRM-based standards to facilitate the development of, and monitor the performance of, OCD tools. This new CD-metrology medium is increasingly popular in the semiconductor- and mask-manufacturing communities. Suitable gratings have been co-fabricated on the same chips as the isolated-line reference features that are reported elsewhere in this document. The results of our continuing collaboration have been reported in two papers listed in the last section here, and a third paper has been accepted for an industry conference in August, 2008.

■ We commented above on the need to develop specialized image-processing software to rapidly extract CD-roughness profiles and average CD from multiple-feature images. A start on this mission has been made by comparing SEM- and HRTEM-CD measurements extracted from a wide selection of SCCDRM test-structures having feature line-widths ranging from 40 nm to 240 nm. Details are provided in a 2008 publication among those listed herein.

■ As mentioned above we have been investigating SAXS as an alternative primary metrology for calibrating the line-widths of SCCDRM features. In the next paragraph, we summarize the scope of our recent accomplishments with the University of Texas in Austin. During precursory research, we had earlier transferred our SCCDRM-fabrication process to facilitate a study of electron transport in silicide materials. Subsequently, UT-Austin had applied basically the same process to the fabrication of gratings, similar to that which has been shown in Figure 3 herein, for nano-materials research. We then asked for some of the gratings to be forwarded for SAXS-based CD metrology at the synchrotron at Argonne National Laboratory by staff of the NIST Polymers Division. Preliminary beam-line exposures were very encouraging. Based on the position of over 20 diffraction peaks that were observed, the pitch of the grating was determined to be 179.8 nm, a value very close to the specified value of 180nm. The X-ray data could not be modeled adequately with a grating model characterized by uniform lines having 0° sidewall angles. However, adding a trapezoidal bottoms to the vertical-sidewall trenches improved the fitting to some extent. This requirement is entirely consistent with known

properties of trenches etched in SCCDRM gratings. In addition, asymmetrical sidewall angles and variations in line-width, seemed to be needed to improve the fit of the observed diffraction patterns to those modeled. These observations are entirely consistent with known characteristics of gratings patterned by EB lithography in a mode susceptible to proximity effects and combined with slight off-axis sawing of the wafers from the ingot. Thus nano-scale geometrical anomalies of the properties of the gratings revealed by the SAXS metrology were credibly explained by orientation and processing issues that might not have been detected by any other means. In the end, SAXS metrology revealed that, with a simple rectangular line cross-section model, the height of the grating features was 490 ± 10 nm and their linewidth was 26.5 nm. Both values were very close to those extracted from SEM images.

■ Recently, the project published a comprehensive full-length report on the fabrication and calibration of SCCDRM Reference Materials entitled RM 8111: *Development of Prototype Linewidth Standard* in the NIST Journal of Scientific Research. Several other papers on special aspects of the fabrication and calibration, such as test-chip design, AFM metrology, and HRTEM imaging, were presented at the SPIE Spring Symposium of February, 2007, and the IEEE International Conference on Microelectronic Test Structures in March, 2007. A paper on the subject of etch-process optimization for uncertainty management was presented at the International Electron, Ion, and Photon Beam Technology and Nanofabrication Conference in June, 2006. A paper on the comparison of SEM-CD measurements and traceable-AFM CD measurements was published in an IEEE Transactions journal in January, 2008. An important first description of fabrication of SCCDRMs on 200 mm bulk wafers which was performed in collaboration with the Scottish Microelectronics Centre was presented at the *Frontiers of Characterization and Metrology for Nanoelectronics* in March 2007.

Collaborations

The project has been actively collaborating with the Microelectronics Research Center of the University of Texas at Austin (http://www.mrc.utexas.edu/amrc/publications.html), and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh in Scotland (http://www.see.ed.ac.uk/IMNS) Both these organizations operate the advanced wafer processing tools that we use to address the customer needs referenced in the sections above. Both institutions have highly skilled staff with both of which we have published recently. In the case of the University of Texas, our collaboration began with using the SCCDRM process to fabricate single-crystal test structures to facilitate a study of electron transport in nickel-silicide features. Since then, our collaboration has expanded into the MEMS arena and a ground-breaking study of the impact of nano-structure on the material properties of silicon, principally elasticity and related characteristics. Our interaction with the University of Edinburgh has recently focused on the fabrication of copper ECD test structures that take advantage of the properties of our SCCDRM technology. In addition, we have jointly published on two types of overlay standard, one of which uses a variant of the SCCDRM process.

We are interacting with the CAD and reticle staff the ISMI Subsidiary of SEMATECH, (http://ismi.sematech.org/) who have invited us to share space on a new reticle for their SVGL 193 nm Step-and-Scan lithography tool to fabricate an advanced generation of SCCDRMs for distribution to the member companies, as well as for possible calibration and distribution from NIST as SRMs.

We also interact regularly and closely with NIST's Physics, Materials Engineering and Information Technology Laboratories (http://www.mel.nist.gov/ and http://www.itl.nist.gov/) with whom we shared an intramural ATP program award to reduce the certified CDs and uncertainties of SCCDRMs through fabrication refinements.

Standards Committee Participation

Standards for Scatterometry Task Force (Michael W. Cresswell).

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen and Michael W. Cresswell).

Recent Publications

B. J. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. Gundlach, L. I. Haworth, A. W. Ross, and A. J. Snell, IEEE International Conference on Microlectronic Test Structures, March 19-22, 2007, Tokyo, Japan, page 165.

E. Kenyon, M. W. Cresswell, H. Patrick, T. A. Germer, *"Modeling the Effect of Finite Size Gratings on Scatterometry Measurements,"* Proceedings of SPIE Advanced Lithography, SPIE Advanced Lithography, February 24-29, 2008, San Jose, California, 8 pp. (25-FEB-2008)

R. A. Allen, W. F. Guthrie, C. E. Murabito, R. G. Dixson, A. Hunt, *"Comparison of SEM and HRTEM CD Measurements Extracted from Test-Structures Having Feature Linewidths from 40 nm to 240 nm,"* IEEE Trans. Instrum. Meas., Vol. 57, No. 1, pp.100-109 (01-JAN-2008)

B. Li, M. K. Kang, K. Lu, R. Huang, P. S. Ho, R. A. Allen, M. W. Cresswell, *"Fabrication and Characterization of Patterned* Single-Crystal Silicon Nanolines," NANO Letters, Vol. 8, No. 1, pp.92-98 (07-DEC-2007)

R. A. Allen, R. Dixson, M. W. Cresswell, W. Gutherie, B. J. Shulver, A. S. Bunting, J. T. Stevenson, and A. Walton, *"CD Reference Materials Fabricated on Monolithic 200 mm Wafers for Automated Metrology Tool Applications,"* 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, Mar 27-29, 2007, Gaithersburg, MD (01-SEP-2007)

R. A. Allen, H. J. Patrick, M. Bishop, T. A. Germer, R. Dixson, W. F. Guthrie, and M. W. Cresswell, *"Study of Test Structures for Use as Reference Materials for Optical Critical Dimension Applications,"* ICMTS IEEE International Conference on Microelectronic Test Structures, April 4-8, 2007, Tokyo, Japan.

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Smith, A. J. Snell, J. M. Stevenson, A. Walton, M. W. Cresswell, R. A. Allen, *"Extraction of Sheet Resistance and Linewidth from All-Copper ECD Test-Structures Fabricated from Silicon Preforms,"* 2007 International Conference on Microlectronic Test Structures, pp.14-19 (22-MAR-2007)

C. Nwokoye, M. E. Zaghloul, M. W. Cresswell, R. A. Allen, C. E. Murabito, *"A New Critical Dimension Metrology for Chrome-on-Glass Substrates Based ons-Parameter Measurements Extracted from Coplanar Waveguide Test Structures,"* SPIE, Bay Area Chrome Users' Symposium, September 18-22, 2006, Monterey, California, 12 pp. (01-OCT-2006)

M. W. Cresswell, W. Gutherie, R. Dixon, R. A. Allen, C. E. Murabito, J. V. Martinez, *"RM 8111: Development of a Prototype Linewidth Standard,"* Journal of Research (NIST JRES), Vol. 111, No. 3, pp.187-203 (01-MAY-2006)

B. Li, L. Shi, P. S. Ho, J. Zhou, R. A. Allen, M. W. Cresswell, *"Test Structures for Study of Electron Transport in Nickel Silicide Features with Linewidths between 40 nm and 100 nm,"* IEEE ICMTS International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.18-23 (01-APR-2006)

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Snell, J. M. Stevenson, A. J. Walton, R. A. Allen, M. W. Cresswell, *"Design and Fabrication of a Copper Test Structure as a Electrical Critical Dimension Reference,"* Proc., IEEE International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.124-129 (01-APR-2006)

JEDEC Standard JESD202, *"Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress,"* March 2006. (Written by H. A. Schafft).

A. E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, and D. L. Blackburn, *"Implementation of Simulation Program for Modeling the Effective Resistivity of Nanometer Scale Film and Line Interconnects,"* NISTIR 7234, February, 2006.

Wafer-Level and Overlay Metrology

Goals

Provide technological leadership to semiconductor and equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily optical based methods used in overlay metrology and optical, wafer level critical-dimension (CD) metrology.

Customer Needs

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high throughput, higher resolution metrology tools, which enable more dense sampling strategies has lead to a comprehensive program at NIST to both support and advance the optical techniques needed to make these high throughput overlay and photomask/wafer critical dimension measurements (see Fig. 1).

Technical Strategy

The main technical thrust areas are overlay calibration techniques and standards, new advanced wafer level target designs, and research into new methods for measuring overlay. The strategic components of the project follow.

1. The development of calibration methods and calibrated overlay structures is one of the primary goals of the project. The technical strategy for calibrated overlay metrology is divided into two components: (a) instrumentation development and the advance of overlay metrology calibration techniques, and (b) the design and calibration of test patterns and standard artifacts. NIST has developed an overlay metrology tool that has undergone extensive development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is now used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. Since pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane, particular concern is placed on ensuring accurate optical measurements through a large depth of focus. Any misalignment in the overlay metrology system will translate into an overlay offset error, referred to as tool induced shift (TIS). Additionally, there are residual errors caused by asymmetries in the targets known as wafer induced shift (WIS).

Technical Contacts:
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R. Allen

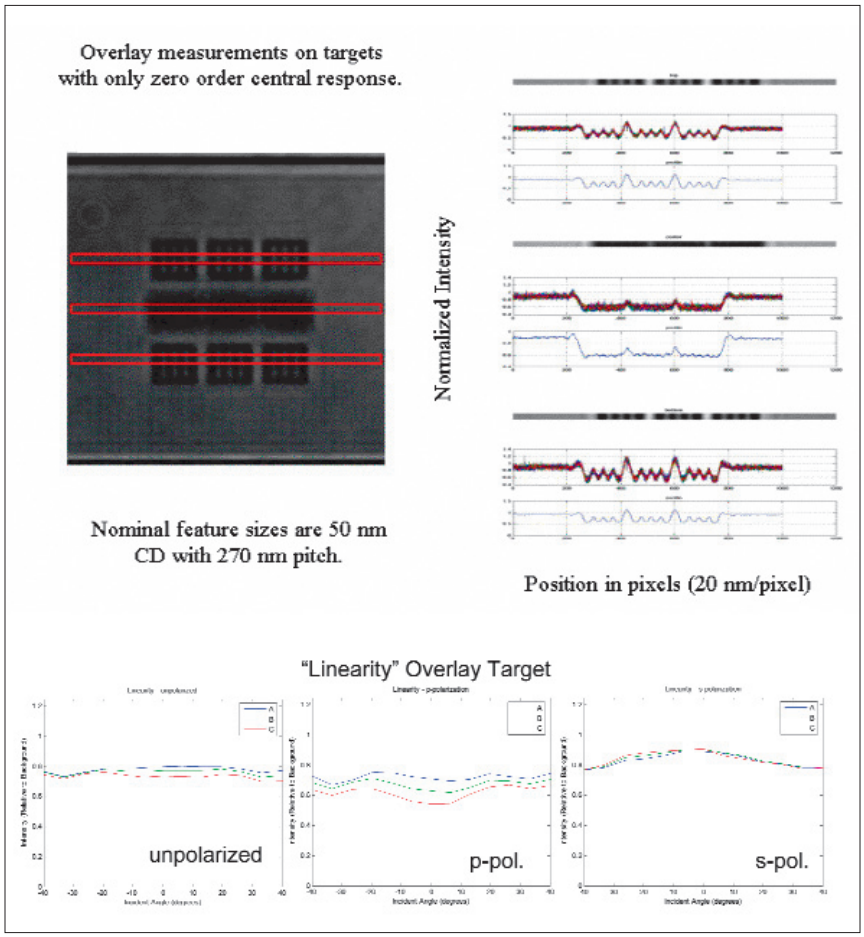

Figure 1. Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in multiple sections of Tables Met 3a and b of the 2007 ITRS as a difficult challenge for both >32 nm and <32 nm processes. Overlay measurements have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table Met 3a shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table Met 3b, the problems are more acute for long term CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

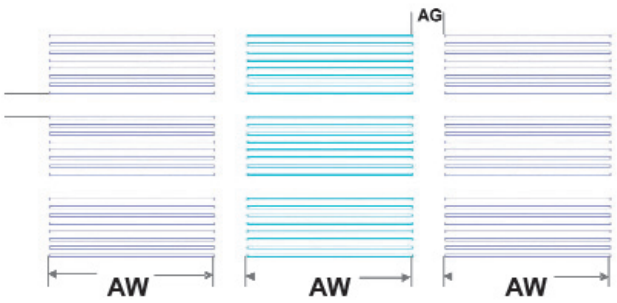

Figure 2 (a)

- Two sets of targets:
  1) This shows equal lines and spaces.
  2) A similar set of targets but with different linewidths for each group of 8 lines. The linewidths span typical process variation windows.
- AW = 2.5 um and 5.0 um
- AG = 1.0 um
- 5 different pitches and 3 offset values: 0, +/-10 nm

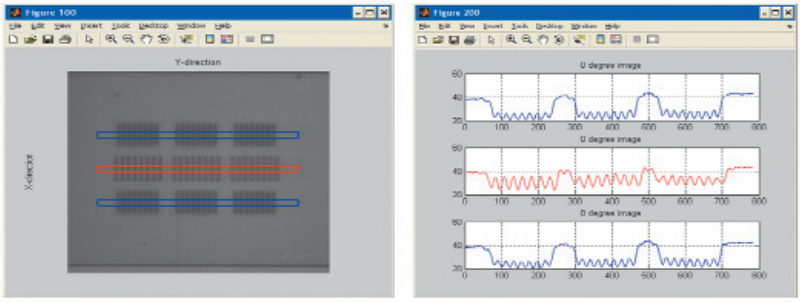

Figure 2 (b)
LITO
90nm 1:3

Figure 2. A schematic of the target designs is shown in (a). This is one example of several variations of this design. The lower part of the figure shows an image and a set of profiles for a target which reflects higher-order optical content.

A set of standard artifacts and alignment procedures, developed at NIST and published, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay measurements. The NIST metrology system used for this is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high resolution image capture with a full field CCD data acquisition system which has been fully characterized and calibrated. This instrument has been used for detailed analysis of CCD array performance and characterization with several CCD acquisition systems evaluated. Many of the techniques developed in the advanced optical imaging section below have been implemented on this tool as well, such as structured illumination and system characterization to enable improved calibrations.

Standard overlay artifacts have been fabricated and calibrated in 200 mm and 300 mm wafers that are now available as SRM 5001. These overlay artifacts are for the calibration of industrial overlay metrology tools, although they have also been used for the calibration of atomic force microscope (AFM) or SEM reference metrology systems. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for an example, Fig. 2.

We have also developed a series of new overlay targets and linewidth targets intended to enable the measurement of overlay and linewidth with device sized features. One variation of these targets allows in-chip structures to be placed throughout the active area of a die. These results have been published and collaborative work is progressing to develop the commercial applications to measure overlay using device-sized features in targets optimized to be the smallest overall dimension. There is a second flavor of in-chip targets, as shown in Fig. 3, that are arrayed targets composed of device-sized features.

DELIVERABLES:

- Implement full optical illumination and collection path characterization and normalization to achieve improved measurement accuracy. Use these techniques to comprehensively evaluate illumination homogeneity errors and intensity/wave front errors for both illumination fields and collection optics. 3Q 2008

- Use the OMAG 4 metrology wafers from the SEMATECH collaboration to develop reference metrology for overlay calibration and wafers. Work with SEMATECH and the Advanced Metrology Advisory Group (AMAG) to develop a new set of calibration structures and techniques for reference metrology in support of the calibration of industry tools. 1Q 2009
- Work with SEMI and SEMATECH to evaluate and identify a new set of target designs for specification as overlay metrology standards. This new specification is focused on identifying a domain of standardization for overlay target designs to enable calibration and standardization in the realm of numerous proprietary overlay target designs. 2Q 2009

Optical modeling is an essential tool for enabling improved optical overlay measurements. Modeling the effects of relevant feature properties and optical instrument characteristics using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 4. NIST has a world class effort in optical modeling that includes the comprehensive comparison of two rigorous coupled wave guide scattering models, a finite difference time domain-based model and a Maxwell integral equation solver. Two of the models are developed in house and form the basis of our critical dimension and overlay simulation tools.

DELIVERABLES:

- Compare and advance the accuracy of the electromagnetic scattering models as exercised in challenging line width evaluation. Complete a comprehensive theory to experiment comparison for a range of CD values with improved agreement primarily through accurate instrument normalization, characterization, and alignment. Publish results for the semiconductor industry. 4Q 2008
- Evaluate through-focus focus-metric techniques for improved illumination homogeneity and alignment. Compare experimental results with modeling results and publish results. 2Q 2008

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This methodology has demonstrated the possibility of using optical methods for line width and overlay metrology with targets composed of features smaller than 30 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. The technique is

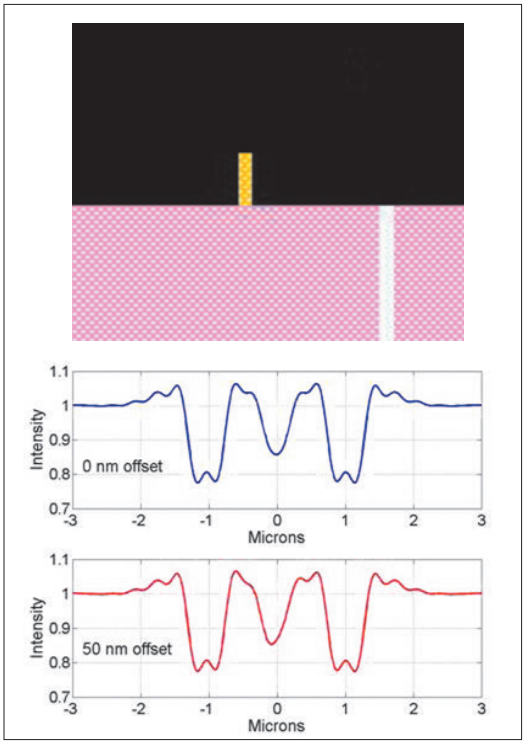

Figure 3. New overlay targets, which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.

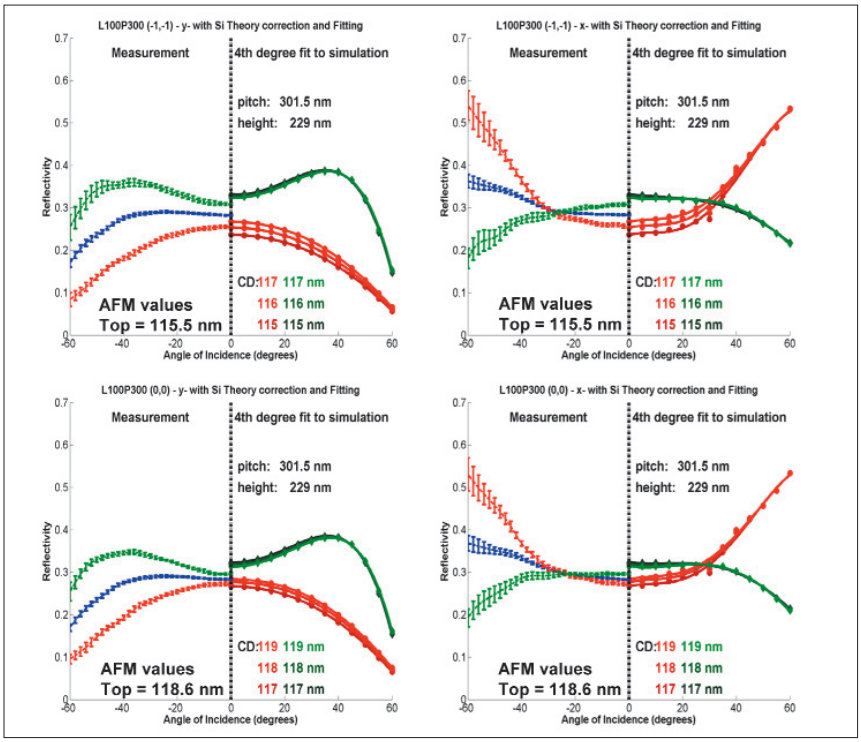

Figure 4. Quantitative parametric modeling results demonstrate consistent agreement on the nanometer scale with AFM reference metrology. More comprehensive data published recently show that nanometer scale sensitivity measurements can be achieved using angle resolved microscopy for nominally 100 nm sized lines and pitches of 300 nm.

well suited for high-resolution microscopy of metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods that can be suitably applied to device-sized features and advance the extensibility of high throughput optical metrology methods. Current metrology requirements are demanding higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques are now viewed as potential solutions to these significant metrology challenges. As a part of this project, we have constructed a new optical tool specifically intended to make this type of scatterfield measurement with structured illumination that controls the frequency content of the illumination fields and of the scattered fields. Figure 5 shows an example controlling the frequency content of a sub-resolution overlay target. This effort includes comprehensive optics modeling as well as a new optical configuration designed in-house. The optical design work includes a thorough examination of illumination effects and accurate methods to prepare optical illumination fields.

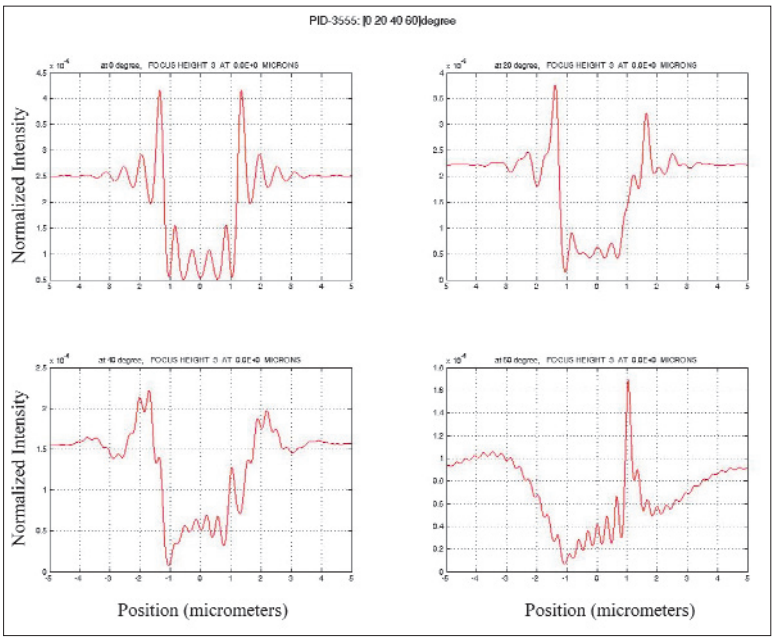

Figure 5. The different panels show the image as a function of illumination angle. The vertical axes are normalized intensity and the horizontal axes are lateral position in micrometers. At the high illumination angles, the higher order diffraction orders are rocked into the collection optics. A dipole or alternative illumination can yield symmetric profiles or overlay which otherwise would show zero order response.

In this effort we are now constructing a 193 nm wavelength optical instrument that has been designed in house. This new tool will provide a flexible architecture for overlay and CD measurements on a high throughput capable platform. The new design creates a large conjugate back focal plane where a range of scanning and illumination control techniques can be applied. The optics have been custom designed and manufactured to NIST specifications with the appropriate 193 nm coatings. The new laser system and optics are housed in a clean room environment and using a new embedded structural design with superb vibration and temperature control, the ultimate performance in a state of the art optical system is the goal.

DELIVERABLES:

- Develop a comprehensive set of techniques to accurately align and measure the optical illumination fields using the scatterfield scanned illumination approach. Acquire comprehensive angle resolved data. Develop. 3Q 2007
- Develop the capability to measure dense features which are smaller than 30 nm CD. Demonstrate the sensitivity to 1 nm changes in linewidth for densely positioned silicon structures, and develop modeling techniques for the accurate interpretation of measurements. 2Q 2008
- Operate the 193 nm optical tool with the full optical configuration in place. Use visible light for alignment and demonstrate performance with the 193 nm laser. 4Q 2008

3. A final element of this project is development of hybrid electrical-optical test structures to provide a validation between in-line optical metrology and actual device performance. These test structures would not displace in-line metrology, but rather will compliment it; providing a tool to evaluate in-line techniques.

DELIVERABLES:

- Complete initial evaluation of test structure using electrical and AFM metrology. 3Q 2008
- Investigate intercomparison of electrical metrology with optical metrology. 4Q 2008

Accomplishments

■ "Nanotech Briefs' Nano 50" Awarded to Scatterfield Microscopy Project. The Scatterfield competence was recognized with this respected award with a citation for the development of a revolutionary measurement technique capable of extending conventional optical metrology instrumentation well beyond their current limits.

■ Patent Applied for on "Zeroeth Order Imaging" method. This new approach combines standard edge-based imaging with signature-based methods. Only the local zero order scattered light is imaged as a function of illumination angle. Based on simulations, the method is extensible to the sub-20 nm domain.

■ Patent Applied for on "Super resolution overlay targets". Joint NIST/SEMATECH patent has been formally applied for on the new super-resolution overlay target, which has the potential to change the target designs and methodology widely used by the industry.

■ Several other invention disclosures submitted during this competence. Through-focus focus-metric analysis and imaging have lead to enhanced image technology using information from multiple focus planes. New target designs and optical imaging methods also submitted.

■ Quantitative agreement achieved between rigorous modeling and experimental data. Published results demonstrating quantitative agreement for scatterfield measurements of densely arrayed 100 nm sized lines which vary in 1 nm increments. This theory to experiment agreement was previously not achievable. This was accomplished by accurate optical characterization/normalization without tunable parameters.

■ Comprehensive development and comparison of NIST electromagnetic scattering models and industry models completed. Researchers in the optical scatterfield competence have both developed and compared model-based simulation results with excellent agreement. Two industrial scattering models as well as the NIST-developed integral Maxwell equation solver and the NIST-developed RCWA model were all compared.

■ New approach to evaluation of optical illumination homogeneity, alignment and aberrations developed. This new approach enables evaluation and accurate characterization of optical aberration and illumination homogeneity of the illuminating fields in bright field microscopes, essential to making accurate optical measurements. The angle-resolved, engineered illumination is essential to accurate characterization.

■ Engineered dipole illumination to control optical image content for overlay metrology was demonstrated in image-based measurements. Leading metrology tool makers are now implementing this approach. Additionally, the through-focus focus-metric technique was used to demonstrate nanometer sensitivity to features in silicon. The technique of sampling scattered fields through focus for CD measurement and optical system alignment has been implemented internationally. Applications are for less dense features.

■ The overlay microscope has been converted to scatterfield scanning design. The existing optical overlay instrument has been enhanced with illumination control for improved data acquisition and tool alignment. Techniques for alignment and imaging implemented.

■ Fully operational new scatterfield optical microscope. The new 450 nm illumination scatterfield microscope has been completed. This is the first optical tool developed ground up at NIST specifically for the purpose of using illumination engineering and structured target designs. The centerpiece of the microscope is the open architecture of the illumination and collection paths. A second generation design has also been implemented. Spatial light modulators have been used to control illumination. The instrument was also used for back focal plane imaging using the scatterfield based illumination configuration. These results were published.

■ 193 nm Optical Tool under construction. The major mechanical systems and most optical train components for the new 193 nm optical metrology instrument are now being assembled in the facility. A custom designed air

table is being used as the mechanical structure and is expected to yield the highest structural rigidity and thermal stability for a NIST designed optical microscope. This new tool uses fused silica optics, a catadioptric objective and is placed in a custom clean room with advanced safety measures.

■ SEMATECH Tech Transfer document highlighted work from NIST optical research staff. A recent document "Summary of 2006 NIST/SEMATECH Studies of Next Generation Overlay Metrology" authored by SEMATECH highlighted a number of recent advances by the Scatterfield competence project. The report details collaborations between NIST, SEMATECH and the semiconductor industry.

■ NIST Competence Program staff has met with several leading optical metrology tool manufacturers regarding recent advances in scatterfield microscopy. The companies include among others KLA-Tencor, Nanometrics, Soluris, Nova and Applied Materials. Metrology instrument makers are now adopting and implementing various elements of the scatterfield optical design. Scatterfield researchers are now funded to develop nanomanufacturing applications for fuel cell production.

■ SEMATECH contract also awarded to evaluate overlay metrology applications of scatterfield microscopy. External funding from SEMATECH member companies to research scatterfield applications for high resolution optical overlay measurements. Report submitted to SEMATECH on contract to investigate defect metrology applications of scatterfield microscopy. Scatterfield competence researchers completed the first round of comprehensive simulations to investigate applications of Scatterfield microscopy to patterned defect inspection. SEMATECH subsequently funded a second round of contracted research.

■ NIST scatterfield researchers delivered report on optical critical dimension (OCD) limits investigation. NIST researchers are currently funded by SEMATECH to investigate fundamental limits of optical critical dimension measurement techniques. The NIST world class modeling capabilities are being applied to scatterfield and scatterometry optical methods. The MEL/Physics collaborative report involved extensive simulation and analysis of structures in silicon as small as 7 nm in size.

Collaborations

SEMATECH, IBM, Intel, KLA-Tencor, Nanometrics, Applied Materials, Motorola, AMD, and several other leading manufacturers and tool vendors.

University of Edinburgh.

Publications

R. M. Silver, B. Barnes, R. Attota, A. Heckert, and R. Dixson, *"Angle Resolved Optical Metrology,"* Proc. SPIE Advanced Lith., Feb. 2008.

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H. Patrick, R. Attota, B. Barnes, T. Germer, R.G. Dixson, M. Stocker, R. M. Silver, and M. Bishop, *"Optical Critical Dimension Measurement of Silicon Grating Targets using Back Focal Plane Scatterfield Microscopy,"* accepted, J Micor/Nanolith., MEMS and MOEMS 7(1), 0137011, 2007.

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R. M. Silver, R. Attota, and E. Marx, *"Model-based Analysis of the Limits of Optical Metrology with Experimental Comparisons,"* Proc. SPIE Germany, Vol. 6617, p. 6617OW, June 2007.

B. J. R. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. T. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. M. Gundlach, L. I. Haworth, A. W. S. Ross, A. J. Snell, *"Array*

Based Test Structure for Optical-Electrical Overlay Calibration," Microelectronic Test Structures, 2007, ICMTS'07, IEEE International Conference, pp. 165-170 (March 2007).

R. M. Silver R. Attota, B. Barnes, and H. Zhou, *"Theoretical Evaluation of Scatterometry for Overlay Applications,"* SEMATECH Tech Transfer Doc, Feb. (2007).

R. M. Silver, T. Germer, R. Attota, B. Barnes, B. Bunday, J. Allgair, E. Marx, and J. Jun, *"Fundamental Limits Optical Critical Dimension Metrology: A Simulation Study,"* SPIE Proc. Feb. Vol. 6518 (2007).

Front-End Processing Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The current gate stacks, poly silicon over SiO_2 and SiON dielectrics, are being replaced by high-κ metal gate stacks. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology, and overall reliability metrology.

Wafer and Chuck Flatness Metrology

Goals

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project provides measurement and technology infrastructure to support the measurement of wafer thickness variation of 300 mm silicon wafers, and surface flatness of chucked wafers.

Customer Needs

With the evolution of exposure tools for optical lithography towards larger numerical apertures, the semiconductor industry expects continued demand for improved wafer flatness at the exposure site. The allowable site flatness for 300 mm wafers is expected to be less than 45 nm by 2010 and it may be as low as 25 nm by 2015 according to the International Technology Roadmap for Semiconductors (ITRS 2006). This requires wafers with low thickness variation and presents a challenge for both wafer polishing and metrology tools, which must be capable of meeting the specifications. We are addressing the need for standard 300 mm wafers with calibrated thickness variation with the Improved Infrared Interferometer (IR3) at NIST. The interferometer is used for independent, traceable wafer thickness calibrations, which enable manufacturers of wafers and wafer metrology instruments to certify the performance of their metrology instruments. In addition, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometeR" (XCALIBIR).

Technical Strategy

1. The Improved Infrared Interferometer (IR3) was developed at NIST for the characterization of the thickness variation of silicon wafers with diameters up to 300 mm. The IR3 interferometer is an infrared phase-shifting interferometer, operating at a wavelength of 1550 nm which measures the thickness of low-doped silicon wafers up to 300 mm diameter in a single measurement (see Fig. 1 and Fig. 2). The interferometer may be used in several configurations with collimated and spherical test wave-fronts. The collimated wave-front mode is the current focus of the project. In this method, the planar infrared wave-front is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wave-fronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation.

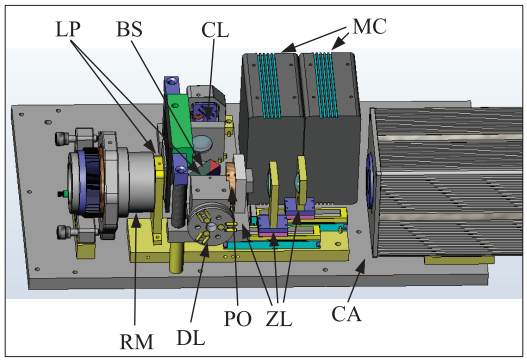

Figure 1. Solid model of NIST's improved infrared interferometer (IR3). The main components of the interferometer are indicated: collimator lens (CL), polarizing beam splitter (BS), λ /4-plates (LP), reference mirror for the Twyman-Green mode (RM), diverger lens (DL), polarizer (PO), zoom lens (ZL), motion controllers for the zoom lens (MC), and camera (CA). The size of the base plate is approximately 20 cm × 30 cm.

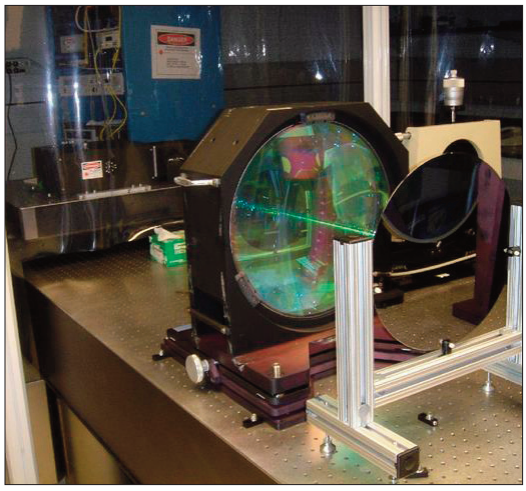

Figure 2. Test arm of the IR3 interferometer. shown are the collimator lens and the beam expander together with a 300 mm silicon wafer. The insensitivity of the measurement to vibration permits the use of a simple wafer mount.

Technical Contacts:
U. Griesmann
Q. Wang
J. Soons

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer thickness metrology has led to unprecedented levels of thickness correction on industry standard 300 mm Si wafers, when combined with deterministic finishing technologies such as MRF. The collaboration with NIST has been a significant and crucial component to the success of this effort."
Paul Dumas and Marc Tricard
QED Technologies –
A subsidiary of Cabot Microelectronics Corp,
Rochester, NY

DELIVERABLES:

- Develop methods for the thickness calibration of thin wafers with thickness below 500 µm. 4Q 2008
- Provide calibrated 200 mm silicon wafers. 4Q 2008

2. Measurements of the flatness of chucked wafers are made with XCALIBIR, a general purpose, 300 mm aperture phase measuring interferometer operating with visible light at 633 nm. The interferometer is housed in a clean room, which eliminates dust particles between chuck and wafer. The results are used to evaluate the influence of wafer-chuck interactions on the chucked wafer flatness.

Accomplishments

■ IR3 has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes, and the spatial resolution of the detector was doubled to 2 pixels/mm. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty. In addition, a new laser with wide tuning range will make it possible to measure very thin wafers. The optical components in the IR3 interferometer were improved to reduce the measurement noise. Wavelength phase-shifting has been implemented and a TTV map repeatability of 5 nm peak to valley has been achieved for 300 mm wafers. The IR3 interferometer is now housed in a clean room, which enables us to make calibration measurements of wafers supplied by industry customers.

■ The flatness of 200 mm and 300 mm diameter wafers on pin chucks was explored using the XCALIBIR interferometer in a collaboration with Wavefront Sciences Inc., Albuquerque, NM.

■ IR3 was used to develop a sub-aperture magneto-rheological polishing process for the finishing of 300 mm wafers with ultra-low thickness variation in collaboration with QED Technologies. Figure 3 shows that a total thickness variation (TTV) of about 40 nm could be achieved. The Square focal plane range square focal plane range (SFQR) resulting from the thickness variation (assuming an ideal chuck) is shown in Fig. 4. These results demonstrate that a suitable sub-aperture finishing process can achieve the exposure site flatness expected by the ITRS for 2015.

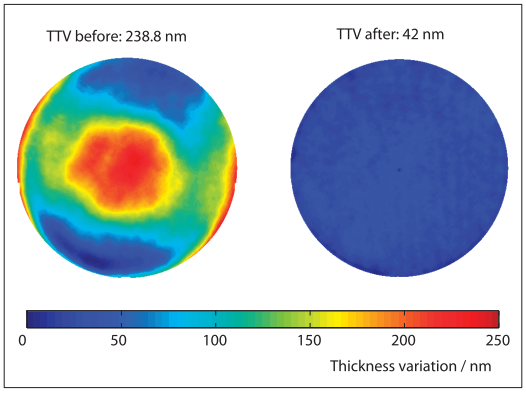

Figure 3. Wafer thickness variation of a 300 mm silicon wafer before and after sub-aperture polishing. The total thickness variation was reduced from 238 nm to 42 nm over a 292 mm aperture (4 mm edge exclusion).

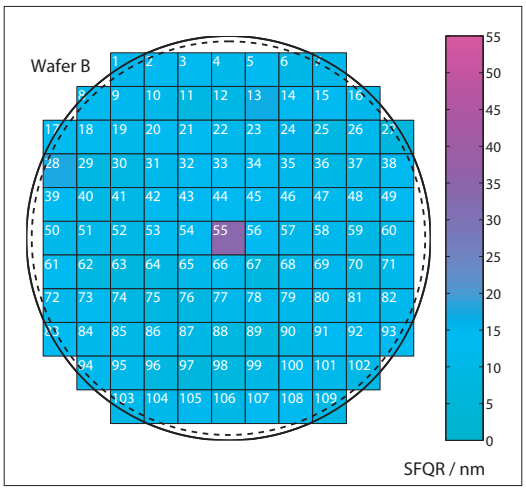

Figure 4. SFQR of the wafer shown in Fig. 3 after sub-aperture finishing for 25 mm x 25 mm sites with the same edge exclusion (4 mm) as in Fig. 3.

Collaborations

During the course of this project, we have interacted with several companies on problems relating to wafer flatness metrology and chucked wafer flatness.

WaveFront Sciences: Flatness measurements of free form and chucked wafers for the validation of a metrology tool developed by WaveFront Sciences.

MEMC Electronic Materials: Wafer thickness standard development.

Siltronic: Wafer thickness standard development.

Intel: Development of very thin silicon thickness standards.

QED Technologies: Development of ultra-flat 300 mm silicon wafers.

Lumetrics: Evaluation of Lumetrics thickness gauging technology for wafer thickness metrology.

Publications

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T. L. Schmitz, A. Davies, C. J. Evans, and R. E. Parks, *"Silicon wafer thickness variation measurements using the National Institute of Standards and Technology infrared interferometer,"* Opt. Eng. 42, 2281-90 (2003).

Modeling, Measurements, and Standards for Wafer Inspection

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in tow sub-sections, each focusing on a single aspect. These are:

- Modeling and Measurements for Wafer Inspection
- Nanoparticle Size Characterization and Standards Development

Modeling and Measurements for Wafer Surface Inspection

Goals

Our goals are: (1) to provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces; (2) to develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS); and (3) investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, non-metallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem currently exist for particles on bare silicon, on non-metallic films, and on wafer backsides, while it is anticipated that no acceptable solutions will exist for metallic films in 2010. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards in-situ sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by 13 different Scanning Surface Inspection System (SSIS) indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other particles sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. The SIA roadmap specifies the need for accurate calibration particles to size critical semiconductor components scaling to 32 nm or smaller by as early as 2008.

Technical Strategy

There are two major strategies for improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be using to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size, especially on rougher surfaces.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The tech-

Technical Contacts:
T. A. Germer

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us.
This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.
VLSI Standards, Inc.

nical focus of our future work will be applying DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) on 300 mm wafers (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLES:

- Publish results of measurements performed using 266 nm from various films to assess the particle detection limits on those films. 4Q 2008

2. Theoretical Light Scattering Calculations – The focus of our theoretical work is on: (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

DELIVERABLES:

- Develop model for scattering by tetrahedral pits beneath a surface. 3Q 2008

3. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle diameters as small as 50 nm. However, discrepancies have been noticed between PSL measurements using DMA, and measurements using light scattering on the surface of a wafer. These discrepancies are possibly due to the PSL particles deforming on the bottom as they adhere to the wafer. This problem will be investigated by comparing measurements of the PSL particles to measurements of silica particles, which are less likely to deform when they contact the wafer surface. Measurements will be performed using both the DMA and light-scattering instruments.

DELIVERABLES:

- Lead industry intercomparison of reference sphere deposition standards. 4Q 2008

4. Resource on Particle Science – Over the past five years, the particle-related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES:

- Provide technical support to the SEMI Advanced Surface Inspection task force. 4Q 2008

Accomplishments

■ Completed and certified the measurements for new NIST Standard Reference Materials (SRM). Measured and certified SRM 1964, particles with

a nominal diameter of 60 nm. Also measured and certified SRM 1963a, with a nominal diameter of 100 nm, to replace the previous 100 nm SRM 1963, which was corrupted due to agglomeration. SRM 1963a and SRM 1964 are currently available for purchase.

■ Completed initial screening process and preliminary measurements for development of a 30 nm SRM. Identified primary and secondary candidate samples for the 30 nm SRM, based on diameter and distribution measurements. Researched measurement uncertainty for particles smaller than 50 nm and devised strategies for reducing the uncertainty.

■ Developed and improved the NIST Calibration Facility, which uses Differential Mobility Analysis for sizing monodisperse spheres in the size range of 50 nm to 400 nm. Reduced the expanded uncertainty to 1.0 % of the particle size by correlating the slip correction to the measured particle size. Increased resolution and accuracy of measurements through improved equipment and intermediate measurements.

■ Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

■ Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

■ In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

■ Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

■ Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 4200 copies of the library have been downloaded from the web. The Modeled Integrated Scatter Tool (MIST), a Windows application for calculating integrated scatter, was released in June 2004.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by the uncertainty in the shape of the particle on the surface. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

■ Assisted in revising SEMI M53, a practice for calibrating scanning surface inspection systems, by developing a model-based calibration scheme that matches measured signals from PSL spheres to the predictions of a theoretical model. The accepted

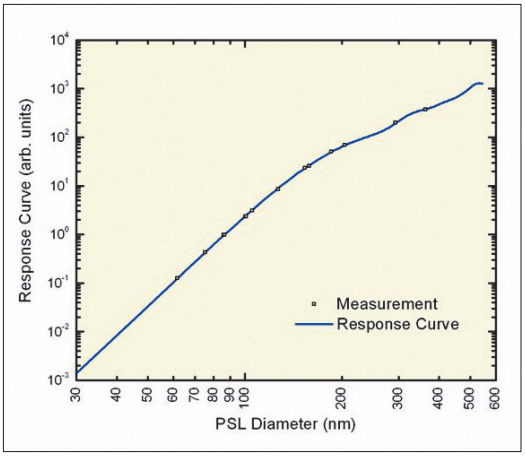

Figure. 2. Sample calibration of a commercial wafer scanner using the new SEMI M53 method. The relative expanded uncertainty in particle diameter has been reduced to less than 1 %.

model for scattering by the spheres is specified in the standard as that provided by the MIST program. The new method has several advantages over the previous method, including: less sensitivity to changes in availability of specific size standards, improved accuracy, less variability between instruments, and an ability to extract a quantitative accuracy from the calibration. The expanded uncertainty found by applying the calibration to a commercial instrument was better than 1 % of the diameter.

Tested the use of silica spheres as a substitute for PSL spheres for calibrating scanning surface inspection systems. PSL spheres exhibit degradation upon repeated ultraviolet exposure, and more inspection tools are using ultraviolet wavelengths. The silica spheres were found to yield comparable calibrations, provided that they are classified with a PSL-sphere-calibrated classifier to reduce their size distribution. The index of refraction of the silica spheres was a byproduct of the measurements and are needed for the calibration.

Collaborations

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

T. A. Germer, C. Wolters, and D. Brayton, *"Calibration of wafer surface inspection systems using spherical silica particles,"* Optics Express 16 (7), 4698–4705 (2008).

T. A. Germer, *"Modeling the effect of line profile variation on optical critical dimension metrology,"* in Metrology, Inspection, and Process Control for Microlithography XXI, Proc. SPIE 6518, 65180Z (2007).

T. A. Germer, *"Effect of line and trench profile variation on specular and diffuse reflectance from a periodic structure,"* J. Opt. Soc. Am. A 24 (3), 696–701 (2007).

M. K. Donnelly, J. C. Yang, *"Screening Candidates for 30 nm Spheres,"* NISTIR 7345, August 2006.

G. W.Mulholland, M. K. Donnelly, C. Hagwood, S. R. Kukuck, and V. A. Hackley, *"Measurement of 100 nm and 60 nm Particle Standards by Differential Mobility Analysis,"* J. Research NIST 111, 257–312, 2006.

Thomas A. Germer, *"Measuring Interfacial Roughness by Polarized Optical Scattering,"* in Light Scattering and Nanoscale Light Scattering, A.A. Maradudin, Ed., (Elsevier, New York, 2007) Chapter 10, pp. 259–284.

Nanoparticle Size Characterization and Standards Development

Goals

Our goals are: (1) perform research and measurements in support of developing nanoparticle size standard reference material (SRM); (2) develop facilities to accurately measure nanoparticle size and to deposit monosize particles on calibration artifacts, in order to reduce the uncertainty in the sizes of particles used by the semiconductor industry; and (3) provide industry with measurements and standards in order to improve the inspection of wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potential show-stopping barrier to device miniaturization. The SIA roadmap specifies the need for accurate calibration particles to size critical semiconductor components, scaling to 32 nm or smaller by as early as 2009. As devices become miniaturized, the need to detect smaller defects has caused the costs of inspecting wafers to skyrocket. Accurate reference particles are needed to develop and advance the systems for high throughput and cost effective wafer production, which is crucial for device miniaturization.

This project is developing a NIST SRM, which can be used by manufacturers as reference for comparing specifications of particle contamination. The standard reference particles are used for calibrating nanoparticle sizing equipment, and are particularly critical for calibrating Scanning Surface Inspection Systems (SSIS) used to detect and characterize defects on silicon wafers. A recent comparison of the measurements of calibration wafers by 13 different SSIS indicated unacceptably large deviations between the SSIS results and the actual particle sizes. In some cases, the SSIS underestimated the particle size by as much as 8 %. The availability of accurately sized standard reference nanoparticles will allow for calibration of SSIS equipment for better wafer inspection. The reference particles may also be used for supplying monosize particles for testing aerosol instruments, and for examining aerosol kinetics and evaluating particle detector response.

By 2009, at the 50 nm node, particles having diameters 20 nm must be detectable on bare silicon and nonmetallic films, with 48 nm on metallic films. No known solutions exist at this time. [2007 ITRS, Yield Enhancement, Table YE7a]

Semiconductor Industry Association. International Technology Roadmap for Semiconductors (ITRS): 2007 Edition, http://public.itrs.net

Technical Strategy

A major focus for this project has been the development of the differential mobility analysis (DMA) method for accurately sizing nanoparticles. Compared to other methods, such as light scattering or electron microscopy, differential mobility analysis has lower uncertainty for measuring small particles and offers good statistics. The technical focus of our future work will be applying the DMA (see Fig. 1) for accurately sizing standard reference calibration particles as small as 30 nm. We will develop methods for generating other types of monosize particles in the nanoparticle size range, and address issues for reducing the uncertainty of nanoparticle measurements.

Specific project elements are defined below:

1. Development of 30 nm SRM – Differential mobility analysis has been used to make accu-

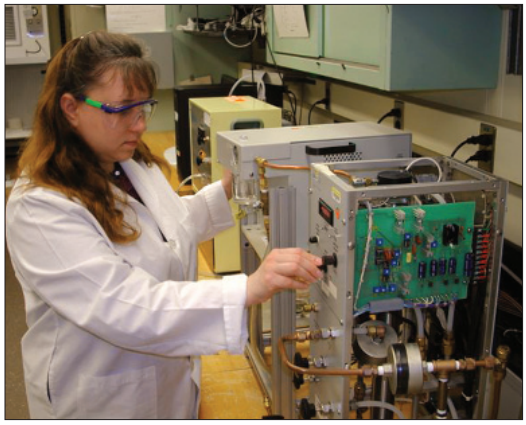

Figure 1. DMA Tool Setup.

Technical Contacts:
M. K. Donnelly
J. C. Yang

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.
VLSI Standards, Inc.

rate size measurements for mean particle diameters as small as 50 nm. To support the needs of the semiconductor industry, a 30 nm diameter SRM is being developed. Potential SRM candidates will be identified, and measurements of particle size and repeatability will be performed.

DELIVERABLES:

- Research sample availability and costs. 3Q 2008
- Perform particle size measurements and repeatability measurements for 30 nm SRM candidates. 4Q 2008

2. Equipment Characterization and Uncertainty Measurements – For particle sizes smaller than 50 nm, probability issues such as the slip correction and particle transfer function, have a greater affect on the uncertainty of the measurements. Further uncertainty computations will be needed to address these issues. Also for smaller particles, variances in equipment operation, such as instabilities in particle generation, become more important and can impact the repeatability of the size measurements. Improving the accuracy and reducing the uncertainty of the measurements will be addressed through better characterization of equipment.

DELIVERABLES:

- Evaluate and repair equipment for particle measurements and depositions. 3Q 2008
- Investigate and perform computations for issues that affect measurement uncertainty. 4Q 2008

Accomplishments

■ Completed and certified the measurements for new NIST Standard Reference Materials (SRM). Measured and certified SRM 1964, particles with a nominal diameter of 60 nm. Also measured and certified SRM 1963a, with a nominal diameter of 100 nm, to replace the previous 100 nm SRM 1963, which was corrupted due to agglomeration. SRM 1963a and SRM 1964 are currently available for purchase.

■ Completed the initial screening process and preliminary measurements for development of a 30 nm SRM. Identified primary and secondary candidate samples for the 30 nm SRM, based on diameter and distribution measurements. Researched measurement uncertainty for particles smaller than 50 nm and devised strategies for reducing the uncertainty.

■ Investigated the possibility of using silica as a material for SRM calibration particles. Verified the use of Differential Mobility Analysis for accurately sizing the silica particles. Completed preliminary diameter and distribution measurements of silica particle samples in a variety of sizes.

■ Developed and improved the NIST Calibration Facility, which uses Differential Mobility Analysis for sizing monodisperse spheres in the size range of 50 nm to 400 nm. Reduced the expanded uncertainty to 1.0 % of the particle size by correlating the slip correction to the measured particle size. Increased resolution and accuracy of measurements through improved equipment and intermediate measurements.

■ Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

■ Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

Collaborations

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

Donnelly, M. K., Yang, J. C., *"Screening Candidates for 30 nm Spheres,"* NISTIR 7345, August 2006.

G. W. Mulholland, M. K Donnelly, Hagwood, C., Kukuck, S. R., and Hackley, V. A., *"Measurement of 100 nm and 60 nm*

Particle Standards by Differential Mobility Analysis," J. Research NIST 111, 257–312, 2006.

T. A. Germer and G. W. Mulholland, *"Particle Size Metrology: Comparison Between Aerosol Electrical Mobility and Laser Surface Light Scattering Techniques,"* in Characterization and Metrology for ULSI Technology 2005, D.G. Seiler, A.C. Diebold, R. McDonald, C.R. Ayre, R.P. Khosla, S. Zollner, and E.M. Secula, eds., Proc. AIP 788, 579–583 (2005).

Front-End Materials Characterization

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in tow sub-sections, each focusing on a single aspect. These are:

- Front-End Materials and Emergining Advanced Materials Characterization
- Micro-and Nanoanalysis of Front End Materials

Front-End Materials and Emerging Advanced Materials Characterization

Technical Contacts:
Kin P. Chueng
Joseph J. Kopanski
Nhan Nguyen

Goals

To provide the IC industry with more useful and accurate measurements, models, data, and measurement transfer mechanisms for the incorporation of new materials into advanced CMOS to enable the continuation of scaling, as well as, beyond the limits of scaling. The major focus in the near term is on the search for new channel materials, new higher-κ dielectrics, metal gates and the integrated structure involving all three material types. Beyond 2011, high-mobility channel materials are expected to replace silicon in CMOS technology. New device structures such as multi-gate non-planner transistor are expected to replace the planar MOSFET. Devices based on semiconductor nanowires, carbon nanotubes, III-V quantum-well transistors, or another technology may even be used. The pace of new materials introduction is expected to increase. The introduction of new materials always presents substantial process integration challenges, as well as new reliability concerns. New metrology techniques must be developed to keep pace with all these changes. New measurement techniques are needed to address physical, chemical, optical and electrical properties of these new materials at the device level. Our current goals are:

(1) To improve the measurements of composition and thickness of thin films and interfaces for high-κ/compound metal gates on III-V compound semiconductors, silicon-on-insulator (confined silicon), and strained silicon-germanium.

(2) To improve measurement capabilities (on large custom made test structures) of interface energy barrier, work function, band offset, and interfacial defect structures of high-κ / metal electrode stacks on III-V systems.

(3) To develop high-resolution techniques (such as various kinds of scanning probe microscopy) to measure two-dimensional dopant profiles in advanced devices, strain profiles in the channel, work function and surface potential distribution, and dielectric constant.

(4) To correlate materials properties to the electrical performance of the transistor.

Customer Needs

The semiconductor industry has historically achieved exponential performance gains by aggressively scaling transistor dimensions. However, as devices approach sub-100 nm dimensions, scaling becomes more challenging and new materials are required to overcome the fundamental physical limits of the existing materials. The pace of new materials introduction is increasing as CMOS technology continues to advance. The introduction of new material into CMOS technology is always extremely challenging. For example, the introduction of high-κ/metal gate stack is so monumental that it was considered impractical for a very long time. Even as high-κ dielectrics and metal gates have begun early production in 2008, the materials and measurement needs for these processes will continue to evolve. The need for alternative channel materials is expected as early as 2011 to overcome the carrier-mobility limitations of silicon. Non-planar, multi-gate transistors are expected to be required as well. Even new device structures based on nanowires may be needed. In current mainstream CMOS technology, the use of strain in the channel region to enhance carrier mobility created fundamental materials questions such as determining the stress-strain relationship on the nanoscale. Such questions urgently need new measurement capability to address them. The answer has direct implication on technology decisions in the next generation and beyond.

Front end materials are in the critical path of technology decisions. A wrong decision may not only be expensive, but also disastrous. Facing the increasingly wider choices (or potential technology options), industry needs highly efficient, highly reliable, and highly accurate metrology tools to help them make the right choice.

The winter 2007 International Technology Roadmap for Semiconductors (ITRS) conference discussed these trends and the new measurement challenges for Front-End Process Metrology, High κ/ metal gate stacks, alternative channel materials, and emerging research materials and devices.

The current most important challenge in III-V nanoelectronics for logic is the compatibility of the III-V and the high-κ/ metal gate.

Technical Strategy

Understanding the physics of the high-κ/metal gate structure on III-Vs is critical to successfully selecting the right dielectric and metal to fabricate and implement the next complex emerging nanoelectronic devices. Within our resources, the approach is to find a way to produce a stable and reliable high-κ dielectric on a III-V substrate. Our focus areas include development of the III-V substrate surface treatment that allows a growth of electronically stable high-κ material and refined metrology methods to determine the interfacial physical, chemical, and electronic properties.

Energy Band Alignment of Metal Gate/ High-κ/III-V compound semiconductor

Intel and IBM have recently successfully implemented metal gate and high-κ dielectric in place of the traditional poly-silicon and thermal SiO2 into the 45nm manufacturing process. Intel cofounder Gordon Moore stated "The implementation of high-κ and metal materials marks the biggest change in transistor technology since the introduction of poly-silicon gate MOS transistors in the late 1960s." Such successes have opened up the possibility of extending silicon-based CMOS to employ metal gate and high-κ dielectric on high-mobility III-V compound semiconductors for high-speed and high-performance electronic device fabrications. However, the main difficulty that hinders the advancement of GaAs-based metal oxide semiconductor field-effect transistors is the lack of an appropriate oxide as a gate dielectric. There have been many efforts to search for electronically reliable and thermodynamically stable gate dielectrics that can be grown or deposited on GaAs. In addition, the stringent requirement that its fabrication method be compatible with Si-based device processing imposes a greater challenge. Several dielectrics have been investigated including Gd_2O_3, Al_2O_3, and HfO_2. One of the deciding factors for the selection of an appropriate dielectric is the band offsets at the dielectric interfaces with the III-V substrate and the metal gate, which must be large enough to minimize leakage currents.

DELIVERABLES:

- Measure band alignment of Al/Al2O3/GaAs 2Q 2008

Recently, in a collaboration with Intel, Purdue University and University of Texas at Dallas, we employed Internal Photoemission Spectroscopy (IPE), Vacuum Ultraviolet Spectroscopic Ellipsometry (VUV-SE), and electrical capacitance-voltage (C-V) measurements to establish the energy band offsets at the interfaces of Al_2O_3 as the high-κ dielectric on GaAs with Al and TaN metal gates. We have shown that barrier height offsets are affected by the chemical conditions of the starting GaAs substrate. The energy barrier height (Φ_0) at the Al_2O_3 and sulfur-passivated GaAs interface is found to be 3.0 eV, which is different from those obtained on unpassivated or NH_4OH-treated GaAs. On the top Al/Al_2O_3 interface, Φ_0 is equal to 2.9 eV. Hole photoemissions from the Al to Al_2O_3 valence band is also observed. With an optical band gap of 6.4 eV for thin Al_2O_3 determined from ellipsometry measurement, the band alignments at both Al_2O_3 interfaces can be configured as shown in Figure 1. This effort is continuing using different high-κ dielectrics and metal gates and involving additional chemical and physical characterization techniques.

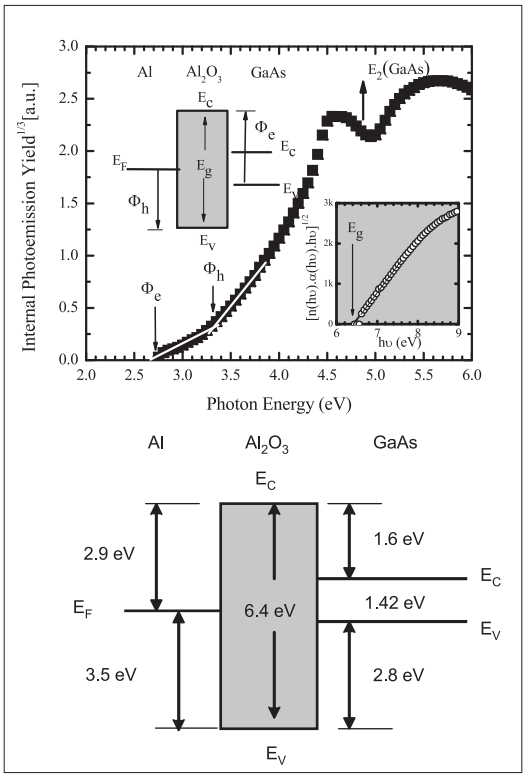

Figure. 1. The top graph is the band offsets at an Al/Al_2O_3 interface determined by Internal Photoemission (IPE) and Vacuum Ultraviolet Spectroscopic ellipsometry (VUV-SE) for an Al/Al_2O_3/GaAs structure (top graph). The bottom diagram is the complete band alignment of Al/ Al_2O_3/GaAs at flat band condition as measured by IPE and VUV-SE.

DELIVERABLES:

- Measure band alignment of TaN/Al_2O_3/GaAs 2Q 2008
- Surface treatment and characterization, and band offset of Al/HfO_2/GaAs and Au/HfO_2/GaAs 4Q 2008

Two Dimensional Dopant profiles, Metal work function, and Strain by Scanning Probe Microscopy

The emerging need for alternative channel materials for ultimate CMOS opens up a plethora of materials characterization issues. Strained Si-Ge has already been implemented in current technology-node CMOS, while alternative channel materials such as Ge-on-insulator for PMOS and III-V for NMOS technology have been proposed for ultimate CMOS. Characterization of the complete MOS stack from the work function of the metal gate, the band offsets, and the interfacial defect structures of high-κ combinatorial metal electrode stacks systems becomes necessary. Integration of these new materials into existing process lines and their effect on device performance and reliability are key concerns.

We are developing and employing several varieties of scanning probe microscopy (SPM) for characterization of several critical front end material parameters. SPMs offer the promise of extremely high spatial resolution measurement of local electrical properties. Scanning capacitance microscopy (SCM) remains of interest for measurement of both the ultra-shallow junction dopant profiles in silicon as well as in strained Si-Ge and III-Vs. Improvements in this technique are needed to achieve the spatial resolution requested in the ITRS. These needs include improved sample preparation techniques to reduce surface-oxide roughness noise (fixed pattern noise) and surface-damage effects on the SCM images; sharper and more durable SCM tips; implementation of the SCM in an inert atmosphere or ultra-high vacuum; and improvements in sensitivity and noise floor of the SCM capacitance sensor. Current work in the Semiconductor Electronics Division has a goal of developing improved capacitance sensors with sensitivity to the atto-Farad level. Test structures that are directly accessible by the SCM tip are under development as a means to more accurately calibrate the current and future generation SCM sensors.

Another technique of great interest is the scanning Kelvin force microscope (SKFM) for the local measurement of contact-potential difference. If the tip work function is known, the work function of the sample under test can be deduced. We have recently demonstrated test structures with multiple different metals, for example, aluminum (φ_{Al} = 4.28 eV), chromium (φ_{Cr} = 4.5 eV), and gold (φ_{Au} = 5.1 eV). Since the effective work functions of these three metals can be measured with tips of known work function, see Figure 2, they can then be employed as a vehicle to determine the work functions of tips that are not known, for example, carbon nanotube tips. Recent work has demonstrated the spatial resolution limits of the SKFM microscope and has suggested a method to improve the spatial resolution. SKFM depends on the capacitance between the tip and the sample, which varies as the inverse square of the separation of the various parts of the tip with the sample. As this is a relatively large-range force, the tip, tip sidewall, and cantilever all contribute significantly to the measured CPD, effectively making measurements that are simultaneously accurate and having high spatial resolution impossible. Several methods for improving the spatial resolution of the SKFM by using the derivative of the force between the tip and sample as the feedback signal are under development. We have also recently begun a collaboration to characterize high-aspect ratio carbon nanotube terminated tips for use with the SKFM. These tips should greatly reduce cantilever effects on SKFM.

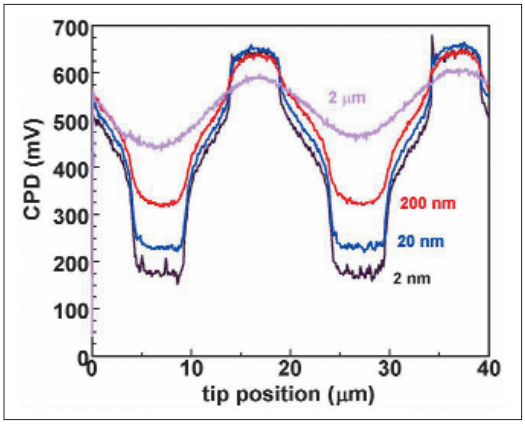

Figure 2. Contact potential difference (CPD) of Au and Al lines, separated by oxide, measured with scanning Kelvin force microscopy. CPD is related to work function via: $CPD = \varphi_{tip} - \varphi_{sample}$

DELIVERABLES:

- Implement a differential force mode SKFM in atmosphere using Q-control and custom feedback electronics. Demonstrate improved spatial resolution over the traditional SKFM mode. 4Q 2008

If a high spatial resolution mode of the SKFM can be developed, multiple characterization problems can be addressed. These include measurement of the work function profile across physically beveled gate-stack structures, measurement of surface state density at pn-junctions and Schottky contacts, detection of single dopants (or clusters) and single defects in bulk semiconductors and nanowire structures, and measurement of the local strain in semiconductors or metal films from the shift in the measured workfunction. A recent collaboration with the University of Albany seeks to characterize the use of SKFM for strain measurements.

DELIVERABLES:

- Characterize the level of strain in Si-Ge films on insulator and metal in films on cantilevers using the SKFM. Determine if quantitative strain measurements are possible with this technique and correlate with nano-Raman. 1Q 2009

Collaborations

Intel – Electrical and optical characterization of metal gate/ high-κ dielectric / III-V high mobility semiconductors.

International SEMATECH – Optical electrical characterization and energy band alignment of ternary metal gate/high-κ / Silicon.

International SEMATECH, ATDF – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers.

International SEMATECH – Improvement of the SCM and SKFM techniques for two-dimensional dopant profiling and surface work function measurements.

IBM – Physical and optical characterization of high- κ on Silicon.

MSEL, NIST – Characterization of metal gate/high-κ systems.

Purdue University – Surface characterization and electrical and optical band offset characterization of metal gate/ high-κ dielectric / III-V high mobility semiconductors.

Rutger University – Defect and structural characterization of high-κ on silicon.

University of Albany – Characterization of strain in Si-Ge on insulator.

University of Texas-Dallas – Surface characterization and electrical and optical band offset characterization of metal gate/ high-κ dielectric / III-V high mobility semiconductors.

University of Maryland, College Park – Ultra-thin gate oxide reliability.

Xidex Corp. – Evaluation of carbon nanotube tip for use in SCM and SKFM.

Yale University – Electrical characterization of high-κ systems.

Recent Publications

N. V. Nguyen, H. D. Xiong, J. S. Suehle, O. A. Kirillov, E. M. Vogel, P. Majhi, and H.-C. Wen, *"Internal Photoemission Spectroscopy of [TaN/TaSiN] and [TaN/TaCN] Metal Stacks,"* Applied Physics Letter **92**, 092907 (2008).

N. V. Nguyen, O. A. Kirillov, W. Jian, J. E. Maslar, W. A. Kimes, and J. S. Suehle, *"Interface Barrier Determination by Internal Photoemission: Applications to Metal/Oxide/Semiconductor Structure,"* Electrochemical Society Transaction, May (2008).

N. V. Nguyen, W. Jiang, Oleg A. Kirillov, Wenyong Wang, John S. Suehle, P. D. Ye, Y. Xuan, N. Goel, K.-W. Choi, S. Safak, and Wiman Tsai, *"Band offsets of atomic-layer-deposited Al2O3 on GaAs and surface treatment affects,"* To be submitted to Applied Physics Letters (2008).

J. E. Maslar, W.S. Hurst, D.R. Burgess, W.A. Kimes, N.V. Nguyen, E.F. Moore, J.T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* Electrochemical Society Transaction in May 2008.

D.H. Hill and R.A. Bartynski, N.V. Nguyen, Albert C. Davydov, and Deane Chandler-Horowitz, and Martin M. Frank, *"The relationship between local order, long range order, and sub-bandgap defects in hafnium oxide and hafnium silicate films ,"* submitted to Applied Physics Letters, Feb 2008.

N. V. Nguyen, O. Kirillov, H. D. Xiong, and J. S. Suehle, *"Internal Photoemission Spectroscopy of Metal Gate / High-k / Semiconductor Interfaces,"* Frontiers of Characterization and Metrology for Nanoelectronics: 2007, AIP Conference Proceedings 931, page 308 (2007).

H.D. Xiong, N.V. Nguyen, J.S. Suehle, E.M. Vogel, *"Work function characterization of TaSiN and TaCN electrodes using CV, IV, IPE and SKPM,"* Electrochemical Society Transaction (2007).

E. Maslar, W.S. Hurst, D.R. Burgess, Jr., W.A. Kimes, N.V. Nguyen, and E.F. Moore, *"In Situ Characterization of Gas-Phase Processes During Hafnium Oxide Atomic Layer Deposition,"* ECS Transactions 2, 133-143 (2007).

J. J. Kopanski, M. Y. Afridi, S. Jeliazkov, W. Jiang, T. Walker, *"Scanning Kelvin Force Microscopy For Characterizing Nanostructures in Atmosphere,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 530-534, Gaithersburg, MD, March 27-29, 2007. (Sept. 2007).

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J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, C. Young, S. Shah, D. Maher, B. Foran, P. Y. Hung, and A. Diebold, *"A Comparison of Thickness Values for Very Thin SiO2 Films by Using Ellipsometric, Capacitance-Voltage, and HRTEM Measurements,"* Journal of the Electrochemical Soc., vol. 153, p. F12, 2006.

N. V. Nguyen, S. Sayan, I. Levin, J. R. Ehrstein, I. J. R. Baumvol, C. Diremeier, C. Krug, L. Wielunski, P. Y. Hung, and Alain Diebold, *"Optical band gaps and composition dependence of hafnium-aluminate thin films grown by atomic layer chemical vapor deposition,"* J. Vac. Sci. Technol. A 23 (2005).

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N. V. Nguyen, D. Chandler-Horowitz, A. Davydov, C. Hacker, S. Park, H. Xiong, J. Ehrstein, J. Kopanski, J. Suehle, E. Vogel and M. Frank, *"Crystallinity and Defects in Hafnium Oxide and Hafnium Silicate Films,"* High Dielectric Constant Gate Stacks III of the 208th Meeting of The Electrochemical Society in October 16-21, 2005.

N. V. Nguyen, Albert V. Davydov, Deane Chandler-Horowitz, Martin M. Frank, *"Sub-bandgap defect states in polycrystalline hafnium oxide and their suppression by admixture of silicon,"* App. Phys. Lett. 87 (2005).

N. V. Nguyen, S. Sayan, I. Levin, J. R. Ehrstein, I. J. R. Baumvol, C. Diremeier, C. Krug, L. Wielunski, P. Y. Hung, and Alain Diebold *"Optical band gaps and composition dependence of hafnium-aluminate thin films grown by atomic layer chemical vapor deposition,"* J. Vac. Sci. Technol. A 23 (2005).

S. Sayan, N. V. Nguyen, and J. Ehrstein, T. Emge and E. Garfunkel, I. Levin, E. P. Gusev, Hyoungsub Kim and P. J. McIntyre, *"Structural, Electronic, and dielectric properties of ultrathin zirconia films on silicon,"* Applied Physics Letter 86, 152902 (2005).

Micro- and Nanoanalysis of Front End Materials

Technical Contacts:
G. Gillen: SIMS
D. Simons: SIMS
J. Small: TEM, X-ray detectors

Goals

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. The major focus is placed on metrology requirements from the 2007 International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) structural and elemental analysis at the device level, including SIMS and HRTEM, and (2) metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project develops new methods for depth-profiling polymeric materials by Secondary Ion Mass Spectrometry (SIMS), defines optimum procedures for ultra-high depth resolution, develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as, characterizes the accuracy and reliability of existing methods. Materials of interest include high-κ and low-κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. High Resolution Transmission Electron Microscopy (HRTEM) is being developed as a chemical tomography tool for determining 3-D elemental distributions in advanced materials.

Customer Needs

This project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack processes and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2007 International Technology Roadmap for Semiconductors (ITRS) near-term difficult challenges for front-end processes include: *metrology issues associated with gate dielectrics film thickness and gate stack electrical and materials characterization and metrology issues associated with 2-D dopant profiling. Metrology needs for thermal/thin films, doping technology, SOI, and strained-silicon are discussed in the Metrology section of the 2007 ITRS.*

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements.

The 2007 ITRS Metrology section identifies structural and elemental analysis at devices dimensions (for example 3-D dopant profiling) as one of the difficult near-term challenges (Table MET1). Off-line secondary ion mass spectroscopy has been shown to provide the needed precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. The ITRS requirements are for at-line dopant profile concentration measurements with precision of 4 % in 2007, decreasing to 2 % precision for the 2010

through 2018 timeframe. The lateral/depth resolutions for 2-D/3-D dopant profiling decrease from 2.5 nm in 2007 to 1.4 nm in 2012. Complete specifications are given for the short term in Table MET5a and for the long term in Table MET5b of the 2007 Metrology section. The need for advances in image and spectral modeling for TEM and STEM applied to 3-D atomic imaging and spectroscopy is discussed under Emerging Research Materials and Devices in the Metrology section of the 2007 ITRS. The desirability of nondestructive direct measurement of stress in nanosized areas of strained silicon is described in the Front End Processes area of the Metrology section, and specific requirements are given for the first time in Tables MET5a and MET5b.

Technical Strategy

The 2007 ITRS expressed as difficult challenges: "starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams," and "measurement of complex material stacks and interfacial properties including physical and electrical properties" (Table MET1, Metrology Section). Our focus areas include development of refined metrology methods and standards for SIMS and TEM and developing improved X-ray detection capabilities for SEMs and electron microprobes.

STRUCTURAL AND ELEMENTAL ANALYSIS AT THE DEVICE LEVEL, INCLUDING SIMS AND HRTEM

The revolutionary changes in device technology needed to sustain long-term improvements in the performance of nanoelectronics demand the development of new more sophisticated nanometer- and sub-nanometer-scale metrology solutions. New device technologies comprise new materials and novel three-dimensional (3D) geometries in the medium term, and a full-scale break from the CMOS paradigm in the long term. We are developing new techniques for 3D characterization using existing 2D projection-based nanometer-scale metrology tools such as conventional or scanning transmission electron microscopy. Specifically, we are using a state-of-the-art high resolution TEM to develop a method for creating 3D chemical tomography with nanometer spatial resolution.

DELIVERABLES:

- Generate 3D chemical tomogram of FinFET device structure with HRTEM. 3Q 2008

2. Strained Si processes have become an accepted means for enhancing carrier mobility and thereby improving transistor performance. The ITRS calls for a nondestructive method for measuring stress in nano-sized areas of Si to accelerate process development. Confocal Raman microscopy is a potential in-line method to achieve this goal with the required sensitivity and spatial resolution. We are conducting a systematic investigation to determine the feasibility of this methodology for achieving the metrology goals for stress and strain that are called out for the first time in the 2007 ITRS.

DELIVERABLES:

- Apply confocal and super-resolving Raman microscopy to the characterization of strain in nanostructured Si. 3Q 2008

As integrated circuit dimensions shrink to the sub-micrometer regime, there is continued need for accurate and quantitative dopant depth profiling with ultra-high-depth resolution. To probe shallow dopant profiles in Si and other materials, SIMS instruments typically utilize very low energy primary ion beams to bombard the sample surface. In this case, it is difficult to obtain a well-focused and high current density beam, especially in a magnetic-sector SIMS instrument. Recently, there has been growing interest in using molecular ion beams for depth profiling. When a molecular primary ion beam impacts the surface, it dissociates into its constituent atoms with each atom retaining a fraction of the initial energy of the cluster. This process can lead to impact energies on the order of a few 10's of electron volts and a corresponding reduction in the depth of penetration of the primary ion. This process may potentially allow for ultra high resolution depth profiling. In this project, we will utilize C_{60}^{+} and Bi_3^{+} cluster primary ion beam sources at NIST to sputter depth profile Si, GaAs, SiC, and multiple delta-layer test materials.

Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. In these cases, the achievable depth resolution is limited not by the penetration depth

of the primary ion but by the topography induced by the sputtering process itself. We will also explore the use of cluster bombardment SIMS for reduction of sputter induced topography in metal films. This approach will be applied to study depth profiling analysis of gold diffusion in copper and the depth distribution of blanket metals films (copper metallization on silicon).

DELIVERABLES:

- Use TEM and and nanoindentation to investigate anomalously thick carbon-rich layers on Si produced by C_{60}^+ bombardment. 1Q 2008

Accomplishments

Implementation of C60+ Cluster Ion SIMS Capability for SIMS Analysis of Silicon Wafers

Previous efforts using SF_5^+ cluster primary ion sources used for SIMS analysis of both organic and inorganic materials on silicon have been very successful. Minimization of beam-induced damage in organic materials has allowed molecular depth profiling of polymers such as photoresists on silicon and enhanced ion yields for high-molecular weight fragments. Inorganic material analysis has benefitted in the area of ultra-shallow depth-profiling as well as for analysis of some particularly difficult systems such as metal multi-layers stacks. Continued development of SIMS for higher depth resolution dopant profiling has led to the implementation of a C_{60}^+ primary ion source on the NIST magnetic sector SIMS instrument. This ion source produces stable ion beams of C_{60}^+ and C_{60}^{2+} at beam energies of 10 keV with typical currents approaching 20 nA under conditions that allow several hundred hours of operation. The beam can be focused into a spot size of ≈1 μm allowing micrometer spatial scale mapping of patterned silicon wafers. Due to the breakup of the C_{60}^+ projectile during impact with the silicon surface, the energy of an individual carbon atom in the cluster is reduced to a few hundred electron volts. This low energy should theoretically provide SIMS depth resolution better than 1 nm. Reduction of the C_{60}^+ impact energy to values less than 10 keV to attempt further improvement in depth resolution is foiled by carbon deposition that precludes the acquisition of depth profiles from the wafer sample. However, the deposition effect may be useful for lithographic applications as it allows direct ion beam writing of a conductive carbon layer on silicon. By using C_{60}^+ impact energies greater than 10 keV, C_{60}^+ SIMS depth profiles have been obtained from a number of semiconductor-related materials including As and B delta-doped structures as well as ion implants of various dopant species. The depth resolution of SIMS depth profiles obtained from these samples has not been has high as expected. To understand the process in more detail, transmission electron microscopy (TEM) studies of C_{60}^+-bombarded silicon have been carried out using focused ion beam (FIB)-prepared cross sections of the sample surface. Figure 1 shows a cross sectional TEM image of a silicon wafer bombarded with C_{60}^+ at an impact energy of 14.5 keV. The figure indicates that C_{60}^+ bombardment of silicon results in the formation of a carbon-rich altered layer that is about 25 nm thick, much greater than the 2 nm range predicted from conventional ion implantation models. Working with Micron Technology and International SEMATECH, we are currently studying the effect of this extended transport of carbon into silicon both from the standpoint of improving the applicability of larger carbon cluster ion beams for SIMS analysis and also as a potential method for direct-write fabrication of SiC films and devices on silicon.

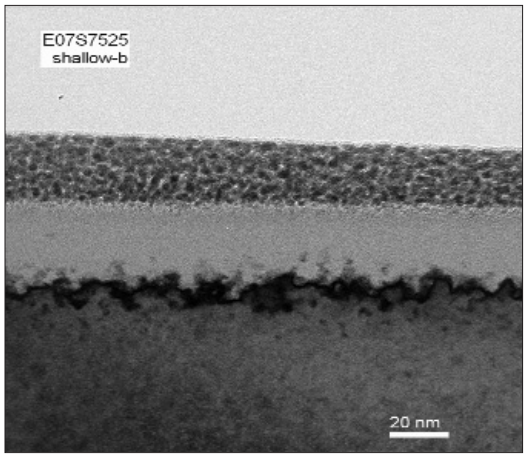

Figure 1. Cross sectional TEM image of C_{60}-bombarded silicon wafer. Top layer is a Pt metal overcoat. Middle layer is C_{60} altered layer. Bottom layer is the silicon substrate.

Depth Profiling of Organic Overlayers Using SIMS

Organic photoresists and low-κ dielectric materials are key components for front end semiconductor processing. There is also a growing interest in the use of organic semiconductor materials for organic

light emitting diodes and organic thin film transistors. In anticipation of a growing need for metrology tools to characterize these types of materials, we are developing new approaches to characterize the chemical composition and in-depth distribution of organic thin films on silicon. Typically, the use of ion beam sputtering techniques, such as secondary ion mass spectrometry (SIMS), results in extensive chemical degradation of organic thin films such as photoresists or organic light emitting diodes. However, we have found that cluster primary ion bombardment SIMS can minimize this degradation allowing for intact characteristic ions to be obtained throughout the depth of the film. Furthermore, it appears that analyzing these organic materials at cryogenic temperatures provides further reduction in beam-induced damage. In this project, an SF_5^+ polyatomic primary ion source was used to depth-profile poly(methyl methacrylate) (PMMA) photoresist by SIMS at a series of temperatures from -75 °C to 150 °C. The depth profile characteristics (*e.g.,* interface widths, sputter rates, damage cross sections, and overall secondary ion stability) were monitored as a function of temperature for atactic, syndiotactic and isotactic PMMA. At low temperatures it was found that the secondary ion stability increased considerably. In addition, the interfacial widths were significantly smaller. Examples of this increased stability at low temperatures for syndiotactic and isotactic PMMA are illustrated in Fig. 2 for the PMMA fragment at m/z = 69. Corresponding AFM images indicated that there was also decreased sputter-induced topography formation at these lower temperatures as illustrated in Fig. 3. Higher temperatures were typically correlated with increased sputter rates. However the improvements in interfacial widths and overall secondary ion stability were not as prevalent as was observed at low temperatures. The importance of the glass transition temperature (T_g) on the depth profile characteristics was also apparent. The sputter properties of isotactic and syndiotactic PMMA differed greatly. Isotactic PMMA showed sharper interface widths and better depth profile characteristics from 0 °C to 65 °C over those observed for syndiotactic or atactic PMMA. The results of this study demonstrate that it is possible to monitor the chemical composition of photoresist thin layers on silicon by analyzing the samples at cryogenic temperatures. This work has resulted in collaborations with SEMATECH to prepare thin films of a PMMA photoresist on silicon that will be used as standards for compositional depth profiling.

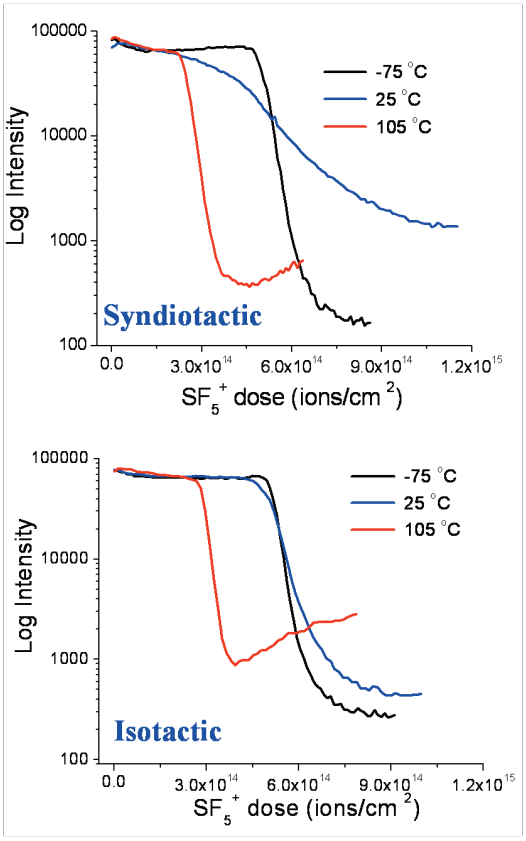

Figure 2. Intensity of m/z = 69 (fragment characteristic of PMMA) as a function of increasing SF_5^+ dose for syndiotactic and isotactic PMMA at three different temperatures.

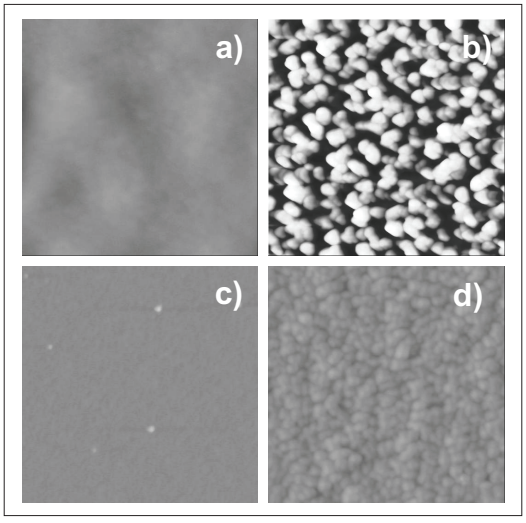

Figure 3. Atomic Force Microscopy (AFM) topography images (1 μm x 1 μm area) of SF_5+ sputtered crater bottoms at different temperatures: (a) PMMA surface, R_{rms} = ~0.85 nm, (b) 25 °C, R_{rms} = ~11.37 nm, (c) -75 °C, R_{rms} = ~0.274 nm, and (d) 125 °C, R_{rms} = ~1.00 nm.

Nanoscale Stress Measurements using Confocal Raman Microscopy

To optimize yield and reliability in microelectronic, photonic, and microelectromechanical devices, measurement tools and metrology must be developed that can accurately detail the stress state of a material on the nanoscale. To address this need, work has been focused on the application and advancement of confocal Raman microscopy and the protocols that enable the characterization of stress in semiconductor structures. The results of high-resolution, high-density stress mapping of nanoindentations in silicon have been used to begin the validation and calibration of the measured stress. In these studies, high-resolution scans detail the stress distribution around the deformed area of the indentation as well as the stress fields that result from accommodation of higher loads, e.g. fracture. Hyperspectral peak-fitting algorithms and super-resolution techniques have been developed that provide stress resolution of approximately 10 MPa, lateral spatial resolution approaching 100 nm, and depth resolution approaching 300 nm. Indentation and crack field stress distributions have been measured and the results agree well with analytical models. The effects of indentation load for both spherical and pyramidal indentation and crystal orientation have been demonstrated on Si(100) and Si(111) surfaces. Figure 4 shows the results of a hyperspectral Raman microscopy stress measurement on Si(100) over a 10 μm x 10 μm area. The color image (bottom) is of a region of a nanoindentation that includes a crack tip. The stress map of this feature and more importantly the functional form of the stress field falloff (shown at the top) provides information (stress-intensity factor and thus toughness) critical for determining the suitability of a material for a given application. Current efforts are focused on the development of models and the benchmarking of experimental protocols for the complete characterization (tensor field vs. scalar map) of intrinsic and engineered stress states in semiconductors.

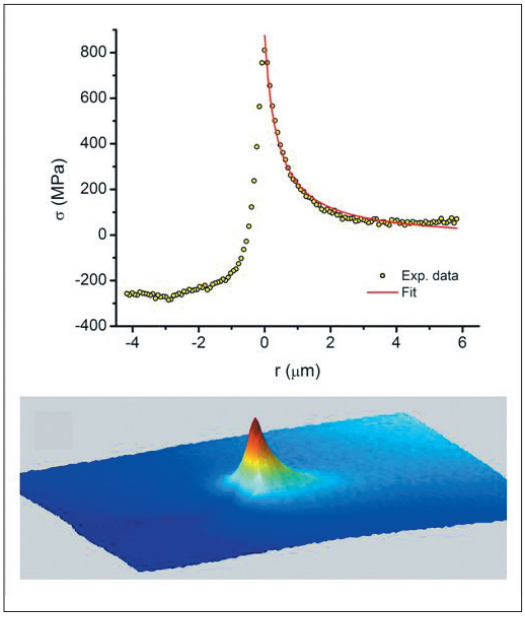

Figure 4. Hyperspectral Raman microscopy stress measurement on Si(100). Bottom: 3D stress map with 128 x 128 spectra over a 10 μm x 10 μm area of a nanoindentation. Top: Line scan of stress and model fit.

Enhanced Performance of Microcalorimeter X-Ray Detector

The NIST transition-edge sensor (TES) microcalorimeter X-ray detector is a versatile instrument that combines the high resolution of wavelength-dispersive detectors with the extended range of energy-dispersive detectors. The detector is a small calorimeter operated at a low temperature (70 mK). The temperature change caused by the absorption of single X-ray photons is registered by a current through the transition edge sensor — a thin metal film that undergoes a superconducting-normal transition at the operating point. Our present detector has demonstrated a FWHM resolution of 4.4 eV at 5.9 keV. The technology of microcalorimeters is more complicated than most X-ray detectors, so that a new set of operating considerations has emerged in the process of developing it as an analytical instrument.

We report here the first operation of the NIST TES microcalorimeter X-ray detector to perform quantitative analysis of a sample with an electron probe. The detector element is mounted at the end of a probe projecting from the dewar into the electron microscope. The probe extends horizontally, which requires a sample mounting angle of 45° to optimize the yield with a vertical electron beam. The sample was analyzed using a microbeam probe with a beam current of 7 nA at an energy of 12 keV.

The detector is a microcalorimeter element 400 μm square, located approximately 30 mm from the source of the radiation. Its energy range is 400 eV to 7 keV. Count rates of 50/s to 170/s were registered while taking spectra of the sample and related

standards. Spectra were processed using conventional analog pulse amplifiers and pulse-pileup circuitry modified for the relatively long period of the microcalorimeter pulses. The pulses were recorded with a 16 K channel multi-channel analyzer board with an approximate resolution of 0.5 eV/channel. All spectra were obtained in 1000s live time.

The sample was the K-411 glass which is part of the NIST Standard Reference Material 470, Mineral Glasses for Microanalysis, a standard intended for use with electron probe microanalysis and SIMS. It contains previously analyzed quantities of SiO_2, MgO, FeO, and CaO. Spectra were also taken of reference standards consisting of Fe, SiO_2, MgO, and chloroapatite [$Ca_5(PO_4)_3Cl$]. A spectrum of K-411 glass used in the quantitative analysis is shown in Fig. 5.

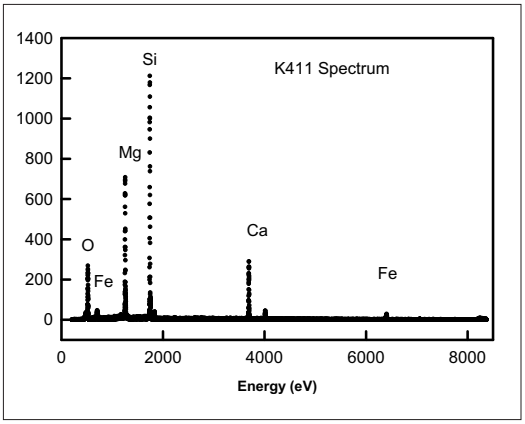

Figure 5. Spectrum of the K-411 Standard Reference Material glass taken with the NIST TES microcalorimeter X-ray detector excited by an electron beam.

Calculations were carried out using a Monte Carlo procedure which varied the composition of the respective elements. The maximum deviation from the concentrations certified in the NIST SRM in the first round of analysis is 2 %. The work demonstrates that the NIST TES microcalorimeter detector has considerable potential for the analysis of X-ray fluorescence lines which would overlap in current energy-dispersive detectors or would be too low in energy for most wavelength-dispersive detectors.

Inkjet Printing for Trace Metal Contamination Standards

Prototype reference materials for trace element contamination on silicon surfaces have been prepared using piezoelectric drop-on-demand inkjet printing technology. Reference materials were prepared for 6 different elements (K, Cl, Ni, Cu, Fe, and Au) at surface area concentrations ranging from 10^7 atoms/cm^2 to 10^{15} atoms/cm^2. Each element was prepared on a separate 2.5 cm diameter silicon wafer. The microdroplets were dispensed onto specific grid squares that had been previously scribed onto the silicon surface in a finder grid pattern with a laser. Different concentrations of the elements were achieved by printing different numbers of microdroplets in the same location. Dispensing droplets onto specific locations on a finder grid allowed different contaminant concentrations to be located easily and analyzed rapidly by SIMS analysis.

Characterization of these reference materials is in progress. SIMS depth profiles from grid squares containing different numbers of printed droplets show an exponential decay, the amplitude of which scales with the number of droplets applied. Integration of the number of ion counts beneath these profile curves is shown in Figure 6 plotted against the number of droplets printed for concentrations of gold ranging from approximately 1 x 10^{12} atoms/cm^2 to 1 x 10^{14} atoms/cm^2. This plot shows the linear relationship between the measured number of gold ions detected and the number of droplets dispensed.

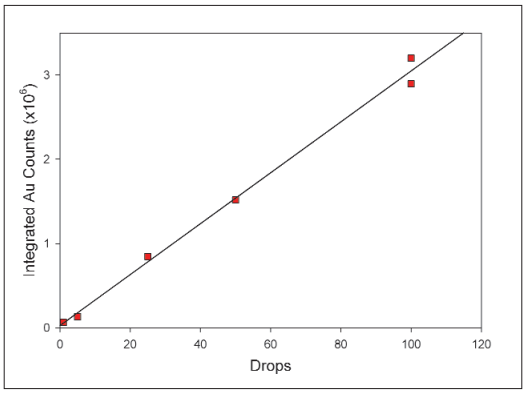

Figure 6. Integrated gold secondary ion counts from depth profiles plotted against the number of droplets dispensed by the inkjet printer. One drop = 1.3 x 1012 atoms/cm^2.

LACSBI: A Technique for Removing Unwanted Diffraction Effects from TEM-Based Chemical Images

As front end devices move from the familiar structures of conventional CMOS toward new materials and complex 3-D geometries, there

will be an increasing need for flexible metrology solutions at the nanometer length scale. Energy-filtered transmission electron microscopy (EFTEM) provides a method for rapid spectroscopic characterization with nanometer resolution, suitable for both conventional 2-D and tomographic (3-D) chemical imaging. However, the extraction of quantitative chemical images with EFTEM is limited by the susceptibility of all convention transmission electron microscopy (CTEM) to diffraction effects in crystalline specimens: coherent scattering contrast that complicates the interpretation of the [incoherent] chemical contrast.

This effect is illustrated in Fig. 7 with an EFTEM spectral image reconstruction of a FinFET device structure. Here, the distinct colors correspond to amorphous silicon oxide (red), silicon nitride (green) and hafnium oxide (blue) phases, as well as the single-crystal silicon fin (cyan). Only the silicon phase will exhibit diffraction effects. At conventional fixed beam imaging conditions (a), the variation in intensity in the fin from its base (bright) to its tip (dark) is actually the superposition of a <011> diffraction pattern on the chemical image. This superposition causes the measured silicon concentration to appear high in the bright regions and low in the dark regions, relative to that measured in the amorphous phases. A comparable image with the microscope operated in large angular convergence scanned beam illumination (LACSBI) mode (b), filters out this diffraction contrast. Since all other phases are amorphous, for which no diffraction effects are expected, this application provides a "null" experiment for identification of potential artifacts with LACSBI. No visible loss in spatial resolution is evident in the comparison of Fig. 7 (a) and (b), and a line trace from the LACSBI image (c) shows a spatial resolution of ≈2 nm and normalized phase fractions that sum to 99.4 % ± 1.1 % along the line trace.

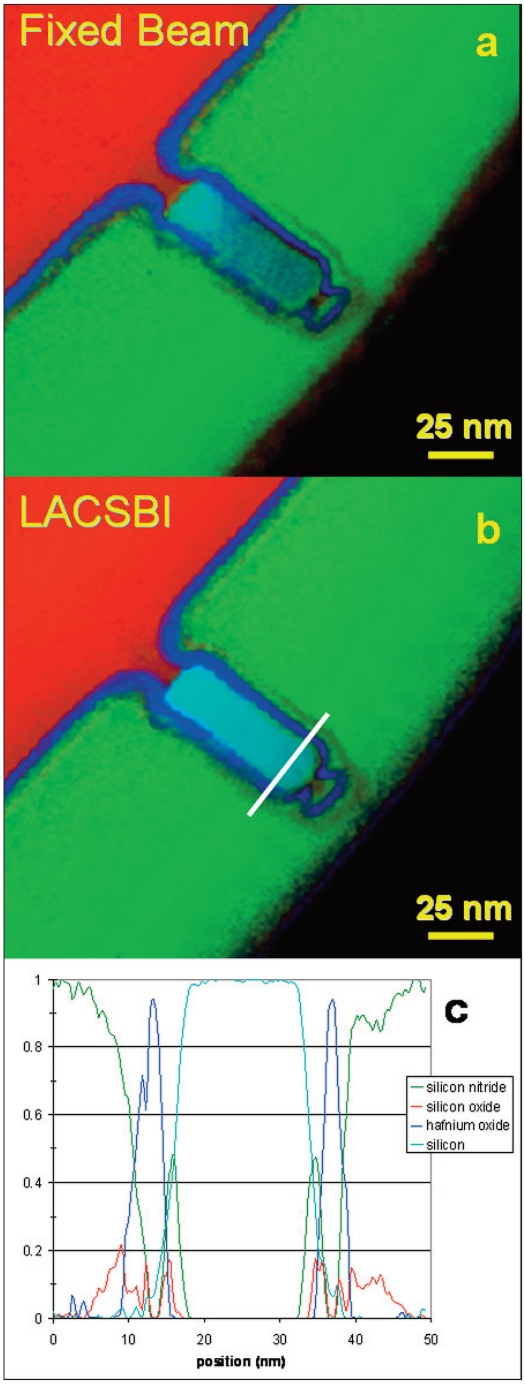

Figure 7. LACSBI with EFTEM imaging of a FinFET. See text for details..

LACSBI mitigates diffraction contrast by averaging the data acquisition over many incident beam orientations, thus providing a largely incoherent image, as required for quantitative analysis. As important as this signal incoherence is for quantitative 2-D imaging and compositional profiles, it is essential for tomographic reconstruction of 3-D chemical images, since the incoherent signal obeys the "projection" requirement for all existing 3-D reconstruction methods from tilt series of images. Thus LACSBI provides a breakthrough in nm-scale metrology for the complex 3-D architectures that are expected for nonconventional CMOS and post-CMOS devices.

This study is a collaboration with Brendan Foran of Aerospace Corp.

Collaborations

Aerospace Corporation – TEM-based chemical imaging.

International SEMATECH, ATDF – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers.

Ionoptika – Development of a C_{60}^{+} primary ion source for advanced semiconductor technology.

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces.

Micron Semiconductor – trace organic detection.

Publications

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Advanced Gate Stacks Materials

Technical Contacts:
M. L. Green

Goals

The goals of this project are to develop novel combinatorially-compatible measurement methods and metrologies that enable the microelectronics industry to select new materials more rapidly and intelligently through use of comprehensive and consistent data sets.

Customer Needs

At present, further scaling (dimensional shrinkage of integrated circuit device elements according to Moore's Law) of Si microelectronics is materials limited. For example, higher mobility substrates (e.g., Ge, GaAs, and strained Si) are needed as replacements for Si, and the traditional gate stack layers (gate dielectric and polycrystalline Si gate electrode) must be replaced with a high-k gate dielectric and a metal gate electrode. The Si microelectronics industry, and the consumer electronics and information revolution that it fuels, is, at $750 billion, one of the largest sectors of the US (and global) economy. The development of materials with superior properties that enable device scaling and enhanced device performance are key to continued innovation in Si microelectronics.

Currently, there are no rapid measurement techniques to determine the physical and electrical properties of novel metal-oxide-semiconductor (MOS) materials; the availability of such methods would enable rapid selection and optimization of these materials and their commercialization in devices.

Key customers include Sematech and major U.S. semiconductor manufacturers such as Intel, Micron, and Qualcomm. We are very active in promoting the use of combinatorial methodologies with these customers.

Technical Strategy

The CMOSFET device (complementary-metal-oxide-silicon-field-effect-transistor, the workhorse of advanced chips such as Pentium microprocessors), is extremely complex, and the identification of replacement materials with superior properties is difficult due to the large number of candidate materials for either gate stack or high mobility applications. Introduction of new materials is complicated by rigid requirements that they not only possess the requisite physical and electrical properties, but also be manufacturable, thermally stable during processing, and compatible with neighboring materials. There are no rapid measurement techniques to determine the physical and electrical properties of novel CMOS materials. The availability of such methods would enable the rapid selection and commercialization of such materials. It is imperative to be able to make hundreds or thousands of measurements in parallel, since there are at least that many combinations of novel gate metal electrode/gate dielectric/substrate materials that must be assessed. Further, for some measurements, such as gate metal electrode work function, the most appropriate measurement technique is not apparent. The traditional gate stack layers (SiO_2 gate dielectric and polycrystalline Si gate electrode) in current Si microelectronic devices must be replaced with a high dielectric constant (high-*k*) gate dielectric and a metal gate electrode. We will develop combinatorial methodologies to: (1) fabricate compositionally-graded thin film libraries of novel gate metal electrode-high-gate dielectric-substrate combinations ("gate stack" structures) ; and (2) measure the key electronic properties (e.g., work function) and thermal stability of such libraries. In addition, a nanocalorimetry method will be developed to measure thermal stability. Comprehensive data sets of electronic properties as a function of composition will be generated for materials systems identified as high priority by the microelectronics industry.

DELIVERABLES:

- Improve calibration procedures for the combinatorial thin film synthesis tool Q1 2008
- Generate comprehensive data sets for materials systems identified as high priority by the microelectronics industry, including design of combinatorial libraries (e.g., work functions in Ta1-xCxNy/HfO2/Si) Q2 2008
- Develop combinatorial measurement methodologies: optimize automated electronic measurement tools to determine work functions in advanced gate stack systems Q3 2008
- Compare combinatorially derived work functions with measurements on selected discrete samples, for benchmarking Q4 2008

Accomplishments

Combinatorial approach to the advanced gate stack

We commissioned a state-of-the-art combinatorial tool capable of producing thin film libraries by reactive sputtering or pulsed laser deposition (PLD). Both chambers are equipped with multiple targets, allowing for the deposition of ternary films of metals and nitrides (by sputtering) and oxides (by PLD) with sub-monolayer (0.5 nm) thickness control. The microelectronics industry has identified HfO_2, Hf-Si-O, and Hf-Si-O-N, among other high- gate dielectrics, as the leading candidate replacement materials for SiO_2; however, the selection of gate electrode materials to replace polysilcon is less advanced. Thus, we have focused our efforts on gate electrode materials, specifically metals (Ni-Ti-Pt ternary system) and metalloids ($Ta_{1-x}Al_xN_y$ system).

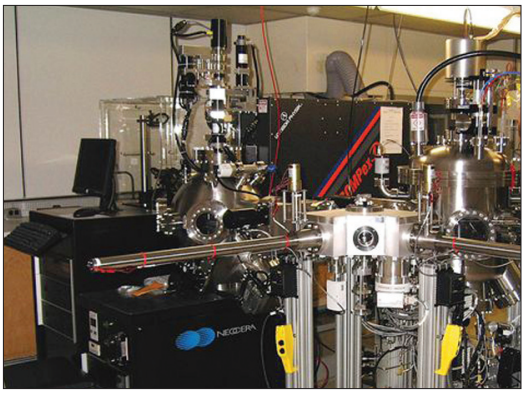

Figure 1. Combisystem1, "combinatorial thin film synthesis tool".

Shadow masks are used during thin film deposition, so etching is not needed to produce capacitor pillars. Each capacitor is individually addressable; the properties of 700 capacitors can be measured in 5 hours. In conjunction with the NIST Electronics and Electrical Engineering Laboratory, we have developed high throughput, automated methods to measure I-V and C-V properties of gate stack structures. From these measurements, the work function (φ_m) and leakage current density (J_L) can be determined. Work function values for a combinatorial Ni-Ti-Pt film library deposited by sputtering onto a HfO_2 dielectric film were determined for capacitors spanning nearly the full composition range of the ternary gate metal system. We also investigated the $Ta_{1-x}Al_xN_y$ system, a metalloid that is stable up to 950 °C and thus is

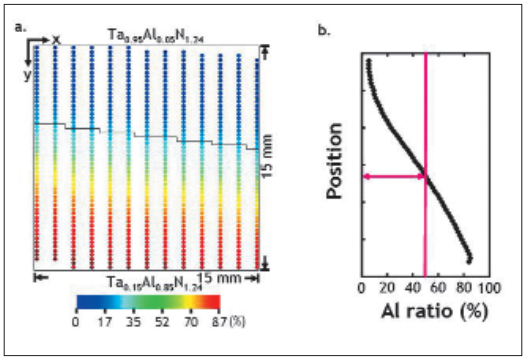

Figure 2. TaAlN1, "Capacitors (each dot) for a $Ta_{1-x}Al_xN_y$ library with $0.05 < x < 0.85$ and $y = 1.24$", and $TaAlN_2$, "Variation in φ_m with composition (x) for the metal gate electrode $Ta_{1-x}Al_xN_y$".

suitable for current "planar" integrated process manufacturing. A library with x varying between 0.05 and 0.85 was deposited onto a HfO_2 dielectric film by reactive sputtering, followed by a forming gas anneal (FGA) at 500 °C. After measuring the C-V and I-V curves, the library was subjected to 900 °C and 1000 °C rapid thermal anneals (RTAs). Work function values before and after the RTAs were compared. Our results on the $Ta_{1-x}Al_xN_y$ and Ni-Ti-Pt systems are the first reported comprehensive measurements of the dependence of work function on composition for ternary gate electrodes on high- dielectrics

Collaborations

IJoint combinatorial gate stack experiments with Intel, Qualcomm, Sematech and IMEC.

Recent Publications

Publications

K.-S. Chang, M. L. Green, J. Hattrick-Simpers, J. Suehle, I. Takeuchi, O. Celik, S. DeGendt, *"Determination of Work Functions in the Ta1-xAlxNy/HfO2 Advanced Gate Stack Using Combinatorial Methodology,"* (submitted to IEEE Trans)

M. L. Green, K.-S. Chang, S. DeGendt, T. Schram and J. Hattrick-Simpers, *"Application of Combinatorial Methodologies for Work Function Engineering of Metal Gate/High-k Advanced Gate Stacks,"* Microelectronic Eng., 84 (2007), 2209-2212.

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Talks

"Combinatorial study of metal gate electrodes on HfO_2 for the advanced gate stack," K.-S. Chang, Spring MRS 2008 (invited)

"Combinatorial Methodology for the Exploration of Metal Gate Electrodes on HfO_2 for the Advanced Gate Stack," K.-S. Chang, ECS Meeting, May 2008 (invited).

Advanced Plasma Process Metrology

Technical Contacts:
M. Sobolewski

"NIST is one of the leaders in plasma processing related research in the U.S. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools."

Peter Ventzek
TEL, Inc

Goals

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS, 2007 update) identifies a need for better, more predictive modeling of the impact of equipment on process results (Modeling and Simulation section, page 4 and Tables MS1, MS2a, and MS2b). To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, the dependence of these properties on processing equipment, and the effect of these properties on process results, further progress in model development and validation is required. The ITRS also identifies a need for development of robust sensors and process controllers (Metrology section, Table MET1 and pages 39-41, and Modeling and Simulation section, page 7) which are able to convert large quantities of raw data into information useful for improving manufacturability and yield.

Technical Strategy

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

First, we develop and evaluate a variety of measurement techniques that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

In addition to measurement techniques, we also provide data necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors. Our reactors include capacitively coupled cells as well as inductively coupled, high-density plasma reactors, one of which is shown in Fig. 1.

Finally, we are engaged in the development and validation of plasma models. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

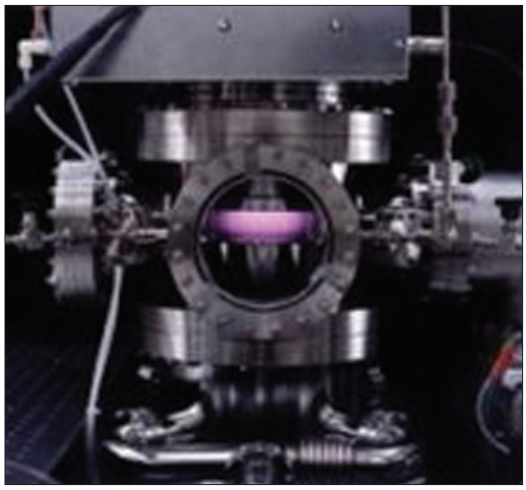

Figure 1. One of the inductively coupled plasma reactors in our laboratory.

"The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries."

Bing Ji,
Air Products and
Chemicals, Inc.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

1. Recently, several new kinds of wafer-based sensor technologies have been developed and commercialized. These technologies allow the integration onto test wafers of sensors that can measure important plasma and process parameters such as ion flux, ion energy, and wafer surface temperature. Integration of multiple sensors allows measurement of the uniformity of these parameters across the wafer surface. Such wafer-based sensors are playing an increasingly important role in the development and characterization of plasma processes and equipment. Often, however, the principles of operation of these sensors are not completely understood. Consequently, the reproducibility and accuracy of sensor measurements may be in doubt. A better fundamental understanding of these sensors, together with more rigorous, quantitative analysis of errors that may be present, could lead to improvements in sensor design and could greatly increase the use of such sensors in industry. Our planned efforts concentrate on validation of wafer-based measurements for ion flux and ion energy. We will compare wafer-based measurements of these parameters to independent measurement techniques of known accuracy that we have developed in previous years. Models for wafer electrical properties and ion dynamics in plasma sheaths that we have previously developed and rigorously tested will be applied to elucidate, on a fundamental level, how the sensors operate and to identify and quantify their sources of uncertainty.

DELIVERABLES:

- Evaluate the accuracy of wafer-based sensors for ion flux in rf-biased, inductively coupled plasma reactors. 2Q 2009
- Evaluate the accuracy of wafer-based sensors for ion energy in rf-biased, inductively coupled plasma reactors. 1Q 2010

2. For real-time process monitoring and control, other types of sensors are required. During an actual manufacturing process, a test wafer equipped with wafer-based sensors will not be present in the tool. There will instead be a product wafer undergoing processing. Other, more traditional measurement methods are similarly unsuitable for use during manufacturing, because they require that an invasive sensor or probe be inserted into the plasma. Such probes cause several problems, including the possibility that materials from the probe would contaminate the wafers being processed. Thus, to be practical for use in manufacturing, a monitoring technique must be noninvasive, i.e., it must not require any probe or test wafer be inserted into the plasma reactor. To meet this need, we have developed electrical measurement techniques that rely on noninvasive, nonperturbing measurements of the radio-frequency (rf) current and voltage applied outside the reactor. The rf measurements contain valuable information about the flux and energy of the ions that bombard wafers during processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of the plasma and its sheaths.

To validate the technique, experiments in an rf-biased, inductively coupled plasma reactor have been performed both with and without silicon wafers loaded in the reactor, on a metallic wafer chuck as well as an insulating chuck that is similar to commercial electrostatic chucks. Plasma potentials, sheath voltages, total ion flux, and ion energy

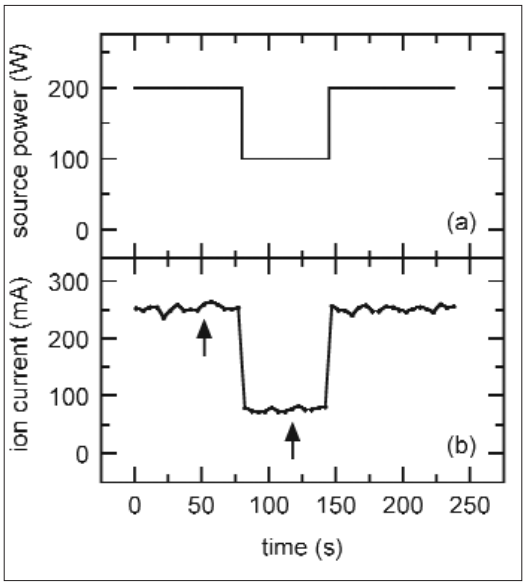

Figure 2. Effect of (a) variations in inductive source power on (b) total ion current at the wafer surface, as measured by the noninvasive technique, for a 50% Ar, 50% CF_4 plasma at a pressure of 10 mTorr, a bias frequency of 10 MHz, and a bias power of 10 W.

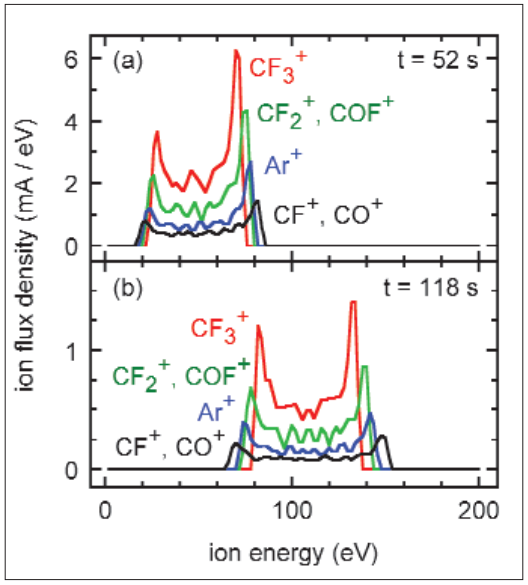

Figure 3. Ion energy distributions from the noninvasive monitoring technique, obtained during the experiment shown in Fig. 2, at (a) 52 s and (b) 118 s after the start of the experiment. The distribution for CF_2^+ and COF^+ has been expanded vertically by a factor of 3, for clarity.

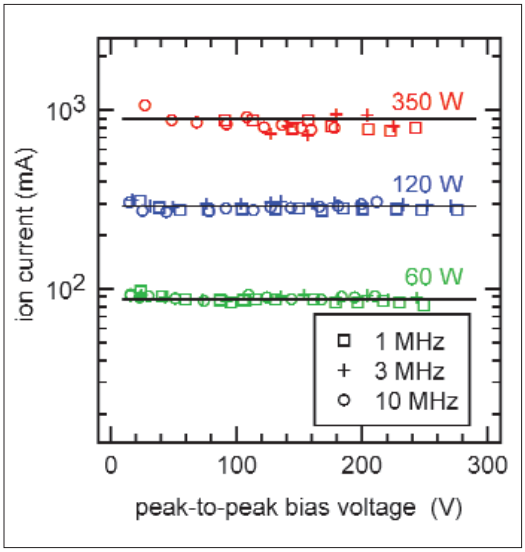

Figure 4. Noninvasive values of total ion current at the wafer (symbols) compared to independent measurements (lines) at inductive source powers of 60, 120, and 350 W, and bias frequencies of 1, 3, and 10 MHz, all at 1.3 Pa (10 mTorr), at a wafer on an insulating chuck.

distributions obtained from the rf measurements have been compared against independent measurements and shown to be in good agreement. The technique has been used to monitor long-term drift in ion energy and total ion flux. We have also monitored the more rapid changes that occur when the pressure, power, and gas flow are perturbed in ways that mimic equipment faults (see Figs. 2 and 3). Small changes in ion energy and total ion flux that occur over the course of an oxide etch have also been monitored. At present, we are investigating the origin of the changes that are observed during etching. The results of this investigation will enable us to evaluate the reliability of existing methods for electrical detection of etching endpoints, and perhaps develop new, more reliable ones. Future efforts also are directed toward demonstration of the usefulness of the noninvasive montoring technique in industrial plasma reactors, which may differ from our research reactors in several ways. For example, many industrial inductively coupled plasma sources are not operated in the high-density, purely inductively coupled mode, but are instead operated in a lower-density mode that couples power into the plasma both inductively and capacitively. We will perform experiments to test and validate the noninvasive technique in this mixed capacitive-inductive mode.

DELIVERABLES:

- Determine origin of changes in ion current observed during etching and evaluate electrical methods for endpoint detection. 3Q 2008
- Perform validation tests of noninvasive, rf-based ion flux and ion energy monitoring in an inductively coupled reactor operated in the low-density, mixed capacitive-inductive mode. 4Q 2008

Accomplishments

The NIST-developed, noninvasive, model-based electrical technique for monitoring ion energy and total ion current has recently been validated (private communication) in an rf-biased, inductively coupled reactor in which the usual, metallic wafer chuck was replaced by an insulating chuck similar to commercial electrostatic chucks. By including the capacitance of the insulating chuck in the electrical model used by the noninvasive technique, total ion current (Fig. 2), sheath voltages, and ion energy distributions were obtained with accuracies as good as that obtained with the metallic chuck. With either chuck, accuracy was excellent over the entire range of experimental conditions, except at very low bias voltages, which produce sheath voltages of only a few volts

and ion bombardment energies of only a few electron volts. Under such conditions, the rf current and voltage waveforms are dominated by electrons, not ions, and the uncertainty in the noninvasive technique becomes larger. Nevetheless, conditions that produce such low ion energies are unlikely to be used by industry for any practical plasma process.

We have also developed new algorithms that increase the speed of the noninvasive monitoring technique. Previously, information was extracted by fitting the measured current and voltage waveforms with waveforms output by a model of the plasma and its sheaths. This fitting process requires that the partial differential equations that make up the model be solved in real-time, which has limited the measurement and analysis time of the technique to a few seconds (1-4 s, depending on how many ionic species are included in the model). In the new algorithms, all model computations are done beforehand, and the model results are stored in tables. During the measurement, after acquiring a set of the current and voltage waveforms, one need only perform interpolations in the tables. This improvement reduces the cycle time of the measurement far below 1 s, making it suitable for use even in processes that are very short or in close-loop control schemes that require fast feedback.

In a collaboration with KRISS, the Korea Research Institute of Standards and Science, a new method for measuring electron number density in plasmas, the wave cut-off method, has been implemented in NIST laboratories. Unlike Langmuir probe measurements, which are commonly used for measuring electron density, cut-off measurements do not suffer from problems with rf compensation or deposition of insulating layers. Comparisons performed in one of our inductively coupled plasma reactors showed good agreement between electron densities measured by the cut-off probe and by a Langmuir probe. The accuracy of the cut-off probe was shown to be greater than the Langmuir probe. The cut-off probe has been used to characterize the spatial variation of the electron density in the inductively coupled reactor and the effect of rf substrate bias on the electron density. Interest in the bias effect has been stimulated by recently proposed, new methods for rf biasing, such as double-frequency bias and non-sinusoidal bias, which may contain Fourier components at frequencies higher than those previously used for biasing. Our measurements showed that even at bias frequencies as high as 30 MHz, the effect of bias on electron density is small, and therefore that nearly independent control of ion energy and ion flux can be maintained even at such high frequencies. Simple analytic models that describe the effect of bias on electron density, which would be useful for estimating such effects under other experimental conditions in other plasma reactors, have been derived and validated by the cut-off measurements. A manuscript describing these results has been written and published.

Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the Web-based NIST "Electron Interactions with Plasma Processing Gases" database. This Web site has experienced tens of thousands of hits throughout its history.

Recent Publications

M. A. Sobolewski and J.-H. Kim, *"The effects of radio-frequency bias on electron density in an inductively coupled plasma reactor,"* J. Appl. Phys. 102, article #113302, 1-13 (2007).

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M. A. Sobolewski, *"Effects of wafer impedance on the monitoring and control of ion energy in plasma reactors,"* J. Appl. Phys. 100, article #063310, 1-13 (2006).

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K. L. Steffens, M. A. Sobolewski, *"2-D Temperature Mapping in Fluorocarbon Plasmas,"* AIP Conference Proceedings, Vol. 788: Characterization and Metrology for ULSI Technology, (American Institute of Physics, Melville, NY, 2005) pp. 333-337.

M. A. Sobolewski, *"Noninvasive monitoring of ion energy in an inductively coupled plasma reactor,"* AIP Conference Proceedings, Vol. 788: Characterization and Metrology for ULSI Technology, (American Institute of Physics, Melville, NY, 2005) pp. 319-323.

M. A. Sobolewski, *"Monitoring sheath voltages and ion energies in high-density plasmas using noninvasive radio-frequency current and voltage measurements,"* J. Appl. Phys. 95, 4593-4604 (2004).

K. L. Steffens and M. A. Sobolewski, *"A technique for temperature mapping in fluorocarbon plasmas using planar laser-induced fluorescence of CF,"* J. Appl. Phys. 96, 71-81 (2004).

M. Edamura and E. C. Benck, *"Effects of voltage distribution along an induction coil and discharge frequency in inductively coupled plasmas,"* J. Vac. Sci. Technol. A 22, 293-301 (2004).

Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. A major new technology thrust over the past several years is the move to three dimensional integration. Environmental pressures have led to the reduction and elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the stacking of chips with via hole interconnect, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Atomic Layer Deposition – Process Models and Metrology

Technical Contacts:
J. E. Maslar
D. R. Burgess, Jr.

Goals

Develop validated, predictive process models and in situ metrologies for atomic layer deposition processes.

Customer Needs

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high-κ gate dielectric layers and DRAM dielectric layers. However, significant developmental issues remain for many of these applications.

One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the *International Technology Roadmap for Semiconductors (ITRS) 2007 Edition as "one of the few enabling methodologies that can reduce development cycle times and costs."* [ITRS 2007 Edition, Modeling and Simulation, page 1] A TCAD topical area identified in the ITRS 2007 Edition is *"Equipment/feature scale modeling—hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings."* [ITRS 2007 Edition, Modeling and Simulation, page 1] A difficult challenge related to this topical area is *"Integrated modeling of equipment, materials, feature scale processes and influence on devices"* [ITRS 2007 Edition, Modeling and Simulation, Table MS1, page 3] with associated issues including *"Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-products, rates ...), and simplified but physical models for complex chemistry"* and ALD deposition modeling. [ITRS 2007 Edition, Modeling and Simulation, Table MS1, page 3] In addition, the 2007 ITRS notes that *"a key difficult challenge across all modeling areas is that of experimental validation."* [ITRS 2007 Edition, Modeling and Simulation, page 2] Further, with respect to experimental validation, *"One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films and ultra-fine structures." [ITRS 2007 Edition, Modeling and Simulation, page 7]* This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and in situ metrologies for ALD processes.

Technical Strategy

This project involves two general directions of investigation: development of in situ metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supportive. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that important reaction species will be identified as the understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, it will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetics properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

Various in situ diagnostics are being evaluated for use in characterizing gas phase and/or surface processes. Gas phase diagnostic development has focused on metrologies that are sensitive to gas phase processes that can be ultimately related to film properties. Such diagnostics can be used to help optimize gas injection conditions rather than simply monitor precursor delivery. ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the gas flow and temperature fields in an ALD reactor. Experimental validation of the overall process model is accomplished by modeling the performance of a custom-built, research-grade ALD reactor with optimized optical accessibility and benchmarking the numerical results with experimental data. HfO_2 ALD using

tetrakis(ethylmethylamino) hafnium (TEMAH) and water has been selected as the chemical system for primary investigation.

1. A number of diagnostics are being evaluated for sensitivity to ALD chemistry and integration into deposition systems. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their proven potential for in situ monitoring. While sensors that are sensitive to gas phase species, e.g., mass spectrometry and semiconductor laser-based spectroscopic techniques, are easier to integrate into commercial reactors (e.g., in the gas exhaust line), these techniques are only sensitive to volatile and relatively stable species. Hence, it is sometimes difficult to relate the species detected with such techniques to mechanisms of interest on the growth surface. Hence, both gas-phase-sensitive and surface-sensitive techniques are being evaluated to probe ALD chemistry. The suitability of Fourier-Transform infrared (FTIR) spectroscopy and laser-based spectroscopic techniques for probing ALD surface processes under actual deposition conditions is being investigated. In addition, the suitability of mass spectrometry, FTIR spectroscopy, and semiconductor laser-based spectroscopic techniques for probing gas phase ALD processes and how best to relate gas phase species to important surface processes is being investigated. A research-grade ALD reactor with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques has been designed and constructed.

DELIVERABLES:

- Determine sensitivity to methylethylamine (a deposition product) of near IR semiconductor laser-based spectroscopic techniques. 2Q 2008
- Optimize quantum cascade laser system for probing HfO_2 ALD gas phase processes. 4Q 2008
- Evaluation of time-resolved, in situ diode laser absorption spectroscopy for measurements of water vapor during ALD processes. Ongoing
- Evaluation of time-resolved, in situ FTIR measurements for probing HfO_2 ALD gas phase processes. Ongoing
- Evaluation of mass spectrometry measurements for probing HfO_2 ALD gas phase processes. Ongoing

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD is an integral aspect of this project. The thermochemical properties and reaction kinetics of most organometallic precursors employed in ALD are poorly characterized. This project obtains these properties through theoretical estimates, comparison with available experimental data, and modeling. This involves compiling the available thermochemical and chemical kinetics data for organometallic precursors and related compounds. These data are supplemented with predictions from quantum calculations of molecular structures, spectroscopic properties, and thermodynamic functions. These quantities are then utilized to develop detailed chemical kinetics models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES:

- Compute vibrational spectra of common hafnium precursors and products. 2Q2008
- Produce manuscript on enthalpies of formation of organometallic (Al, Hf, Zr, Ga, Ti) precursors with comparison to compiled experimental data. 3Q2008
- Complete development of an ALD mechanism for HfO_2 deposition from TEMAH and water for incorporation into a two-dimensional CFD reactor model. 4Q2008

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of ex situ film characterization measurements to reactor conditions as determined by in situ measurements and numerical modeling of the temperature and flow fields in the reactor. In situ measurement techniques include those techniques being developed for model validation. Ex situ measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy (XPS), X-ray diffractometry, atomic force microscopy, ultraviolet Raman spectroscopy, and various electrical measurements. The data provided by these measurements, spatially resolved when possible, include such film characteristics as thickness, stoichiometry, HfO_2 phases present, degree and type of impurity incorporation, leakage current, and dielectric constant.

DELIVERABLES:

- Investigate the relationship between HfO_2 ALD process parameters, reactor gas flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics. Ongoing

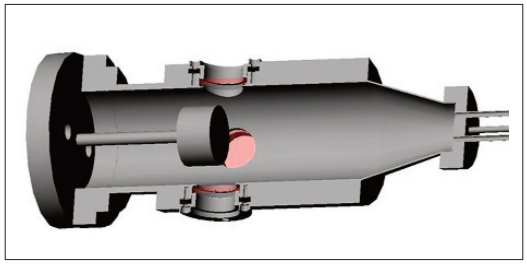

Figure 1. A schematic of the cross section of the reactor as configured with optical windows.

Accomplishments

■ ALD Reactor Design — An ALD reactor with diagnostic access near the wafer surface that exhibits operational parameters approximating some industrial single wafer reactors was designed and fabricated. Gas flow in the reactor near the wafer is laminar and parallel to the wafer surface normal with four diagnostic ports oriented perpendicular to the wafer surface normal, as shown in Fig. 1.

■ Diagnostic access does not significantly perturb gas flow, especially near the wafer surface. Using this reactor, reproducible, high-quality HfO_2 films can be deposited at the same time that in situ measurements are being performed. This reactor is being used to provide data to validate process models and develop metrologies.

■ HfO_2 Film Deposition — ALD HfO_2 films are being deposited under a variety of process conditions using tetrakis(ethylmethylamino) hafnium (TEMAH) and water. Films have been characterized with a number of techniques, including VUV-SE, XPS, FTIR, Raman spectroscopy, X-ray diffractometry, atomic force microscopy, and current-voltage measurements. Ex situ measurement results indicate that this reactor design can be used to reproducibly grow microelectronics-quality HfO_2 films.

■ ALD Reactor Modeling — Gas flow and temperature profiles in this reactor have been simulated using three dimensional CFD modeling, as shown in Fig. 2.

■ In addition, time-resolved precursor distributions have been modeled. The results from these models have been used to help optimize reactor designs, especially optical window design, and deposition conditions, as well as interpret in-situ measurements. Chemical reaction mechanism models for HfO_2 ALD are being developed for use with these three dimensional flow and temperature models to simulate the entire ALD process.

■ *In-Situ* Measurements — *In-situ* gas phase FTIR measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to deposition reactants, TEMAH, and products, methylethylamine, as illustrated in Fig. 3

■ In addition, in-situ, time-resolved diode laser-based water vapor absorption measurements were performed during ALD cycles. The water absorption signal measured in the presence of a wafer with completely saturated surface reaction sites can be simulated very well with CFD reactor models, as shown in Fig. 4.

■ A quadrupole mass spectrometer has also been used to monitor volatile species present

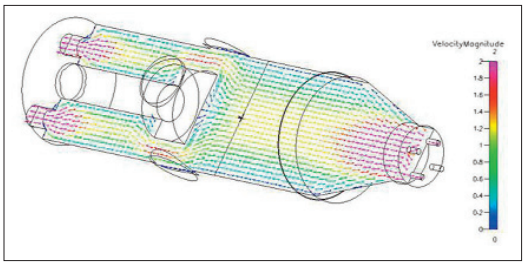

Figure 2. A cross section of the helium carrier gas velocity distribution in the diagnostic-accessible reactor under typical deposition conditions (obtained from a full three dimensional simulation).

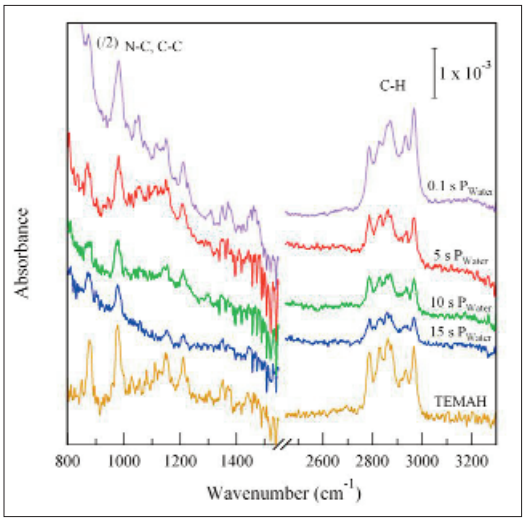

Figure 3. Gas phase FTIR spectra as a function of purge time following a water pulse.

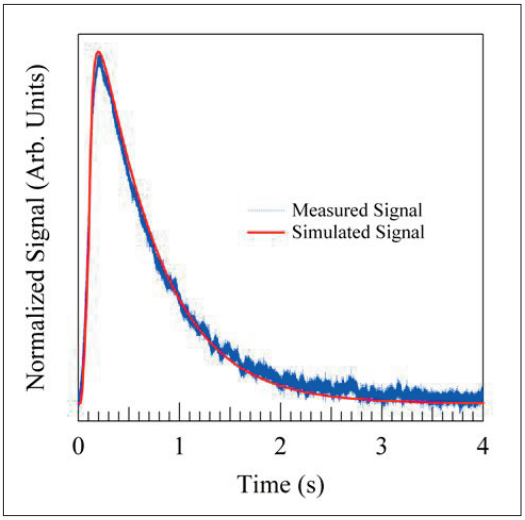

Figure 4. Diode laser-based water vapor absorption measurements and simulations.

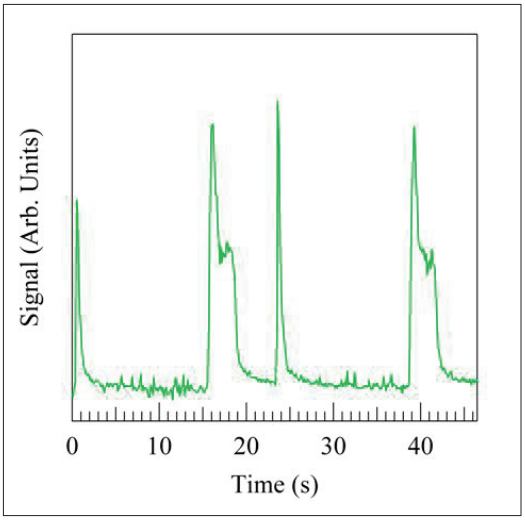

Figure 5. Mass spectrometric measurement of mass-to-charge ratio representative of methylethylamine during ALD cycles.

during ALD, including methylethylamine as illustrated in Fig. 5

■ Chemical Properties Calculations — Molecular structures and energies for precursors, intermediates, and products have been calculated using quantum chemical methods for ALD of HfO_2 from TEMAH/tetrakis(dimethylamino) hafnium (TDMAH) and water. Supplementing these data are calculations for organometallic and halide precursors used in deposition processes for other systems with a variety of ligands (alkyl, alkoxy, amino). Comparisons are made between the calculated predictions and experimental data to develop reliable and self-consistent values. A detailed chemical kinetics model for ALD of HfO_2 from TEMAH and water is being developed and refined based on reactor model simulations and comparison with experimental observables.

■ Reference Spectra Development — Reference spectra of TEMAH, MEA, dimethylamine (a volatile product of the TDMAH and water reaction), and diethylamine (a volatile product of the tetrakis(diethylamino) hafnium and water reaction) were recorded in the near IR and mid IR spectral regions. The measured mid IR vibrational frequencies were compared to vibrational frequencies that were calculated with DFT (Density Functional Theory) using B3LYP (Hybrid DFT method, B3 stands for 3 parameter exchange functional developed by Becke; LYP stands for a correlation functional (developed by Lee, Yang, and Pau) theory with LANL2DZ (LANL2DZ is a basis set used for the calculations developed at Los Alamos National Laboratory (LANL) and it is a double zeta quality, thus 2DZ) basis set, as shown in Fig. 5 for TEMAH and MEA.

■ In the infrared spectra, vibrational modes in the CH wavenumber range were scaled by 0.95 and the modes in the lower wavenumber range were scaled by 0.961. Near IR spectra are necessary to design semiconductor laser-based spectroscopic techniques utilizing relatively inexpensive telecommunications lasers. MEA, dimethylamine,

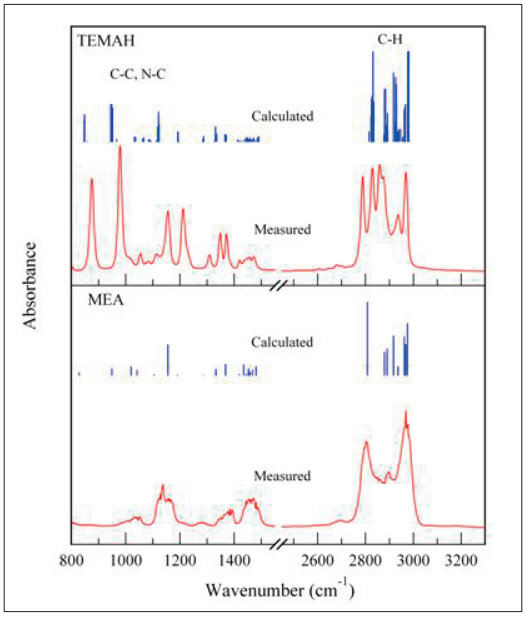

Figure 6. Comparison between calculated and measured spectra of TEMAH and MEA.

and diethylamine spectra are useful for other than just HfO_2 ALD from Hf-containing alkyl amines. These compounds are the primary reaction products in water-based thermal ALD employing other metal alkyl amines, e.g., tetrakis(diethylamino) zirconium and tetrakis(ethylmethylamino) silicon.

■ Database Website — A Website http://kinetics.nist.gov/CKMech has been made available. This site contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes, including information pertaining to ALD and CVD of aluminum, Al_2O_3, and other related ALD systems (e.g., Zr, Hf, etc.), as well as a significant amount of information pertaining to hydrocarbon-based reactions.

Recent Publications

J.E. Maslar, W.S. Hurst, D.R. Burgess, W.A. Kimes, N.V. Nguyen, E.F. Moore, J.T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* ECS Transactions (in press).

J. E. Maslar, W. S. Hurst, D. R. Burgess, Jr., W. A. Kimes, N. V. Nguyen and E. F. Moore, *"In Situ Monitoring of Hafnium Oxide Atomic Layer Deposition"* in Frontiers of Characterization and Metrology for Nanoelectronics, D. G. Seiler, A. C. Diebold, R. McDonald, C. M. Garner, D. Herr, R. P. Khosla and E. M. Secula Editors, p. 121, American Institute of Physics, Melville, NY (2007).

J. E. Maslar, W. S. Hurst, D. R. Burgess, Jr., W. A. Kimes, and N. V. Nguyen, *"In Situ Characterization Of Gas-Phase Species Present During Hafnium Oxide Atomic Layer Deposition,"* ECS Transactions 2, 133-143 (2006).

Advanced Nanoscale and Mesoscale Interconnects

Technical Contacts:
T. P. Moffat
D. Josell

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations for both on-chip, chip stacking, and MEMS applications, examining the generality of the superconformal filling mechanism, expanding the applicable materials set, and exploring processes utilizing novel barriers and/or seed geometries. This is complemented by surface chemistry studies aimed at understanding and optimizing the feature-filling process.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever-smaller dimensions has led to the rise of new challenges, including fabrication of ever-thinner copper seeds, which are required for the copper superfill process and increased resistivities of the metallizations due to size effects. At the same time a strong movement towards 3-D integration of integrated circuits (i.e. chip stacking) is under way. This involves the replacement of long horizontal conductors by short vertical interconnections; in addition to an improved RC response, the new architecture enables integrations of heterogeneous devices. Many challenges to the fabrication through-silicon-vias (TSV) remain that require an understanding of the surface chemistry of copper. To help overcome these hurdles, the National Institute of Standards and Technology (NIST) is enhancing existing copper technology through improved understanding of the surface chemistry and metrologies for the superfill process, examining new interconnect materials, and pursuing new fabrication techniques such as seedless processing and atomic layer deposition. Similarly, there is also increasing interest in expanding the materials set available for constructing 3-D MEMS architectures. In this regard NIST has begun exploring the integration of ferromagnetic materials into Damascene processing.

Interconnect metallization issues are discussed in the Interconnect section of the 2007 update of the International Technology Roadmap for Semiconductors.

Technical Strategy

To meet future industrial needs, we have, over the life of this project, developed metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill features over a wide range of length scales. The derived Curvature Enhanced Accelerator Coverage (CEAC) mechanism has served as a platform for this understanding. A key element to bottom-up surperfilling is the competition between deposition rate suppressing polymers and rate accelerating sulfonated alkythiols (and/or disulfides) for copper surface sites. In the case of on-chip interconnects an important consequence of bottom-up superfilling is the overshoot phenomenon known as "momentum plating" that can lead to bump formation above filled features. These bumps greatly hamper subsequent planarization processes. However, the overshoot process may be controlled by the addition of certain cationic surfactants to the copper plating baths. In a related manner, cationic surfactants exert an even greater influence on the filling of larger scale TSV's geometries. In close collaboration with , we are using a variety of electroanalytical and feature-filling experiments that help establish strategies for quantifying and understanding the influence of surfactants on film growth over a range of length scales. Through this activity the CEAC model was successfully extended to explain and predict the filling behavior during deposition from complex plating baths containing combination of suppressors, accelerators, and levelers.

In parallel with this effort a variety of surface analytical studies, *e.g.* ellipsometry, XPS, and *in-situ* STM, are under way to directly probe the competitive adsorption dynamics between multiple additives and the copper surface in order to provide molecular level insight into additive function and design. Particular attention is given

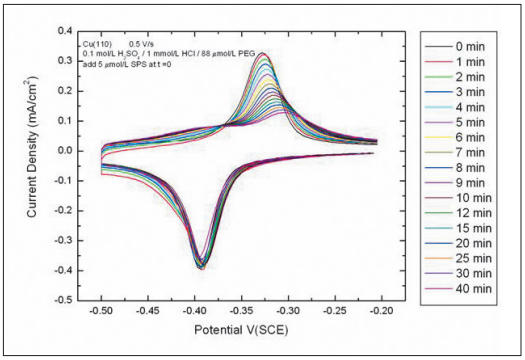

Figure 1. An in-situ scanning tunneling microscopy image revealing sulfur atoms (four bright spots) within an adsorbed chloride monolayer (square grid of atoms) on a Cu(100) single crystal surface)

to the role of potential-dependent adsorption processes that are central to the performance of the copper pulse plating method used to form TSVs. The competitive and co-adsorption of surfactants relevant to superfilling may be monitored and quantified by voltammetry as shown in Fig 1. These studies are complemented by in STM examinations of the surface structure and dynamics as shown in Fig 2. Close attention is being given to connecting the results of the single crystal studies with feature-filling experiments.

DELIVERABLES:

- Publications using surface and electroanalytical probes to independently quantify adsorbate coverage and dynamics relevant to superconformal feature filling. 4Q 2008.

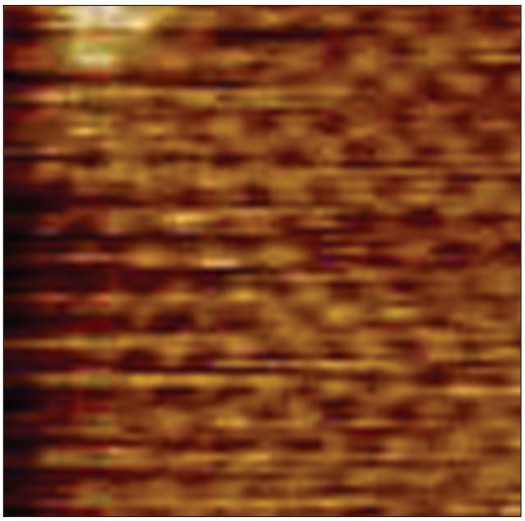

Figure 2, Atomically-resolved in-situ STM image of individual sulfide species (bright spots) within the ordered c(2x2) chloride adlayer (square grid). The Cl-Cl separation is 0.36 nm.

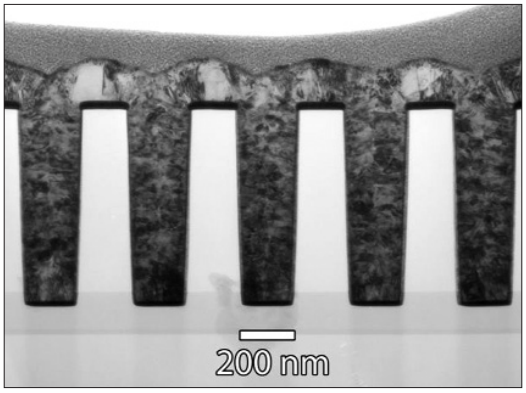

Figure 3. Void-free nickel filled trenches formed by electroplating from a $NiSO_4$-$NiCl_2$-H_3BO_3 electrolyte containing a single benzimidazole derivative.

The generality of the bottom-up superfilling process to the application of other material systems in ULSI and MEMS remains a subject of great interest. In addition to silver (the only metal with a higher conductivity than copper) and gold (a metallization for wide-bandgap semiconductors) the prospect for deposition of iron group metals (for MEMS and magneto-electronic circuitry) has been examined. Most recently, a simple solution for integrating nickel and nickel-iron alloys (Permalloy) into the Damascene processing has been demonstrated. As shown in Fig. 3, the addition of a simple benzimidazole derivative to a nickel plating bath enables void-free filling of trenches.

DELIVERABLES:

- Publications detailing the first manufacturable example of deposition of conducting magnetic materials for Damascene metallization. 2Q 2008 and 4Q 2008

In addition to the electrodeposited copper conductor itself, current metallization technology employs a barrier metal and a PVD copper seed. As feature sizes continue to shrink, the resistive barrier materials negatively impact electrical performance, and deposition of, and on, the PVD seed becomes problematic. These difficulties are driving a search for alternative barrier/wetting layer materials and processes. Ruthenium is one focus because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers, it is immiscible with copper, and copper can be electroplated directly on it, eliminating the need for the PVD copper seed layer and the corrosion problems that come with it. In the past we have demonstrated direct

copper superfilling on Ru, Os, and Ir barrier/adhesion seed layers as well as appropriate metrological aspects required for process control. This work continues with the evaluation of state-of-the-art ALD WN-XN novel barrier materials.

DELIVERABLES:

- Publications detailing seedless superfilling copper on WN-based ALD layers and measurement of the resulting electrical behavior. 4Q 2008

Accomplishments

■ The existing CEAC model of superfilling was extended to include the effect of leveling additives along with the metrology required for assessing the kinetics of the competitive adsorption process. The impact of leveling additives on overfill bump formation during trench filling was demonstrated using prototypical cationic surfactants.

■ Void-free superconformal deposition of nickel and nickel-iron alloys was demonstrated by the addition of a simple benzimidazole derivative to the electrolyte. Filling proceeds by a new mechanism that involves transient breakdown of an inhibiting molecular layer that is coupled with the trench geometry in a manner that enables void-free filling.

■ A range of electroanalytical and surface analytical studies are well under way to quantify the competitive and co-adsorption processes associated with copper superfilling additives. A combination of surface analytical and electroanalytical methods was used to reveal a.) difference in adsorption behavior between rate accelerating thiols versus disulfides, b.) irreversible adsorption of thiols and disulfides versus reversible adsorption of halide and PEG, c.) inhibition of PEG adsorption by a pre-adsorbed sulfonate-terminated thiol or disulfide monolayer film, and d.) displacement of the deposition rate inhibiting PEG layer by adsorption of the sulfonate-terminated thiol or disulfide accelerator.

Collaborations

D. Wheeler, C.H. Lee, J.E. Bonevich, M.L. Walker, L.J. Richter, P.J. Chen, W.F. Egelhoff: NIST.

Christian Witt: AMD.

R. Gordon, Harvard University.

C.S. Allen, E. Reddington, Z. Niazimbetova and M. Lefebvre

Recent Publications

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C.H. Lee, J.E. Bonevich, J.E. Davies and T.P. Moffat, *"Magnetic Materials for 3-D Damascene Metallization: Void-free Electrodeposition of Ni and Ni70Fe30 Using 2-Mercapto-5-benzimidazolesulfonic Acid,"* J. Electrochem. Soc., in press (2008).

S-K. Kim, J.E. Bonevich, D. Josell and T.P. Moffat, *"Electrodeposition of Ni in Submicrometer Trenches,"* J. Electrochem. Soc., 154, D443 (2007).

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D. Josell, T. P. Moffat and D. Wheeler, *"Superfilling When Adsorbed Accelerators Are Mobile,"* Journal of the Electrochemical Society, 154(4), D208-D214 (2007).

T. P. Moffat, D. Wheeler, S. K. Kim and D. Josell, *"Curvature Enhanced Adsorbate Coverage Mechanism for bottom-up superfilling and bump control in damascene processing,"* Electrochimica Acta, 53, 145 (2007).

D. Josell, *"A paradigm for interconnect geometry to reduce grain boundary resistance,"* J. Appl. Phys., 100, 123705 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, *"Cationic Surfactants for the Control of Overfill Bumps in Cu Superfilling,"* J. Electrochemical Society, 153 (12), C826-C833 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, *"Electrodeposition of Cu in the PEI-PEG-CL-SPS Additive System: Reduction of Overfill Bump Formation During Superfilling,"* J. Electrochemical Society, 153 (9), C616-C622 (2006).

M. Walker, L. J. Richter, and T. P. Moffat, *"Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study,"* Journal of the Electrochemical Society 153(8), C557-C561 (2006).

T. P. Moffat, D. Wheeler, S.-K. Km and D. Josell, *"Curvature Enhanced Adsorbate Coverage Model for Electrodeposition,"* Journal of The Electrochemical Society, 153(2) C127-C132 (2006).

D. Josell, D. Wheeler and T. P. Moffat, *"Gold Superfill in Submicrometer Trenches: Experiment and Prediction,"* Journal of the Electrochemical Society, 153(1) C11-C18 (2006).

Nanoporous Thin-Film Metrology for Low-k Dielectric Materials

Technical Contacts:
C. L. Soles

Goals

This project addresses critical development and integration issues with the interlayer dielectric (ILD) insulator materials needed for semiconductor interconnect applications by developing measurement methodologies to quantify their porous structures and related properties. This is accomplished by working closely with industry and academia to develop and apply these methods on state-of-the-art materials and processes that are leading candidates for next generation integrated circuit applications. Our measurement infrastructure has evolved around a synergistic packaging of specular X-ray reflectivity (SXR), X-ray porosimetry (XRP), and small angle scattering using both neutrons and X-rays (SANS and SAXS). In cases where the chemical composition of the film is unknown, we have also developed a suite of ion beam scattering techniques including Rutherford backscattering spectroscopy (RBS), grazing angle backscattering (GBS), and forward recoil elastic spectroscopy (FRES) to extract the chemical composition data that is needed for our other measurements. With this platform we can provide high quality data and measurements of the film thickness, density, coefficient of thermal expansion (CTE), moisture uptake, porosity, pore size distribution, wall density within a porous matrix, and even the degree of order in the pore structures. Over the past decade we have used these measurements to help guide materials development in the interconnect community. More recently we have been transferring and modifying this suite of measurement technologies to address integration issues. Specifically, we are focusing on how the various ashing, etching, deposition, or chemical mechanical polishing (CMP) processes that tend to alter or damage the final structure of the porous material. We now have a greater emphasis on the process induced damage to the critical pore characteristics moreso than materials development, to reflect the current industrial focus. Integration issues are currently the greatest concern when trying to implement porous ILD materials into functional CMOS devices. Lastly, we have also be merging our nanoporous characterization tools with our critical dimension metrology or pattern shape measurements base on SAXS and SXR to look at porous patterned low-k dielectrics, moving away from the planar film geometry.

Customer Needs

The continued scaling or shrinking of the integrated circuit (IC) requires new, more efficient ILD materials to combat the growing problems of a rapidly increasing power density on the chip, greater signal propagation delays due to the RC time constant, and increased cross-talk between the adjacent interconnects that continue to be squeezed closer together. The solution has been to develop low dielectric constant (low-κ or ultralow-κ) materials that incorporate nanometer scale pores to lower their effective dielectric constant. While this recognized approach is effective in meeting the ultralow-κ dielectric constant target, introducing porosity simultaneously compromises many of the other properties that are equally as important such as mechanical strength, thermal conductivity, thermal expansion, and the crucial barrier properties (i.e., resistance to Cu ion migration or moisture uptake) of these highly porous materials. Likewise the integration process exposes these materials to harsh conditions, including mechanical stresses under a caustic environment in CMP polishing, ashing and etching induced degradation of the material, and thermally generated stresses resulting from the CTE mismatch of dissimilar materials and the large and rapid temperature changes in the back end of the line (BEOL) processes. All of these processes tend to damage or degrade the porous structures. Developing a material that is optimized to meet all of these conditions has been an enormous challenge. There is still currently no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates have included silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. Irrespective of the candidate materials, there is a strong need for high quality structural data to understand correlations between applied processing conditions and the final physical properties. Only through quantitative nanoscale measurements will materials engineers have the proper feedback to know how a process affects the porous material and to then rationally design new materials that are suitable to withstand the harsh integration processes associated with CMOS fabrication.

Technical Strategy

While the field of porosimetry is broad and generally well-established, the small sample sizes (typically films less than 1 μm thick) and the desire to characterize materials *in-situ*, directly on an actual silicon wafer, greatly narrows the number of suitable measurement methods. Therefore a suite of measurement techniques that are especially sensitive to samples in the thin film geometry have been developed at NIST. When combined, these techniques can fully characterize the properties that are critical for ILD applications. The measurement techniques include various combinations of our reflectivity techniques (SXR and XRP), small angle scattering (SANS and SAXS), and ion beam scattering methods (RBS, GBS, and FRES) to determine important structural and physical property information in porous films less than 1 μm thick. These measurements are performed directly on films supported on thick silicon substrates, meaning that actual processing effects can be investigated.

The elemental composition of the analyzed material is often needed to convert the scattering length densities obtained from our X-ray and neutron techniques into a more meaningful physical density. For the case of unknown or proprietary ILD materials, we have developed RBS & GBS ion beam techniques to determine the Si, C, and O (or other elements other than H) content of the film while the FRES ion beam technique quantifies the H content. In all of these techniques a beam of high-energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy and angle. We have developed a method to fit the spectra and then compute the absolute ratios of the C, O, Si, and H in the film. From chemical composition, we can convert the scattering length densities into the physical or mass density of the film.

SANS and SAXS are transmission scattering techniques well-suited for characterizing critical length scales of the porous networks. Inclusions in the film of a different scattering length density than the matrix lead to small angle scattering when their length scales are on the order of 5 to 500 nm. By modeling the diffracted intensity as a function of the scattering vector, one can determine parameters such as the pores size, the pore size distribution, the inter-pore spacing, and the periodicity with which the pores are distributed. For ordered porous structures this reveals the symmetry or periodic lattice on which the pores are distributed. In the case of SANS, a powerful contrast matching technique can be used by mixing hydrogenated and deuterium substituted organic condensate vapors (such as toluene). At a critical concentration the hydrogenated-deuterated mixture of solvents will have exactly the same scattering length density as the matrix. By controlling the partial pressure of this mixture, the vapor can be selectively condensed inside the pores of a given radius (governed by the critical radius for capillary condensation), thereby rendering the condensed pores "invisible" to the scattering technique. This is an extremely powerful method to specific size dependent information about the population of pores.

High-resolution XR is an established, powerful technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. In addition, changes in the density profile from processing or post-application treatments can be determined. The CTE is determined from measurements of the film thickness at different temperatures. More recently, we have been extending the characterization with XR measurements to the lateral or in-plane dimensions of nanopatterned structures using an effective medium approximation. The density measurements are averaged over lateral length scale larger than the coherence length of the X-ray source. In the limit of periodic patterns, the density profile as a function of height conveys information about the average line to space ratio (or the equivalent patterned volume to unpatterned volume ratio for non-linear structures) as a function of pattern height. When these line-to-space ratios are coupled with a precise measure of pattern pitch or periodicity from a SAXS or SANS measurement, one can characterize the entire pattern cross section as a function of height.

Our final measurement tool couples SXR measurements with a mechanism of capillary condensation of a volatile organic penetrant to form a quantitative porosity measurement tool known as X-ray Porosimetry (XRP). As shown in Figure 1, we recently published NIST Recommended Practice Guide, Special Publication 960-13, entitled "Poros-

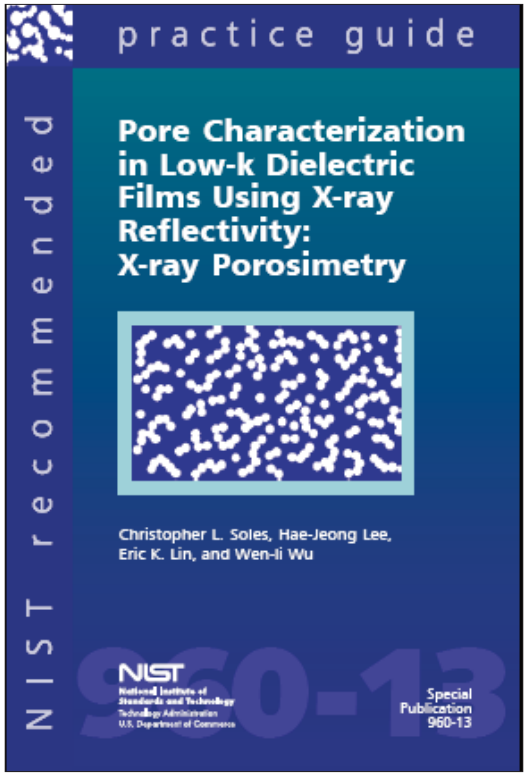

Figure 1. Cover of the XRP Recommended Practice Guide

ity Characterization in Low-k Dielectric Films Using X-ray Reflectivity: X-ray Porosimetry," that describes these measurements in detail. XRP is a simple yet powerful technique that can quantify the average density of a porous interlayer dielectric, the density of the "wall" material between the pores, the total porosity, and even the pore size distribution. Copies of this Recommended Practice Guide are available for free download through our website:http://polymers.msel.nist.gov/PDF/X-ray_Porosimetry_Recommended_Practice.pdf.

DELIVERABLES:

- Measure and report the impact of processing on the integrity of porous structures in nanoporous ILD materials

The semiconductor industry has successfully integrated nanoporous materials as inter level dielectrics (ILD) in the latest generation of devices. A major issues has been the understanding and predicting the impact of processing using wet and dry etching techniques aft the critical properties of these ILD materials. In general processing tend t to alter the mechanical and chemical integrity, and thereby the effective dielectric constant of the dielectric stack. Measurements techniques are needed to assay and quantify the extent of damage induced by such processing,

DELIVERABLES:

- Extend X-ray porosity characterization techniques from planar films to patterned nanoporous structures.

Our porosity characterization measurements thus far have focused on planar, non-patterned low-κ films. While this has been successful in the early stage evaluation of candidate materials, our techniques are starting to loose traction for the integration issues where patterned low-κ structures are of interest. It is therefore critical to extend our measurements to patterned low-κ materials. Recently, we have shown that the effective medium approximation is valid for the nanoscale periodic patterns of the size scale that are of interest to the semiconductor industry. This means that we can characterize the average density as a function of height through a nanoscale pattern. In periodic linear grating patterns, this average density defines the line-to-space ratio as a function of height. When coupled with an accurate knowledge of the pattern periodicity, we can define the average pattern width as a function of pattern height. Now that we have shown that the average density within the patterned material can be characterized, the next step is to see how the density changes when a probe molecule is condensed inside the pores of the patterned material. This will allow us to determine the porosity and wall density of the patterned material as a function of pattern height, extending the use of XRP from planar to patterned structures.

DELIVERABLES:

- Characterize the fidelity and porosity of nanoporous material patterned by nanoimprint lithography.

There is a growing interest within the Integrated Circuit (IC) community to directly pattern spin-on organosilicate ILD materials by nanoimprint lithography (NIL). It has been shown that by imprinting the ILD material with a multi-level nanoimprint template to directly fabricate a T-gate type structure, one can greatly reduce the number of lithography, deposition, and etching steps in the back end of the line process. This could *significantly* reduce manufacturing costs. Efforts this year will synergistically couple our expertise in thin film nanoporous X-ray metrology with our

simultaneous efforts in NIL metrology development. Specifically, we will adapt our XR shape metrology to quantify the fidelity of the nanoimprint process to evaluate the quality of the patterned ILD materials. We will also adapt our XRP measurements on patterned samples to quantify how the NIL process itself affects the pore structure. These measurement techniques will quantify the feasibility of NIL processes for back end of the line interconnect fabrication schemes. This is a topic that all of the major NIL tool companies are actively engaged in.

Accomplishments

■ Back in 2006 we formally completed our contract work with the SEMATECH (ISMT) Interconnect program, under which we have evaluated over 180 candidate films for ISMT. These films have been characterized in terms of their thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density / chemical composition by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and distributed to member companies. Additional measurements were performed on specific samples for further analysis using methods such as additional SANS configurations or X-ray porosimetry. These measurements were critical in helping the industry rationally narrow the wide field of candidate materials for next generation ILD materials.

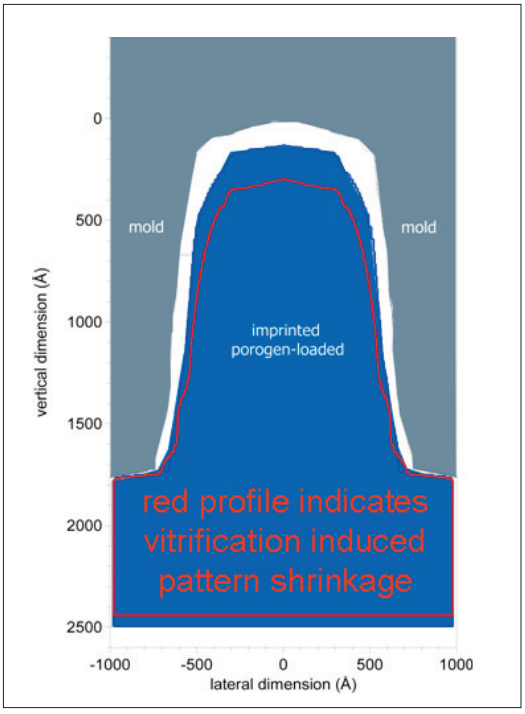

Figure 2. Cross-sectional profiles derived of the as imprinted pattern, before vitrification, (blue) relative to the mold (grey) indicating the shrinkage upon imprinting.The red curve indicates the additional shrinkage that occurs after the high temperature vitrification.

■ It is clear that porous version of the interconnect materials are generally more susceptible to damage by the plasma process encountered in BEOL integration. So while our the traditional focus in terms has been on optimizing the pore structure of an interconnect material in term of the pristine dielectric constant, materials developers and integration engineers are now worried about how the integration process alter the dielectric constants and lead to the concept of "effective k," or the dielectric constant after integration. In an effort to help quantify this notion of an effective k, we recently teamed with colleagues at Intel to systematically quantify how the plasma, etching, and ashing processes induce a dense skin on the surface of the dielectric films. Using X-ray reflectivity, our recent Applied Physics Letters article illustrates how we can quantify the thickness, density, and porosity of this damaged skin. This establishes a quantitative language for the materials development people to speak with the process engineers and try to minimize losses of the effective k during integration.

■ For cost reduction purposes, there is the desire to eliminate or simplify several of the integration steps in BEOL. An alternative is to introduce NIL processes to directly pattern the low-k dielectric material. As described above, this can completely eliminate several of the etching and ashing processes that result from transferring a resist pattern into a dielectric layer; directly patterning the dielectric material itself can completely eliminate several of these pattern transfer steps that lead to the increase in the effective k. This concept of directly patterning the ILD materials was originally introduced in 2006 by Professor Grant Willson's group. However, to date the only examples of this type of patterning have been on very low modulus materials with relatively high dielectric constants that would not be suitable for current ILD applications. This year we showed that ILD materials with an intrinsic dielectric constant on the order of 2.0 and a sufficiently high modulus could be directly patterned with NIL with very high fidelity. This demonstration was made possible through high

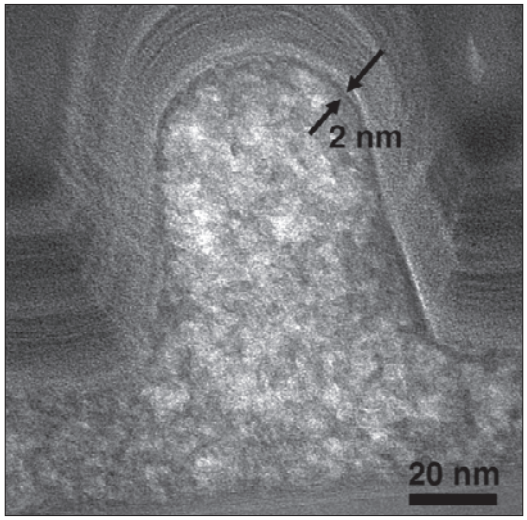

Figure 3. A cross-sectional TEM image of imprinted nanoporous pattern showing the densified skin layer approximately 2 nm thick.

resolution critical dimension measurements on both the NIL mold and the imprinted pattern. Using a combination of SXR and SAXS shape measurements, we showed that the pattern shape in the imprint mold could be transferred to the ILD material with extremely high fidelity, even through the high temperature vitrification stage where the spin on organosilicate is condensed into a hard, ceramic-like material. This vitrification process is usually associated with shrinkage of the material. As shown in the figure above, our measurement show pattern shrinkage in all dimensions, not only relative to the mold immediately after imprinting, but also after the free standing pattern is vitrified at 430 °C. Our pattern shape measurements are able to define the pattern fidelity throughout the entire process. These seminal pattern shape measurements were described in a high profile *Advanced Materials* article.

■ We also quantified the impact of NIL patterning process on the critical porosity of these low-k materials. We developed a variant of XRP that is applicable to patterned materials and were able to extract the porosity as a function of pattern height. When combined with complimentary positron annihilation lifetime spectroscopy and cross-sectional transmission electron microscopy (TEM) measurements, this study revealed an NIL induced dense skin on the surface of the porous pattern, on the order of a few nm in thickness. The cross sectional TEM image to the left shows evidence of this dense skin, which is highly attractive from an application point of view. Integration processes often require the addition of a densified skin on the ILD pattern to reduce interdiffusion. That NIL could intrinsically induce this barrier layer is highly attractive. These findings were also published in a second *Advanced Materials* article.

■ To a large extent, our successes in the direct NIL patterning of ILD materials were enabled by our access to state-of-the-art ILD materials. As materials development is out of the scope of the NIST mission, we have augmented our measurements development by partnering in an open collaboration with Seoul National University. Our group has formal Memorandum of Agreement signed with Professors Do Yeoung Yoon (Chemistry Department) and Kookheon Char (Chemical Engineering) that bring their materials development expertise to our laboratory through a formal student and postdoc exchange program. One clear example is the direct imprinting of the ILD materials. Critical to the success of this effort was access to a spin-on ILD material with sufficient modulus/hardness to withstand the mechanical deformation processes. Professor Yoon's group is internationally known for developing some of the highest modulus spin-on organosilicate materials to date. Through this agreement, our high power measurement methods have also been instrumental in helping develop and understand the structural basis for these high modulus materials (also published in *Advanced Materials* – see below). All of these data have been published in the open literature for the benefit of the entire community. Throughout the process of imprinting these ILD materials, our partners at Seoul National University have been an active partner.

Collaborations

Polymers Division, NIST – Hae-Jeong Lee, Hyunwook Ro, Ronald L. Jones, Wen-li Wu, Eric Lin.

International SEMATECH/Intel - Youfan Liu.

University of Massachusetts-Amherst – James Watkins.

IBM – Qinghuang Lin, Robert Miller.

Seoul National University – Kookheon Char, Do Yoon.

University of Michigan - David Gidley.

Kyoto Institute of Technology – Hiroshi Jinnai.

Recent Publications

H. W. Ro, H.-J. Lee, E. K. Lin, A. Karim, D. R. Hines, D. Y. Yoon, and C. L. Soles, *"Nanoimprint Lithography for the Direct Patterning of Nanoporous Interlayer Dielectric Insulator Materials,"* Emerging Lithographic Technologies XI, Ed. Michael J. Lercel, Proc. of SPIE, 6517, 651715 (2007).

H. J. Lee, C. L. Soles, H. W. Ro, S. Kang, E. K. Lin, A. Karim, W.-l. Wu, D. R. Hines, *"Characterizing Pattern Structures Using X-ray Reflectivity, Metrology, Inspection, and Process Control for Microlithography,"* XXI, Ed. Chas N. Archie, Proc. of SPIE, 6518, 651813 (2007).

C. L. Soles, H.-J. Lee, B.D. Vogt, E.K. Lin, and W. Wu, *"Structure Characterization of Nanoporous Interlevel Dielectric Thin Films With X-Ray and Neutron Radiation,"* in Dielectric Films for Advanced Microelectronics,Ed. Mikhail Baklanov, Martin Green, Karen Maex, John Wiley and Sons Publisher , West Sussex, England (2007) p100.

H. W. Ro, K. Char, E.-C. Jeon, H.-J. Kim, D. Kwon, H.-J. Lee, J. K. Lee, H. W. Rhee, C. L. Soles, D. Y. Yoon, *"High Modulus Spin-On Organosilicate Glasses for Interlayer Dielectric Applications,"* Advanced Materials 19, 705 (2007).

H. Wook Ro, R. L. Jones, H. Peng, D. R. Hines, H.-J. Lee, .E. K. Lin, A. Karim, D. Y. Yoon, D. W. Gidley, C. L. Soles, *"The Direct Patterning of Nanoporous Interlayer Dielectric Insulator Films by Nanoimprint Lithography,*" Advanced Materials 19 (2007) 2919.

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H. W. Ro, H. Peng, K. Nihara, H.-J. Lee, E. K. Lin, A. Karim, D. W. Gidley, H. Jinnai, D. Y. Yoon, and C. L. Soles, *"Self–Sealing of Nanoporous Low Dielectric Constant Patterns Fabricated by Nanoimprint Lithography,"* Advanced Materials (2007).

H.-J. Lee, C. L. Soles, H. W. Ro, D. R. Hines, R. L. Jones, E. K. Lin, A. Karim, and W. Wu, *"Characterizing Nanoimprint Pattern Cross Section and Fidelity from X-ray Reflectivity,"* Proc. SPIE Int. Soc. Opt. Eng. 6151, 61510N (2006).

H.-J. Lee, C.L. Soles, D-W. Liu, B. J. Bauer, E. K. Lin, W.-l. Wu, *"Structural Characteristics of Methylsilsesquioxane Based Porous Low-k Thin Films Fabricated with Increasing Cross-linked Particle Porogen Loading,"* J. Appl. Phys. 100, 064104 (2006).

Interconnect Materials And Reliability Metrology

Technical Contacts:
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D. Josell

"Mechanical properties are key to integration."

Roey Shaviv
Novellus Systems Inc.

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the material properties that control the reliability of thin conducting and insulating films in interconnects under mechanical, thermal, and electrical stresses; these include basic tensile properties, elastic modulus by both static and dynamic means, residual stresses and strains, fatigue and fracture resistance, and thermomechanical response; and (2) to advance the ability to anticipate and meet interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of failure in nanoscale interconnect structures.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 11 thin-film layers now, and will reach 15 layers in the long term *(International Technology Roadmap for Semiconductors, 2007, Interconnect, Table INTC2b)*. These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low-κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the *Roadmap (2007 Edition), Interconnect, p. 39, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated.* The 2005 iNEMI *(International Electronics Manufacturing Initiative)* Research Priorities document reports a similar need. The top five research areas listed by iNEMI include *Materials & Reliability* and *Design*. Under *Design*, the top five research priorities include *Mechanical and Reliability Modeling, p. 16.* Appendix C of the document has a detailed section on *Reliability, Mechanical Analysis, and Simulation, p. 44*, which emphasizes the need for material characterization and reliability prediction. Key considerations in this paragraph and elsewhere in the document are effects of temperature and of cyclic loading and effects of size scaling. The iNEMI document specifically calls out the need to *predict and understand failures in MEMS devices, p. 39*. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets, and with the push into exotic nanoscale materials.

Because the films are formed by physical vapor deposition, electrodeposition, or spin-on deposition, their microstructures, and hence, their mechanical properties, are different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 0.1 to 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results. Industry needs test methods that are efficient and integrable in the fab environment. We see nanoindentation and high-amplitude a.c. measurements as candidates to become routine, or perhaps even on-line, methods. Compared to these, the microtensile test is more laborious, but it provides unambiguous results. We will continue to promote and offer the microtensile test as a reference method, while developing methods to extract needed material property information from the

more integrable methods such as nanoindentation and high-amplitude a.c. testing.

We held a second nanomaterials workshop entitled Materials Characterization for Nanoscale Reliability, 14–16 August 2007, to gauge customer interest in the available tools, and needs for new tools, for characterization of nanomaterials, which, of course, encompasses advanced interconnect structures at both current and foreseen size scales. Microelectronics manufacturers were represented, along with universities, national laboratories, and more general commercial interests. The referenced report, from the similarly-themed 2004 workshop, gives the details, but two key messages for this research project were the widespread adoption of nanoindentation for material characterization, and the serious consideration given to atomic-scale materials engineering. New messages from the 2007 workshop were the need for all materials analysis tools to provide nanometer resolution, so that, for example, chemical variation across interfaces could be examined, and the need for ongoing cooperation between measurement laboratories and industry.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand. We study individual

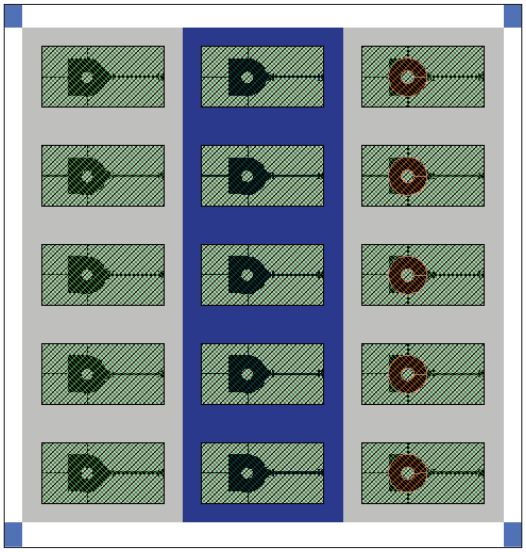

Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1).

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. thermomechanical fatigue and micro- and nanoscale characterization of industrially relevant materials. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the SEM. This system has now been used on specimens as small as 2 μm wide. The microtensile test provides complete and unambiguous mechanical design data.

Multiple wafer sections containing patterned specimen geometries of electrodeposited copper and other materials were received directly from our counterparts in industry during the past year. We have reported initial measurement results directly to the industrial collaborators, and received feedback about what they are interested in. For example, with an industrial collaborator, we are performing an extensive study of the

variability of the mechanical properties of electrodeposited copper, to determine the effect of deposition conditions, surface treatment, and other relevant variables.

DELIVERABLES:

- A joint industry-NIST publication on the effect of processing variables on the mechanical properties of thick electrodeposited copper. 4Q 2008.

Our measurements involving alternating current stressing of chip-level interconnects are being used to explore the relationships between electrical, thermal, and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in unconstrained lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including EBSD, SEM, and TEM has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This indicates at least the possibility that electrical tests may be exploited to produce information about the mechanical characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because of the experimental convenience of electrical stressing on specimens of a wide range of sizes, including very small and subsurface specimens. We have continued to improve our electrical measurements, and have begun SEM studies of the failure mechanisms in electrically-tested damascene copper interconnect lines.

DELIVERABLES:

- Conference presentation with short paper on studies of failure rates and mechanisms in electrically-tested damascene copper lines. 2Q 2008

For the relatively simple situation of a few-micrometer wide aluminum line on a silicon substrate, the ultimate strength value can be estimated from the a.c. test by extrapolating the results back to one loading cycle, and correcting for the residual stress present in the line-on-substrate specimen. However, physical differences between the a.c. and microtensile tests include: thermomechanical vs mechanical stressing; elevated and variable temperature in the a.c. test; residual stresses in the film on substrate vs none in the free-standing tensile specimen; substrate constraint causing biaxial loading as well as additional strengthening in the a.c. test; and cyclic loading vs monotonic strain to failure. By more realistic treatment of these differences, in measurements on specimens of different materials with different grain sizes and different line widths, we will quantify the uncertainty with which static mechanical properties can be deduced from the a.c. test. As a point of reference, the rule of thumb used to estimate ultimate tensile strength from nanoindentation hardness is only useful for detecting trends, and does not provide a generally applicable quantitative estimate of the tensile strength.

DELIVERABLES:

- Book chapter on Metrologies for Mechanical Response of Micro- and Nanoscale Systems 2Q 2008

Accomplishments

■ Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results. Microstructural characterization is critical for defining the applicability of test results for different materials and test techniques. Currently, we are improving our measurements for characterizing the microstructure of electrodeposited copper in order to better understand the influence of microstructure on reliability. Figure 2 shows the grain structure of a commercially produced copper film, as mapped out by EBSD. The colors represent local crystallographic orientation, according to the inset. Regions of constant color are metallographic grains. The long, straight, parallel boundaries are twin boundaries.

We found that we could make similar measurements on 100 nm wide copper lines in a damascene structure, Figure 3. The same wafer

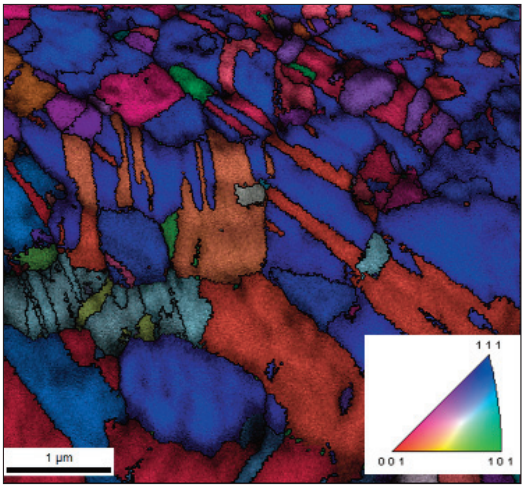

Figure 2. EBSD map of electrodeposited copper film specimen. The colors indicate the surface-normal crystallographic orientation of each pixel, according to the key, inset. Regions of constant color are crystallographic grains. The long, straight, parallel boundaries are twin boundaries.

contained large copper features; these had a grain diameter approximately 2.5 times larger than the grain length along the narrow lines. This result indicates that for the process sequence used on this wafer, the large grain size of the copper overburden did not propagate into the narrow lines.

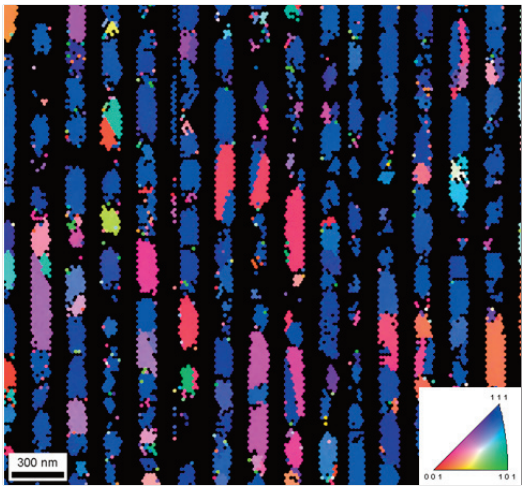

Figure 3. Electron backscatter diffraction map from a section of a 100 nm serpentine line structure. The black regions are the dielectric between the copper lines. The color represents the local crystallographic orientation normal to the plane of the page according to the inserted stereographic triangle. This mapping displays individual grains as colored regions. Note that the grain lengths average about 2.5 times the linewidth.

■ Based on input received at our 2004 workshop on Reliability Issues in Nanomaterials, an international round robin to assess interlaboratory reproducibility of measurements of hardness and elastic modulus by instrumented indentation, on thin film materials typical of those used in interconnect structures in microelectronic devices, has been conducted; a technical publication reporting the results has been published. A specimen film selected after consultation with a group of experts in the field, consisting of a copper film with a platinum passivation layer, was contributed by Sandia National Laboratory. Open participation was solicited by e-mail to over 100 laboratories. Fragments of the specimen wafer were distributed to approximately 30 laboratories around the world. The goal was to obtain results representative of the experience of a "typical customer" using a testing laboratory. Approximately 25 laboratories conducted tests and contributed reports. The results have been analyzed with assistance from the NIST Statistical Engineering Division. The scatter in modulus and hardness are much larger from laboratory to laboratory than within laboratories; Fig. 4 shows the hardness data. This result indicates that comparisons of instrumented indentation results from different laboratories should be treated with caution, and that further investigation is needed to identify the sources of the scatter.

■ We have been working to demonstrate the applicability of our small-scale mechanical testing techniques to materials recently introduced in the microelectronics industry, specifically copper, in

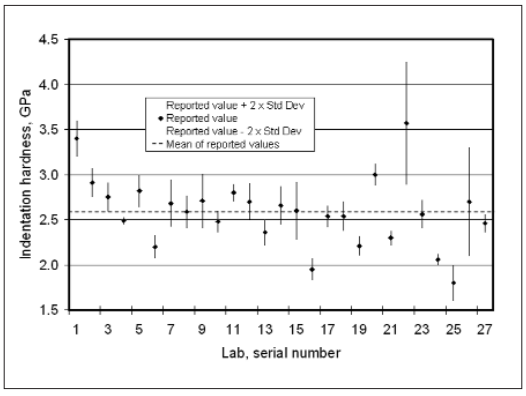

Figure 4. Reported results for indentation hardness of the round robin specimen material, a Cu film on a silicon substrate. The error bars at each data point span a total range of 4 times the standard deviation reported for multiple indentations. The average of the reported hardness values is 2.59 GPa.

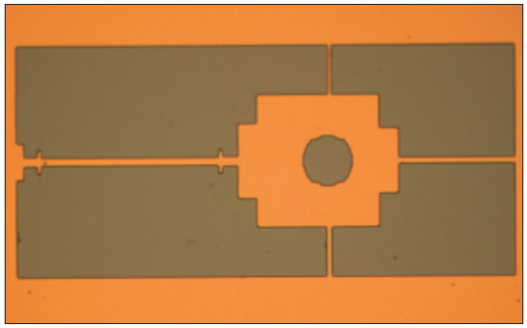

Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5.

We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 μm to 10 μm, increases the ductility from around 1 % or less to 5 % or more. These data were obtained in microtensile tests of a new variety of electrodeposited copper supplied by an industry collaborator. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 °C. Figure 6 shows recent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen mate-

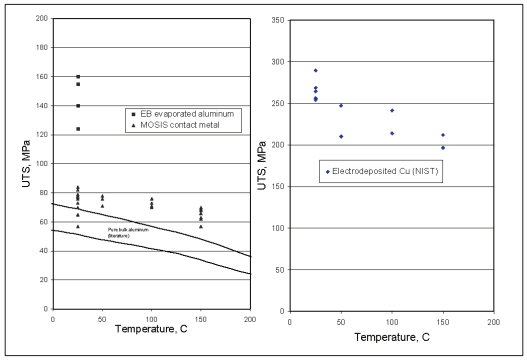

Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

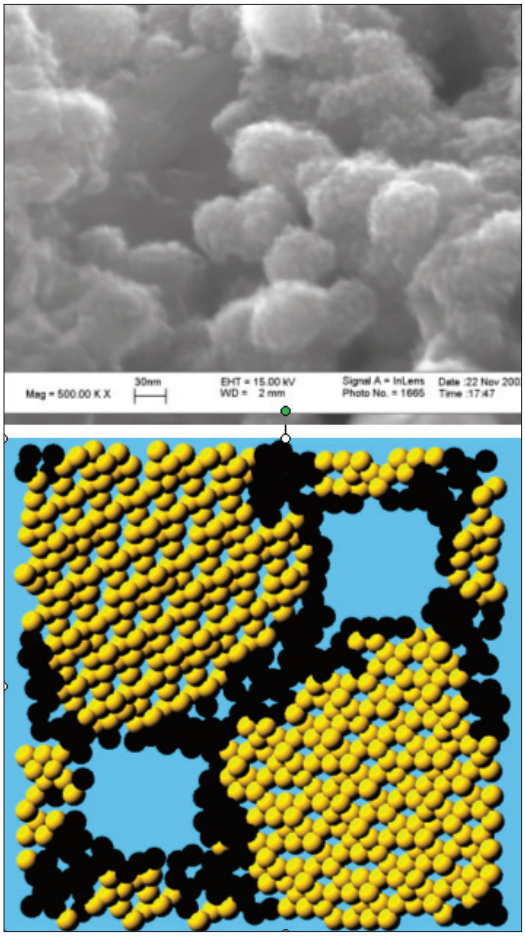

Figure 7. (a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper "balls" are 30 nm to 50 nm in diameter. (b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal facecentered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000 atom model simulates a specimen of indefinite size.

rials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

Figure 7a shows a high-resolution SEM image of the surface of an electrodeposited (ED) copper specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, mi-

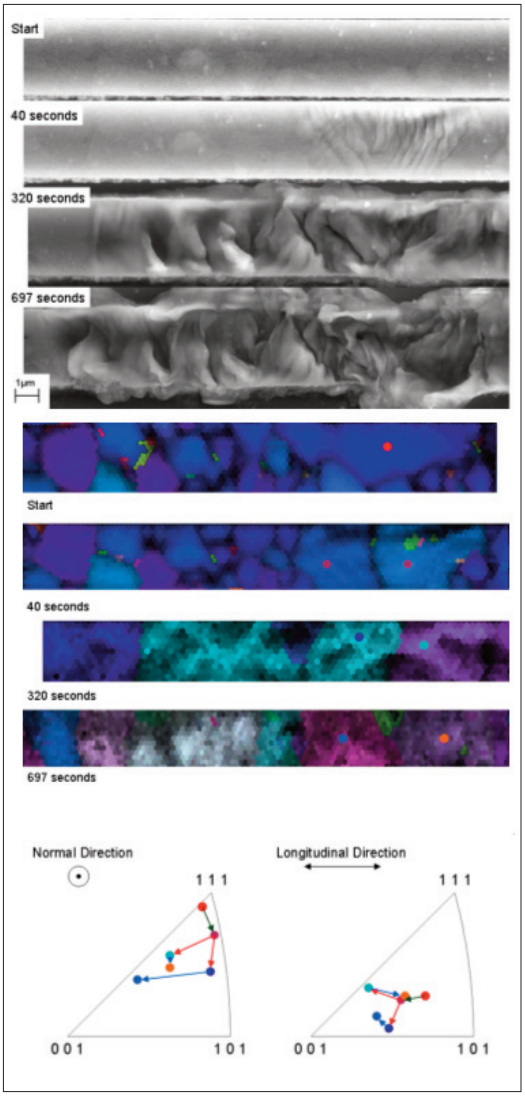

Figure 8. A.C. testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of A.C. cycling at about 12 MA/cm^2. Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

crostructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic model that simulates the mechanical behavior of this morphology, though at a smaller scale. The atoms shown as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible explanation for our measured value of the elastic constant of ED copper, which is lower than the bulk value.

■ Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. To understand the results, we have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 8).

Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

We are exploring the applicability of the a.c. test to commercial damascene copper structures. In these initial experiments we have plotted the data as lifetime to open circuit vs cyclic temperature range in Fig. 9. On this basis, we found a big difference between vias and lines, but no difference between oxide and low-κ dielectric structures. The preliminary conclusion from these tests is that the combined effects of thermal, electrical, and mechanical stresses need to be accounted for in designing reliable interconnect systems. The damage sequence shown in Fig. 8 is much different from electromigration. Results of our tests in damascene lines also indicate that the a.c. test excites thermal-mechanical failure mechanisms. We have designed and fabricated special specimens to isolate the direct effect of electrical current from the thermal-mechanical effects. Figure 10 shows this

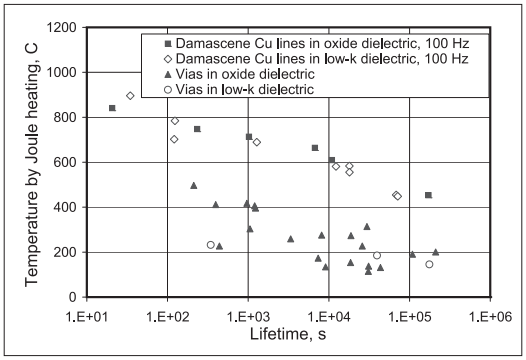

Figure 9. Comparison of lifetimes under high amplitude a.c. of Cu lines and Kelvin vias in damascene structures made with oxide and low-κ dielectric, plotted as cyclic temperature vs lifetime. When plotted in these coordinates, the vias fail at much lower temperatures than the lines in both structures, but the dielectric material does not affect the lifetimes.

"proximity effect" specimen. It consists of a heater, made of polysilicon or tungsten, and a test line; these are in thermal contact, but not in electrical contact. A.c. in the heater line applies thermal cycles to the test line. The purpose of the very long sections is to create a large constant-temperature zone free from end effects. Although the test line in this example is a conductor, this design also allows dielectrics to be thermo-mechanically cycled.

Collaborations

Roey Shaviv and Tom Mountsier, Novellus Inc.

Intel Corp., Hillsboro, OR, Sadasivan Shankar.

Freescale, Inc., AISL, Tempe, AZ, Vijay Sarihan and Aric Buchta.

University of New Mexico, Prof. Walter Gerstle.

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

Recent Publications

R. R. Keller, D. C. Hurley, D. T. Read, and P. Rice, "*Metrologies for Mechanical Response of Micro- and Nanoscale Systems*," in Micro and Nano Mechanical Testing of Materials and Devices, Springer-Verlag, edited by F. Yang F and J. C. M. Li, in press (2008).

R. H. Geiss and D. T. Read, "*Microstructure of 100 nm damascene copper overburden and lines*," in Instrumentation, Metrology, and Standards for Nanomanufacturing, edited by M. Postek and J. Allgair, Proc. of SPIE Vol. 6648 (on CD), 664808-1—664808-8, 2007.

R. H. Geiss and D. T. Read," *Defect behavior in aluminum interconnect lines deformed thermomechanically by cyclic joule heating*," Acta Materialia 56 (2), 274-281, 2008

R. R. Keller, N. Barbosa III,, R. H. Geiss, and D. T. Read, *"An Electrical Method for Measuring Fatigue and Tensile Properties of Thin Films on Substrates,"* Key Engineering Materials, Vols. 345-346 (2007) pp. 1115-1120 (online at http://www.scientific.net).

D. T. Read and V. K. Tewary, "*Multiscale model of near-spherical germanium quantum dots in silicon",* Nanotechnology 18 (10) 105402, 2007.

R. H. Geiss and D. T. Read, "*Need for Standardization of EBSD Measurements for Microstructural Characterization of Thin Film Structures"*, Proceedings of the 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, edited by D. Seiler et al., AIP Conference Proceedings 931, 168-172, 2007.

D. T. Read and R. H. Geiss, "*Study of Fatigue Behavior of 300 nm Damascene Interconnect using High Amplitude AC Tests,"* in Materials, Process, Integration and Reliability in Advanced Interconnects for Nicro- and Nanoelectronics, edited by Q. Lin, E. Ryan, W. Wu, and D. Yoon, Mat. Res. Soc. Symp. Proc. Vol. 990, 121-126, 2007.

D. T. Read and A. A. Volinsky, *"Thin Films for Microelectronics and Photonics: Physics, Mechanics, Characterization,*

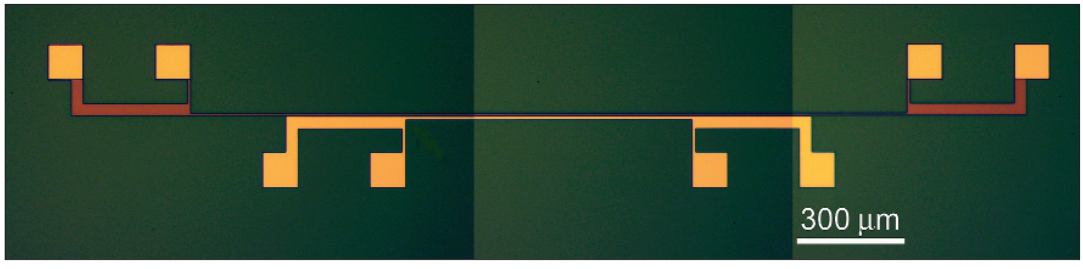

Figure 10. "Proximity effect" specimen for cyclic thermal-mechanical stressing. The upper, longer line is the heater; the lower line is the material to be examined.

and Reliability," in Micro- and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging, edited by E. Suhir, C.P. Wong, Y.C. Lee, Springer, New York, 2007.

N. Barbosa III, R. R. Keller, D. T. Read, R. H. Geiss, and R. P. Vinci, *"Comparison of Electrical and Microtensile Evaluation of Mechanical Properties of an Aluminum Film,"* Metallurgical Transactions A—Physical Metallurgy 38A (13), pp. 2160-2167, 2007.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Metallurgical and Materials Transactions A — Physical Metallurgy 38A (13), 2263-2272, 2007.

D. T. Read, R. R. Keller, N. Barbosa III, and R. H. Geiss, *"Nanoindentation Round Robin on Thin Film Copper on Silicon,"* Metallurgical and Materials Transactions A—Physical Metallurgy 38A (13), 2242-2248, 2007.

High Throughput Measurements of Thermoelectric Materials for Cooling Applications

Technical Contacts:
M. L. Green

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the material properties that control the reliability of thin conducting and insulating films in interconnects under mechanical, thermal, and electrical stresses; these include basic tensile properties, elastic modulus by both static and dynamic means, residual stresses and strains, fatigue and fracture resistance, and thermomechanical response; and (2) to advance the ability to anticipate and meet interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of failure in nanoscale interconnect structures.

Customer Needs

One of the most important impediments to further scaling of microelectronic devices is the removal of the enormous heat dissipated as a result of their operation. Passive heat removal is no longer an option. Device mounts and packages must contain active heat removal technology.

Thermoelectric materials, i.e., materials that can directly convert thermal energy into electrical energy and vice versa, are being developed for two energy applications: solid-state cooling for microelectronic devices, and waste heat recovery in engines for automotive, aerospace, and military applications. Improved cooling of microelectronic devices would result in greater operational efficiency and device reliability in the $43B U.S. semiconductor industry.

Technical Strategy

Currently, the energy conversion efficiency of well-established, bulk thermoelectric materials is too low for low-temperature (cooling) commercial device applications. There have been reports of higher conversion efficiencies in thin film materials, but the material properties affecting device conversion efficiency, i.e., Seebeck coefficient, S; electrical conductivity, σ; and thermal conductivity, κ are difficult to quantify or verify in thin film materials. Although there will be only limited applications for thin film thermoelectric cooling devices (for example, a ΔT of only 40°C across a 2 μm film represents a thermal gradient of 2×10^7 °C/m, which is not possible to sustain by known thermal management techniques), thin films, especially combinatorial thin films, are useful vehicles for screening of thermoelectric materials.

Our technical strategy is to develop standard reference materials (SRMs), measurement methods, and combinatorial materials methodologies to accelerate the commercial introduction of thermoelectric materials to the microelectronics market place. Thermoelectric SRMs and measurement methods will allow for inter-laboratory validation of data, leading to more rapid commercialization of thermoelectric materials for solid-state cooling applications. Measurement methods, especially for the case of thin film thermoelectric materials, are not standardized, and there are currently no methods to accurately and reproducibly (laboratory to laboratory) measure the material properties that determine thermoelectric conversion efficiency, i.e., Seebeck coefficient (S), resistivity (ρ), and thermal conductivity (κ). High-throughput combinatorial methodologies will be employed to generate comprehensive data sets (S, ρ, κ) for industrially-relevant bulk and thin film thermoelectric materials. We will also collaborate with several industrial, university and government laboratories to generate the appropriate data sets and standard reference materials.

DELIVERABLES:

- Start building cross plane thermal conductivity scanning tool (cross-plane measurements) for combinatorial thin films 1Q 2008
- Perform round-robin testing on candidate low temperature Seebeck SRM materials 2Q 2008
- Complete building combinatorial thermal conductivity scanning tool 3Q 2008
- Demonstrate applicability of thin film thermal conductivity scanning tool 4Q 2008

Accomplishments

Thermoelectric Measurements, Materials and Standards

In addition to equipping a new laboratory for thermoelectric property measurement, we accomplished two other goals: the completion of a round-robin survey of two potential bulk standard reference materials (SRM's) for measurement of the low-temperature Seebeck coefficient, and development of a scanning tool for Seebeck coefficient and resistivity measurements on combinatorial thin film libraries of thermoelectric materials.

The Seebeck coefficient round robin data were analyzed using a parametric model to generate common fitted curves for data generated from various laboratories (laboratories were at AIST (Japan), Michigan State University, Hi-Z Technology Corp., Quantum Design Corp., Clemson University, Naval Systems Weapons Center, U. Maryland, Oak Ridge National Labs, University of South Florida, GM Corp., and University of Michigan) using different measurement techniques and samples from the same batch. Of the two candidate materials, Bi_2Te_3 and Constantan (a copper-nickel alloy), we found that the coefficient of variance for Bi_2Te_3 was smaller across the entire temperature range compared to that of Constantan. Further, Bi_2Te_3 has a larger Seebeck coefficient than Constantan. Therefore, we have chosen Bi_2Te_3 as our prototype SRM, and production of Bi_2Te_3 low temperature Seebeck coefficient SRMs is proceeding according to schedule. The completion of this SRM will enable accurate instrument calibration, and therefore meaningful interlaboratory comparison of data.

Next, an automated Seebeck coefficient screening tool has been successfully designed and constructed. The tool consists of a probe and an automated translation stage to move the probe in the x, y, and z directions. This tool takes as little as 20 seconds to measure both electrical conductivity and Seebeck coefficient at each sample point; thus, over 1000 sample points can be measured within 6 hours. The tool's measurement capability has been demonstrated for a ternary composition library film of the thermoelectric system $(Ca\text{-}Sr\text{-}La)_3Co_4O_9$. The power factor ($S^2/\rho$) is seen to peak between the Sr-rich and La-rich regions.

Professional Participation

- Outside NIST activities:
  - Thermoelectric Program Reviewer: Reviewer for DOE Freedom Car Program with regard to Solid State Energy Conversion
- Meeting Co-organizer
  - Thermoelectric Materials and Applications, MS&T06, Oct 15-19, 2006, Duke Energy Center, Cincinnati, OH, co-organizer (W. Wong-Ng)
- Thermoelectric Materials: Science, Technology and applications, MS&T08, Oct. 5-9, 2008, Pittsburgh, PA, co-organizer (W. Wong-Ng)
- Panel Discussion, 'Future Needs for Thermoelectric Metrology', International Conference on Thermoelectrics (ICT2008), Corvallis, Oregon, Aug. 3-7, 2008 (W. Wong-Ng)
- DOE SBIR proposal reviewer on thermoelectrics (2007, 2008) (W. Wong-Ng)

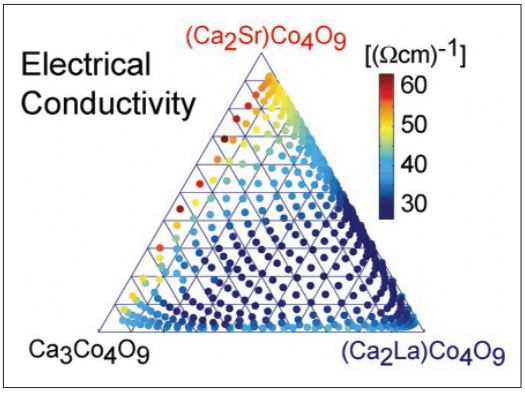

Figure 1. Electrical resistivity of a $(Ca,Sr,La)_3Co_4O_9$ film

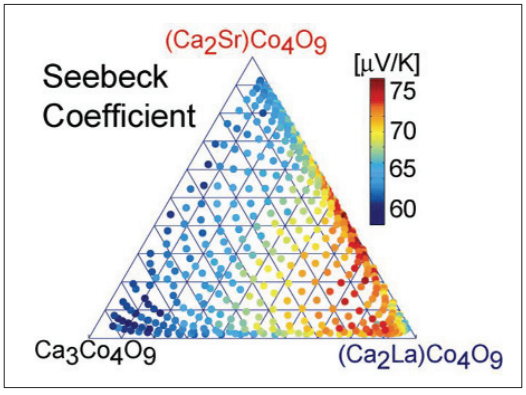

Figure 2. Seebeck coefficient of a $(Ca,Sr,La)_3Co_4O_9$ film

Collaborations

Low temperature Seebeck coeffiecient round robin study with eleven labs mentioned above.

High temperature Seebeck coefficient effort started with GM corporation.

Recent Talks/Publications

Publications

N. Lowhorn, W. Wong-Ng, W. Zhang, J. Lu, M. Otani, M. Green , T.N. Tranh, et al., *"Round-robin measurements of two candidate materials for a Seebeck Coefficient Standard Reference Material"*, submitted to APL (2008).

M. Beekman, J.A. Kaduk,J. Gryko,W. Wong-Ng, A. Shapiro, and G.S. Nolas, *"Synthesis and transport properties of framework-substituted $Cs_8Na_{16}Cu_5Ge_{131}$"*, J. Alloys and Compounds, in press (2007).

M. Otani, N.D. Lowhorn, P.K. Schenck, W. Wong-Ng, and M. Green, *"A High-throughput Thermoelectric Screening Tool for Rapid Construction of Thermoelectric Phase Diagrams,"* Appl. Phys. Lett. 91, 132102 (2007)

W. Wong-Ng, Y.F. Hu, M.D. Vaudin, B. He, M. Otani, N.D. Lowhorn, and Q. Li, *"Texture \Analysis of a $Ca_3Co_4O_9$ Thermoelectric Film on Si (100) Substrate,"* J. Appl. Phys, 102(3) 33520 (2007).

M. Otani, K. Itaka, W. Wong-Ng, P.K. Schenck, and H. Koinuma, *"Development of high-throughput thermoelectric tool for combinatorial thin film libraries,"* Appl. Surface Science, 254 765-767 (2007).

M. Beekman, W. Wong-Ng,J.A. Kaduk, A. Shapiro, and G.S. Nolas, *"Synthesis and single-Crystal X-ray diffraction studies of new framework substituted type II clathrates, $Cs_8Na_{16}AgxGe_{136}$-x (x < 7)"*, J. Solid State Chem. 180 1076 (2007).

N. Lowhorn, W. Wong-Ng, W. Zhang, J. Lu, M. Otani, M. Green , T.N. Tranh, et al., *"Round-Robin Studies of Two Potential Seebeck Coefficient Standard Reference Materials,"* in press, IEEE Transaction (2007).

Matt Beekman, James A. Kaduk, Q. Huang, Winnie Wong-Ng, Z. Yang, Dongli Wang, and George S. Nolas, *"Synthesis and Structure of a New Zeolite-like Framework Phase in the Na-Ge System: $Na_{1-x}Ge_{3+z}$,"* Chem. Commun. 837 (2007).

Talks

High-throughput Seebeck Coefficient Screening System for thermoelectric materials Combinatorial Library Films, NIST Technology Transfer Showcase (TEDCO), April 8, 2008, NIST, Gaithersburg, MD (M. Otani).

Thermoelectric Properties in the Ce-Co-Sn System: A Combinatorial Approach Using Sputtering American Chemical Society (ACS) Meeting Poster Session, New Orleans, LA (Spring 2008)(E. Thomas).

Overview of thermoelectric research at the Ceramics Division of NIST, Columbia University, March 28, 2008, New York, New York (W. Wong-Ng).

High-Throughput Seebeck Coefficient Screening System for Thermoelectric Materials Combinatorial Library Films, Thermoelectric Symposium, MRS, Nov. Boston, MA 2007 (M. Otani).

Development of a bulk, low-temperature Seebeck coefficient Standard Reference Material, MRS, Boston, MA, Nov. 29, 2007 (N. Lowhorn).

A Combinatorial Approach to the Study of the Phase Diagram and Thermoelectric Properties in the Ce-Co-Sn System, Materials Research Society (MRS) Meeting Poster Session, Boston, MA (Fall 2007) (E. Thomas).

High-Throughput Screening System for Thermoelectric Material Exploration Based on Composition-Spread Approach, Combinatorial symposium, MRS, November, 2007 (M. Otani).

High-throughput screening system for thermoelectric material exploration based on combinatorial pulsed laser deposition, DTEC, Vail, Aug. 2007 (M. Otani).

Overview of thermoelectric research at NIST, Direct Energy Conversion (DTEC) Workshop, Vail, CO, Aug. 21-23, 2007 (W. Wong-Ng).

Crystal Chemistry and Crystallography of the Type-II Clathrate, Cs8Na16Ge136-xAgx, and a Novel Phase, Na1-xGe3+z, American Crystallographic Association annual meeting, Salt Lake City, Utah, July 22-26, 2007 (W. Wong-Ng).

High-Throughput Screening System for Thermoelectric Material Exploration Based on Composition-Spread Approach, Brookhaven National laboratory, Brookhaven, NY, June 2007 (M. Otani).

High-Throughput Combinatorial Thermoelectrics Research Using Sputtering, Brookhaven National Laboratory, Condensed Matter Physics and Materials Science Division, Upton, NY (June 28, 2007) (E. Thomas).

Overview of the coated conductor and thermoelectric research at the Ceramics Division of NIST, Korean Institute of Science

and Technology (KIST), Seoul, Korea, June 12, 2007 (W. Wong-Ng).

Overview of the thermoelectric research at the Ceramics Division of NIST, Seoul National University, Seoul, Korea, June 11, 2007 (W. Wong-Ng).

Development of a Low Temperature Seebeck Coefficient Standard Reference Material, International Conference of Thermoelectrics (ICT2007), June 7, 2007, Jeju Island, Korea (W. Wong-Ng).

Development of a Seebeck Coefficient Standard Reference Material, ICT2007, Jeju Island, Korea, June 3-8, 2007 (W. Wong-Ng).

Round-Robin Measurement Survey for Seebeck Coefficient Standard Reference Material, APS, Denver, CO, March 7, 2007 (N. Lowhorn).

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High-Throughput Screening System for Thermoelectric Material Exploration Based on Composition-Spread Approach, AIST, Tsukuba, Japan, Feb. 2007 (M. Otani).

High-throughput screening system for thermoelectric material exploration based on combinatorial pulsed laser deposition, US-Japan Combinatoiral Workshop, San Juan, Puerto Rico,Dec. 2006 (M. Otani).

Texture Analysis of Ca3Co4O9 thermoelectric films, MS&T06, Cincinnati, OH, October 15, 2006 (W. Wong-Ng).

Combinatorial synthesis and characterization of Ca3Co4O9-based composition-spread thin films, MS&T, Cincinnati, OH, October 15, 2006 (M. Otani).

Development of High Throughput Characterization Tool for Combinatorial Thermoelectric Materials Research, NCMC-10, NIST, Gaithersburg, MD, Oct. 2006 (M. Otani).

Development of a Standard Reference Material for Seebeck Coefficient DTEC, Coronado, CA, Sept 1, 2006 (N. Lowhorn).

Effect of Rare-Earth Doping on the Thermoelectric and Electrical Transport Properties of the Transition Metal Pentatelluride HfTe5, MST, Cincinnati, OH, Oct 15, 2006 (N. Lowhorn).

Round-Robin Measurement Survey for Seebeck Coefficient Standard Reference Material, MST, Cincinnati, OH, Oct 16, 2006 (N. Lowhorn).

Development of High Throughput Characterization Tool for Combinatorial Thermoelectric Materials Research, DTEC, Sept. 1, 2006, Coronado, CA (M. Otani).

Pb-Free Surface Finishes for Electronic Components: Sn Whisker Growth

Goals

The microelectronic industry is faced with an extreme reliability issue due to Sn whisker induced failures. This project is providing data and materials measurements to improve the reliability of solder interconnects degraded by the switch to Pb-free technology. In particular the state of compressive stress and the localized creep response (whisker growth) of Sn-based, Pb-free electrodeposits are being measured. Industry will use these measurement methods and data to modify processing conditions to mitigate the formation of Sn whiskers.

Customer Needs

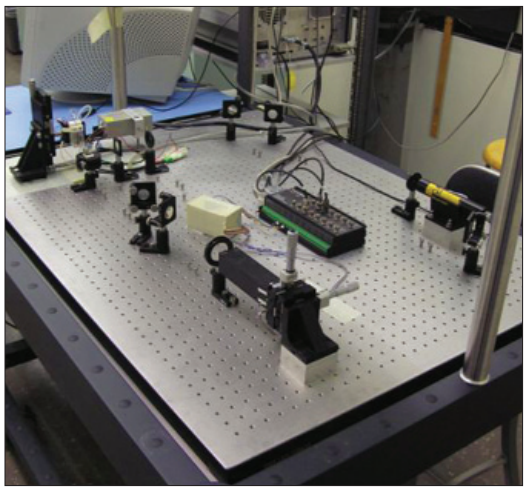
Sn is widely used as a coating in the electronics industry because it provides excellent solderability, ductility, electrical conductivity, and corrosion resistance. However, Sn whiskers have been observed to grow spontaneously from Sn electrodeposits and are known to cause short circuits in fine pitched pre-tinned electrical components. In the 1960s, the addition of a few percent of Pb to Sn was found to greatly reduce the tendency to form whiskers. However, recent demand for Pb-free surface finishes for ecological reasons has renewed interest in understanding whisker growth and developing whisker mitigation strategies. It is widely recognized that compressive stress is a necessary, but insufficient, condition for whisker growth.

The U.S. microelectronics industry needs a method to measure stress in the Sn electrodeposited surface finishes of electronic components to predict the propensity of whisker growth before these components are assembled on circuit boards to prevent the loss of both revenue and life from Sn whisker failures. The 2007 International Electronics Manufacturing Initiative (iNEMI), and 2006–2007 IPC technology roadmaps clearly articulate the need for Sn whisker research. In order to prevent or mitigate whisker growth, workshops sponsored by industry and academia have reached a consensus list of concerns: understand the influence of electroplating conditions, grain structure/shape/orientation, compressive stress in the electrodeposits, intermetallic compound (IMC) formation at the SnCu interface, diffusion of Sn, and thermal cycling effects on electroplated components.

Mitigation strategies being investigated include the elimination of columnar grain shape and elimination of intermetallic reaction with the substrate. Focused ion beam (FIB) milling reveals the internal microstructure so that changes in grain structure can be directly correlated to whisker growth. Also models of stress accumulation and relaxation are used to interpret the stress measurements and describe the whisker/hillock growth.

Technical Strategy

Our work on Pb-free electrodeposits is focused on grain structure modification and the measurement of stress. Two methods are currently used for electrodeposited Sn surface finishes: (1) X-ray measurement. (2) Optical stress measurement during and after electrodeposition by wafer curvature technique. Although it is easy to obtain stress values from these techniques, understanding the source of measurement errors is undeveloped. Errors can be a significant fraction of the measured quantity. Electroplated Sn has a preferred crystallographic orientation that can vary depending on plating conditions. Sn is a low melting metal (0.6 TM at RT), with a low yield strength (≈30 MPa) that creeps at room temperature. These factors as well as geometrical, diffraction, and optical subtleties complicate the two measurement methods. The techniques also have disparate temporal and spatial resolution that measure different aspects of the stress.



Technical Contacts:
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K.-W. Moon
G. R. Stafford
M. E. Williams

"NIST's involvement in the iNEMI Tin Whisker project work has been a great asset to the team. Their diligence in generating and sharing data has been instrumental in making progress in this field. They are a great technical asset and are always willing to help design tests and generate data when needed".

Dr. Richard D. Parker
Lead Technologist, Delphi Electronics & Safety
Advanced Assembly Technologies
Kokomo, IN 46904-9005

DELIVERABLES:

- Host a NIST workshop "Methods for measuring residual stress in Sn and Sn alloy electrodeposits". 3Q 2008
- Develop technique to grow whiskers on demand with the application of external force. 3Q 2008
- Perform simultaneous wafer curvature and x-ray diffraction stress measurements. 4Q 2008
- Complete Manuscript "Recommended Practice for measuring residual stress in Sn electrodeposits with the x-ray sin2 method" 1Q 2009

Accomplishments

■ Results show that the columnar grain structure of Sn electrodeposits can be modified to an equiaxed structure by pulse plating combined with the addition of Bi. Pulsed deposition is used to selectively turn on and off the Sn deposition reaction. Since the standard potential for Bi is more positive than Sn, during the off cycle a displacement reaction between metallic Sn on the electrode surface and Bi^{3+} in solution selectively dissolves Sn and deposits Bi, effectively terminating the growth from the previous cycle and forcing the Sn to nucleate a new grain on the Bi-enriched surface. The grain size is tunable by varying the pulsing conditions, and an equiaxed structure can be obtained with as little as 3 at.% Bi. This surface enrichment of Bi by potential modulation is similar to that which occurs naturally in Sn-Pb deposition, and provides an avenue for breaking up the columnar grain structure inherent to pure Sn, thus providing an additional diffusion path for Sn that may prevent whisker growth.

■ Compressive stresses are the driving force behind whisker formation. Two sources are evident. Intrinsic electrodeposition stresses are influenced by many factors including current density, alloying additions, plating bath additives and deposit thickness. Stress arising from room-temperature formation of the Cu_6Sn_5 intermetallic compound (IMC) at the interface between the electroplated Sn and the Cu substrate provide additional the driving force for the growth of Sn whiskers.

■ To separate the effects of intrinsic plating stress from the stress generated by IMC growth, Sn and Sn-Cu alloys were plated on Tungsten (W) substrates that do not react with Sn to form IMC. Whiskers and hillocks formed due to the intrinsic plating stress but with reduced density and/or length. The claim by various authors that IMC formation is the *unique* cause of whisker growth is thus disproved.

■ Stress in the Sn and Sn alloys was measured by electrodepositing on cantilever beams made of either Cu or W. The deflection of the cantilever beam as a function of time was monitored. To complement the stress measurements obtained by the cantilever beam deflection measurements, residual stress in electroplated Sn deposits was measured using the $\sin^2\psi$ x-ray diffraction method. The preferred orientation of the deposits and the low stress levels (≈ 10 MPa) presented many challenges for this technique. A detailed analysis of errors in the measurement method as it applies to Sn has been performed and a recommended practice guide is being written. Also a major summary of whisker/hillock growth to intrinsic electrodeposition stress and IMC generated stress has been published (Boettinger, et al., 2005)

■ In June 2007, the two iNEMI technology working groups, Sn whisker Modeling and Accelerated Sn Whisker Test, combined to form the Sn Whisker Group. NIST remains an active participant in the Sn Whisker Group with bi-weekly teleconferences and round robin experiments (members include Alcatel-Lucent, Cisco Systems, Cookson, Delphi Delco, Freescale, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics).

Collaborations

In an effort to develop a standard X-ray diffraction method to measure stress in Sn electrodeposits we are conducting round robin experiments with Dr. Robert Hilty of Tyco Electronics located in Middletown, PA.

NIST provided advice and expertise to Univ. of Maryland group for the production of fast growing whisker samples of Sn-Cu electrodeposits on Zn substrates for tests of acrylic conformal coatings. These samples can reduce the evaluation time of the coatings used by industry as a whisker mitigation method to prevent whisker related failures of electronic devices.

Publications

E. Sandnes, M.E. Williams, M.D. Vaudin and G.R. Stafford, *"Equi-Axed Grain Formation in Electrodeposited Sn-Bi"*, Journal of Electronic Materials, v 37, n 4, April, 2008, p 490-497.

K.-W. Moon, U.R. Kattner, C.A. Handwerker, *"The Effect of Bi Contamination on the Solidification Behavior of Sn-Pb Solders",* Journal of Electronic Materials, Vol. 36, No. 6, pp.676-681, June 2007.

E. Sandnes, M.E. Williams, U. Bertocci, M.D. Vaudin and G.R. Stafford, *"Electrodeposition of Bismuth from Nitric Acid Electrolyte",* Electrochimica Acta, Vol. 52, Issue 21, pp. 6221-6228, June 2007.

K.-W. Moon, U.R. Kattner, C. A. Handwerker (Purdue Univ.), *"Chapter 2: Fundamental Properties of Pb-Free Solder Alloys",* Springer Press, in Pb-Free Soldering, ed J.S. Bath, ISBN978-0-387-32466-1, 2007.

G. R. Stafford, C. Beauchamp, U. Bertocci, E. Sandnes, and W. J. Boettinger, *"Sn Whisker Formation: Stress Generation at the Sn-Cu Interface,"* Spring MRS Meeting, Symposium E: Pb-Free and RoHS-Compliant Materials and Processes for Microelectronics, San Francisco, California, April 9-13, 2007.

M.E. Williams, K-W Moon, W. J. Boettinger, D. Josell, and A. Deal (Lehigh University), *"Hillock and Whisker Growth on Sn and SnCu Electrodeposits on a Substrate Not Forming Interfacial Intermetallic Compounds",* Journal of Electronic Materials, Vol. 36, No. 3, pp.214-219, Feb.2007.

W. J. Boettinger, U. R. Katttner, K.-W. Moon and J. H. Perepezko (U. of Wisconsin, Madison), *"Recommended Practice Guide for Differential Thermal Analysis (DTA) and Heat Flux Differential Thermal Analysis (DSC) Measurements of Alloy Melting and Freezing,"* NIST Special Publication Series 960-15, Feb. 2007.

G. R. Stafford, M. E. Williams, C. E. Johnson, K.-W. Moon, U. Bertocci, O. Kongstein, and W. J. Boettinger, *"Whisker Formation in Pb-free Surface Finishes,"* ECS Transactions, v 1, n 13, Green Electrodeposition, 2006, pp 71-85.

M. E. Williams (NIST), V. Schroeder (HP), P. Bush (SUNY Buffalo), N. Vo (Freescale), H. L. Reynolds (Sun Microsystems), *"Tin Whisker Test Method Development,"* IEEE-Transactions on Electronics Packaging Manufacturing, V29, 4, 2006, pp 231-238.

Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Copper is now predominantly the conductor of choice over aluminum because of its intrinsic higher conductivity. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material was sufficient, but now more exotic materials such as transition metal oxides, silicates, and aluminates are being introduced. Additionally, the gate conductor, traditionally polysilicon, is being replaced by metal or metal silicide to eliminate the polysilicon depletion effect. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Water and other contaminants at extremely low levels in process gases present serious manufacturing difficulties. Accurate calibration of water vapor and other contaminants at extremely low vapor pressures is required.

Atomic layer deposition processes are increasingly being used for high quality thin dielectrics and conductors. Techniques for understanding the deposition mechanisms and characterizing the compounds that are formed are being developed. Theoretical studies elucidating the thermodynamics and quantum mechanical properties of these compounds are being conducted.

Low Concentration of Humidity Standards

Technical Contacts:
J. T. Hodges
D. Ripple
K. Bertness

"The LFPG is the 'Gold' standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard."

Suhas Ketkar,
Air Products and Chemicals

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control — functions that are relevant to minimizing wafer misprocessing.

Customer Needs

Measurement needs and technical challenges for airborne molecular contamination (AMC) in semiconductor wafer processing spanning the next 15 years are given in the 2007International Technology Roadmap for Semiconductors (ITRS) http://public.itrs.net/. A key measure of technological progress defined in the ITRS is yield enhancement (YE) which is the process of improving baseline yield for a given technology generation from R&D yield level to mature yield. AMC affects YE and constitutes a major impediment to wafer environment contamination control particularly for 300 mm wafer manufacturing processes. VLSI Research Inc. estimates that "a 1 % yield increase equates to $1M per day additional profits for a modern 300 mm fabrication line," The Chip Insider®. The ITRS also states "The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation ... to measure AMC at the part per trillion level … low cost, routine monitoring may be required as devices approach molecular dimensions." Target impurity levels relevant to wafer environmental contamination control for a number of AMC including H_2O, THC, CO_2 and other AMCs in various bulk gases are given in ITRS Tables YE9a and b, and quantify the measurement needs in a variety of wafer production processes. Of these impurities, water vapor is one of the most ubiquitous and difficult to eliminate. Similarly, the Semiconductor Equipment Manufacturers International (SEMI) has standards describing the production and delivery and value assignment of ultra-high purity gases for semiconductor manufacturing http://downloads.semi.org/PUBS/SEMIPUBS.NSF/webstandardsgases. These standards illustrate the stringent requirements for gas purity measurements in semiconductor processes. We also note a new emphasis (beginning with the 2004 ITRS) on epitaxial processes that use gases as source materials, including SiGe and III-V semiconductor requirements for power amplifiers and extension of physical models to III-V semiconductors.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather, they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG) (see Fig. 1 and Fig. 2), serves as the project cornerstone and is capable of delivering 3 nmol to 3 mmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize water vapor measurement and generation

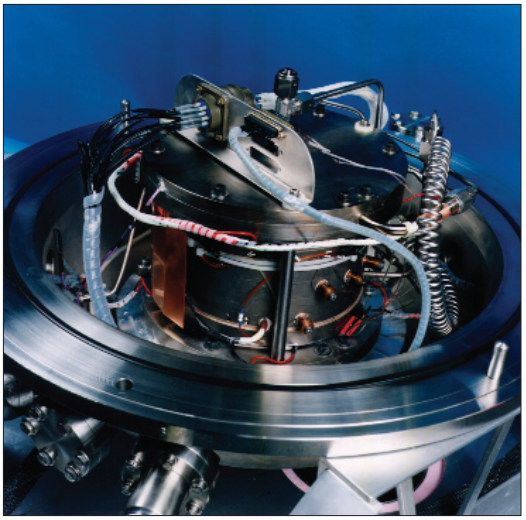

Figure 1. NIST Low Frost-Point (humidity) Generator.

systems at the research and development stage as well as commercial devices.

1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We have constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards. Experience with the system has revealed several limitations of traditional implementations, including deviations of the output from the equation generally used to predict the temperature dependence of the permeation rate.

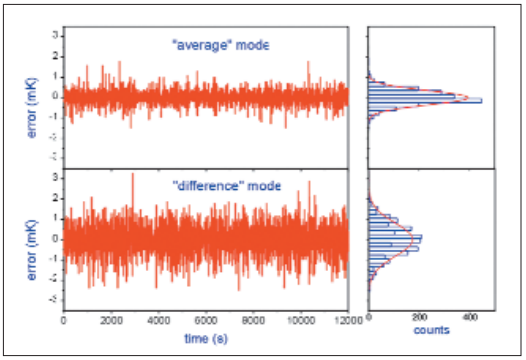

Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

DELIVERABLES:

- Commission calibration service. 2Q 2008

2. In its standard mode of operation, the LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N_2 based on the minimum achievable temperature of the saturator. We now regularly generate pmol mol^{-1}-levels of humidity using dry-gas dilution of the water vapor/gas mixtures produced by the LFPG output stream. We have validated the technique and established the uncertainties with a variety of self-consistency tests. Development of gas-handling manifolds with ultra-low adsorption/desorption of water will be a key focus of our work in the next year.

DELIVERABLES:

- Investigate attainable dry-drown rates using coated tubes for gas manifolds. 2Q 2008
- Publish results on coated tubes. 3Q 2008

3. As part of the NIST mission to provide reliable measurement standards, we compare our standards with those of other nations. These international comparisons are conducted under strict guidelines, with all results blind to the participants until the completion of the comparison.

DELIVERABLES:

- Participate in an international comparison of humidity generators for the concentration range (10 to 20000) μmol mol^{-1}. 2Q 2008

4. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct vibrational absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line intensities. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10^{10} molecules cm^{-3}. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much

smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method (Fig. 3). CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequency-stabilized cavity ring-down spectroscopy (FS-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. Taking advantage of the high spectral resolution afforded by FS-CRDS, various line shape effects such as speed-dependent pressure-broadening and collisional narrowing of these transition line shapes by various media can now be quantified.

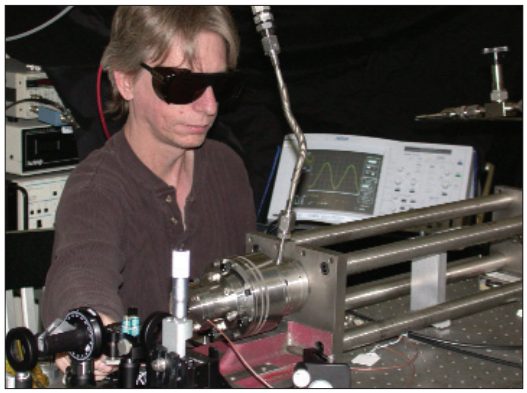

Figure 3. Frequency-stabilized CRDS system.

Using the existing FS-CRDS apparatus and a portable fiber-optics-based FS-CRDS system, we are making independent measurements of H_2O transition line shapes and line intensities in the vicinity of 1380 nm. We are also comparing our FS-CRDS measurements of water vapor concentration with those produced by a commercial CRDS-based hygrometer. We will use transfer standards for humidity generation and measurement as well direct measurement of humidified gas samples delivered by the thermodynamic-based LFPG.

DELIVERABLES:

- Perform line intensity measurements for H2O transitions by direct comparison with LFPG using portable FS-CRDS apparatus. 3Q 2008
- Perform direct comparison of FS-CRDS system with commercial CRDS system 4Q 2008

5. Moisture contamination is a serious problem in phosphine, arsine, silane, ammonia, and similar gases used in the epitaxial growth of high-purity semiconductor layers. Semiconductor device manufacturers have expressed frustration with the irreproducibility of source material purity from vendor lot to vendor lot. The critical concentrations of the impurities are not well known; however, it is believed that >10 nmol/mol oxygen or water in most process gases is undesirable. Optical methods for measuring the moisture impurity concentrations combine high sensitivity and straight-forward traceability through the LFPG absorption line strength measurements. In collaboration with researchers in the NIST Chemical Science and Technology Laboratory, researchers in the NIST Electronics and Electrical Engineering Laboratory have developed a CRDS system linked with a semiconductor crystal growth system to measure H_2O at very low concentrations in semiconductor source gases and to correlate the process gas impurities with crystal properties. The system is being used to measure the lineshape, absorption coefficients, and frequency of optical transitions for water, phosphine, and ammonia in the vicinity of 935 nm and 1380 nm. This information is critical to facilitate the use of high-sensitivity spectroscopy techniques in these gases. The laboratory is equipped to allow safe handling of toxic gases such as phosphine and arsine, enabling collaborative experiments with industry on direct measurements of moisture in those gases. The CRDS capability should ultimately lead to improvements in semiconductor source gas purity, which will allow crystal growers to choose less expensive growth conditions without sacrificing optical emission efficiency and yield in LEDs, semiconductor lasers, and photodetectors.

DELIVERABLES:

- Modify CRDS system for parallel tests with commercial instrumentation and conduct joint experiments on H_2O in phosphine. 3Q 2005

- Measure phosphine absorption lines in vicinity of H_2O transition line at 943.082 nm and compare to previous H_2O lines explored for overlap with phosphine. If new line offers superior sensitivity, measure pressure broadening coefficients for H_2O in phosphine. 4Q 2005

Accomplishments

■ We have constructed a permeation tube calibration facility (see Fig. 4). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and either a high-sensitivity quartz crystal microbalance (QCM) or commercial CRDS hygrometer. The water-containing permeation tubes to be calibrated are placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a precisely controlled stream of purified N_2. The diluent gas flow rate is adjusted so that the water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. As seen in Fig. 5, the calibrations derived from this system are repeatable to approximately 1 %, which is significantly superior to traditional gravimetric methods. We have performed multiple replicate runs with this system, and have used the resulting data to complete the uncertainty analysis of this system.

■ A new strategy for pmol mol^{-1} (ppt)-level humidity generation has been successfully implemented. The approach, shown in Fig. 6, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above. At mole fractions below 10^{-9}, the uncertainty in water vapor mole fraction is dominated by water vapor background produced by adsorption/desorption of water on internal plumbing surfaces and by water vapor remaining in the diluent after purification. We performed three sets of measurements to validate the method. First, the same nominal output concentration was produced while varying both the water vapor concentration produced by the Low Frost-Point Generator and the level of flow dilution. Deviations from a constant concentration were measured. Second, the calculated water vapor mole fraction of the diluted generator output was compared against the reading of a commercial hygrometer based on cavity ring-down spectroscopy. Third, we measured the water remaining in the diluent gas after purification at various flowrates both with and with-

Figure 4. New PTG calibration apparatus.

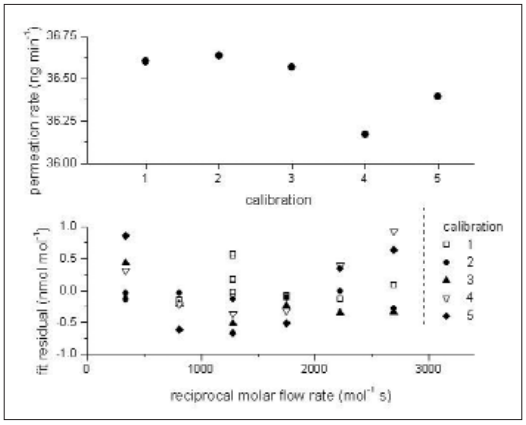

Figure 5. Calibration repeatability (top) and deviations from the fi tting function (bottom) of a water-vapor permeation tube in the NIST Permeation Tube Calibration Facility.

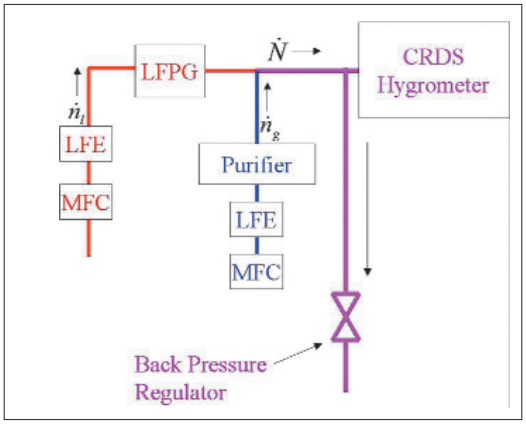

Figure 6. Dilution system for extending the LFPG operating range to pmol mol^{-1} levels.

out an additional cryotrap. An approximate water background of 0.3 × 10^{-9} was inferred from the data, and the results were consistent within the combined uncertainty of the LFPG output and the water background.

■ The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may affect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results, shown in Fig. 7, indicate that the background contribution to H_2O from system components downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H_2O mole fraction are less than 0.1

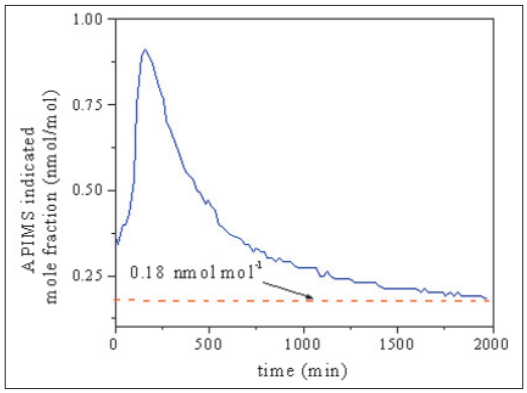

Figure 7. APIMS measurement of LFPG background H_2O concentration showing decay to steady state level.

nmol/mol.

■ We recently participated in two international comparisons of humidity generation standards. Measurements of test gas produced by the LFPG were performed at frost-point temperatures between -50 ºC and -10 ºC and were included in a key comparison of humidity generators that was organized by Working Group 6 of the Consultative Committee on Thermometry (CCT), part of the Bureau International des Poids et Mesures (BIPM). We are also participating in an exploratory study of trace humidity generators over the humidity concentration range from 10 to 20000 parts per billion of water vapor in nitrogen. Four national metrology institutes are participating, including NIST, National Physical Laboratory (NPL,UK), Physikalisch-Technische Bundesanstalt (PTB, Germany), and National Metrology Institute of Japan (NMIJ, Japan). NIST and NPL are acting as pilot laboratories in this study.

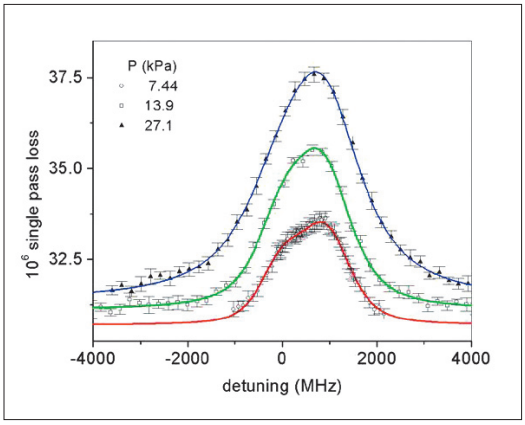

Figure 8. High-resolution FSSM-CRDS spectrum of a pair of pressure-broadened water vapor absorption transitions. Symbols are experimental points, and lines are Voigt fits to the measured profiles.

■ We have successfully developed an FS-CRDS system with automated spectral scanning capability to measure the absorption coefficient of trace quantities of water vapor. In FY 2005 the FS-CRDS method was used to probe H_2O absorption transitions in the 935 nm spectral region, and a spectral resolution of 50 kHz and reproducibility better than 0.25 % were demonstrated. In conjunction with humidity standards for determination of water vapor concentration, these spectroscopic measurements yielded relative uncertainties in line intensities less than 0.5 %. Figure 8 shows measured spectra (symbols) and theoretical spectra (solid lines) for a pair of overlapping water vapor absorption transitions, each case corresponding to a given total gas pressure (with N_2 as the buffer gas). These results illustrate that the spectral resolution and linearity of the FS-CRDS method enable precise quantification of pressure broadening, collisional narrowing and asymmetries of the absorption line shape, thus minimizing systematic errors in the determi-

nation of number density and line intensity that typically arise from instrumental line broadening effects. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 935 nm. In FY 2006, we constructed a portable FS-CRDS apparatus to probe H_2O absorption in the 1.39 m region, and we tested its performance using a transfer standard permeation tube water vapor source and a transfer standard hygrometer linked to the LFPG. We measured spectra with signal to noise ratios exceeding 2500:1 and we demonstrated a water vapor detection limit of 0.7 nmol mol^{-1}. In another FS-CRDS study in FY 2006, we made high-resolution measurements of blended water vapor spectra demonstrating the ability to deconvolute closely space overlapping lines. In this study, line intensities were determined with relative uncertainties of 0.6 %.

■ In collaboration with Matheson Tri-Gas and Tiger Optics, we demonstrated sensitivity of less than 10 nmol/mol for H_2O in phosphine using commercially available instrumentation, the first such measurement with this low sensitivity (see Fig. 9. Additional experiments at NIST with arsine indicated that new wavelengths were needed to measure H_2O in arsine to similar sensitivities. We have also used the NIST hazardous gas CRDS system to measure water vapor concentrations in the toxic gases phosphine and arsine in the 940 nm spectral region. Testing of both arsine and phosphine in this spectral region indicated that the least overlap with host gas lines, and hence the highest sensitivity to water contamination, is present for the H_2O line at 943.082 nm. Future experiments will characterize this line for pressure broadening coefficients and ultimate sensitivity limits. Figure 10 shows a typical H_2O spectrum in arsine.

■ We have used a similar FS-CRDS system to measure water vapor concentrations in the toxic gas phosphine in the 935 nm spectral region. Testing of five strong water absorption lines in this region indicated that the least overlap with phosphine lines, and hence the highest sensitivity to water contamination, is present for the line at 943.082 nm. Future experiments will characterize this line for pressure broadening coefficients and ultimate sensitivity limits. Figure 9 shows a typical H_2O spectrum obtained with the automated FSSM-CRDS system and comparison with previously published measurements.

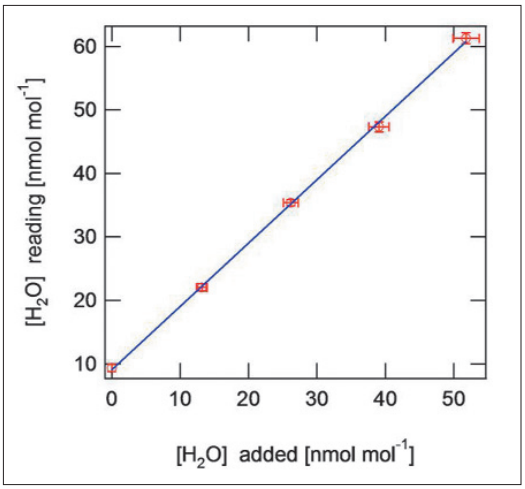

Figure 9. Response curve for commercial instrument measuring H_2O in phosphine with sensitivity of 1.3 nmol mol^{-1}.Zero offset of 9 nmol mol^{-1} is most likely from residual H_2O in phosphine.

COLLABORATIONS

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

Matheson Tri-Gas, Mark Raynor and Hans Funke; CRDS measurements of trace moisture in phosphine.

Tiger Optics, Yu Chen; CRDS measurements of trace moisture in phosphine.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers and humidity generators for standards laboratories.

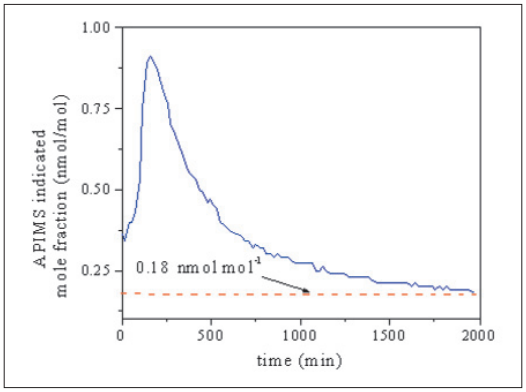

Figure 10. Pressure dependence of the absorbance spectra for H_2O in arsine showing feasibility of measuring H_2O concentrations on the order of 50 nmol mol^{-1} of various process pressures.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Tiger Optics, Calvin Krusen ; evaluation of commercial CRDS technology.

Air Products and Chemicals Inc.; CRDS measurements of trace H2O in corrosive process gases.

Restek Corporation, David Smith; drydown rates for stainless steel tubing.

Publications

J. T. Hodges, D. Lisak, N. Lavrentieva, A. Bykov, L. Sinitsa, J. Tennyson, R. J. Barber, R. N. Tolchenov, *"Comparison between theoretical calculations and high-resolution measurements of pressure broadening for near-infrared water spectra,"* Journal of Molecular Spectroscopy, doi:10.1016/j.jms (2008).

D. Lisak, J. T. Hodges, *"Low-uncertainty H2O line intensities for the 930-nm region,"* Journal of Molecular Spectroscopy, doi:10.1016/j.jms. (2007).

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Physical Properties of Liquid Precursors

Technical Contacts:
R. Berg

Goals

New materials used in gas phase processes will require new measurements and standards for their efficient delivery to the wafer surface. The National Institute of Standards and Technology (NIST) is supplementing its project to measure the thermophysical properties of semiconductor gases with a new effort to measure the relevant properties of liquid precursors. Vapor pressure is the most important property because it controls the behavior of vapor delivery devices. Therefore, the project's first goal is to produce accurate vapor pressure data for relevant liquid precursors from room temperature to as high as 200 °C. Such data will improve the modeling of chemical vapor deposition processes and the design and use of bubblers and other devices that deliver precursor vapors. Other goals are to characterize the thermal stability of liquid precursors and to devise a method for measuring vapor pressure that is suitably accurate yet more convenient than existing methods.

Customer Needs

Precursors for chemical vapor deposition are frequently liquid compounds that, until recently, were either rare or nonexistent. Their vapors are delivered to the process chamber either by direct injection (flash evaporation) or by bubbling a carrier gas through the liquid held in a "bubbler." Anecdotes from companies that either sell liquid precursors or sell the associated process equipment suggested an industrial need for improved property data of these specialty chemicals. Designers and users of mass flow controllers, bubblers, and other gas and liquid delivery devices could use such data to optimize the performance of those devices.

Vapor pressure determines the concentration of the precursor-carrier mixture produced by a bubbler, and it sets a lower limit on the wall temperature of the delivery line and process chamber. Although high vapor pressures are preferred, the acceptable range is wide. For example, when heated to 100 °C, the vapor pressure of the widely used liquid TEOS (tetraethyl orthosilicate) is $P_V(100\ °C) = 12$ kPa. In contrast, a candidate precursor might be considered even if its vapor pressure were 100 times lower, say $P_V(100\ °C) = 0.1$ kPa.

Other important properties include liquid viscosity and thermal stability. Viscosity can affect the performance of injection systems. Thermal stability is important because the precursor's decomposition rate may limit the process's upper operating temperature and thereby the vapor pressure.

This work is guided in part by the output of a workshop organized by NIST at Semicon West 2006 with the goal of soliciting directions for research on the physical properties of gases and liquid precursors. A report of the workshop is available at *http://www.cstl.nist.gov/div836/836.06/*. Although some precursors, such as TEOS, have been used for many years and have well known properties, others are poorly characterized because they were only recently created or identified. As an example of the resulting diversity, precursors used recently by researchers to make hafnium oxide have included hafnium nitrate, hafnium chloride, tetrakis-dimethylamino hafnium, and tetrakis-diethylamino hafnium. The diversity inherent in research and the proprietary concerns of precursor manufacturers are considerations in selecting a precursor to characterize. Several workshop participants suggested that NIST first measure the example precursors named by the SEMI task force on precursor specifications (Liquid Chemicals committee / Europe). The workshop report lists some of those examples, and a broader range of precursor examples is listed in the supplementary table of precursors attached to the ITRS. The workshop participants pointed out that, in addition to vapor pressure, other important properties include thermal stability, liquid viscosity, and materials compatibility.

Technical Strategy

NIST will identify and assess the quality of existing vapor pressure data of compounds such as Hf $[(CH_3)_2N]_4$ (acronym TDMAH). NIST will also fill gaps in the existing data by developing apparatus capable of accurate vapor pressure measurements. The resulting accurate databases will be provided to industry. NIST also will investigate alternate methods to measure vapor pressure.

DELIVERABLES:

- Automate and test apparatus to measure the vapor pressures of metal-organic precursors. 2Q 2008

The apparatus uses pressure gauges that operate at the same temperature as the sample. This direct method was chosen over indirect methods that rely on, for example, thermogravimetric

analysis or nuclear magnetic resonance. Challenges include achieving appropriate control of the sample temperature, handling the vapors of hazardous samples, and avoiding systematic errors due to the presence of decomposition products, dissolved gases, and other impurities. Tests will include measurements of the vapor pressures of well characterized liquids.

DELIVERABLES:

- Identify existing vapor pressure data. 3Q 2008

Existing data can be found in journal publications, the NIST Chemistry WebBook, NIST standard reference database 87, and other databases. The applicability of estimation techniques, such as group contribution methods, will be examined.

DELIVERABLES:

- Develop a system to measure the decomposition rate of metal-organic vapors. 3Q 2008

Some metal-organic precursors are known to decompose at temperatures below 200 °C. The new system will use a gas chromatograph / mass spectrometer to identify the decomposition products as well as contaminants present in the original sample. The capillary sampling system, which will be suitable for metal-organic vapors at 200°C, will include a modified commercial switching valve, and a heated capillary transfer line.

DELIVERABLES:

- Investigate alternate methods to measure vapor pressure. 4Q 2008

The initial investigation will include an estimate of the method's uncertainty and the identification of sources of systematic error. The leading candidate is speed-of-sound measurements of a mixture comprising the equilibrium vapor plus one atmosphere of an inert gas.

DELIVERABLES:

- Investigate alternate methods to measure vapor pressure. 4Q 2008

Accomplishments

■ The vapor pressure apparatus, which consists of an oven, a vacuum system, a novel thermoelectric temperature control scheme, capacitance diaphragm pressure gauges, and other appropriate instrumentation, has been upgraded to allow runs lasting multiple days. Such runs are needed due to the long time required for the *in situ* pressure gauges to recover from temperature changes. Temperature stability within the requirement of 20 mK has demonstrated up to 200 °C, and measurements of the vapor pressure of water showed agreement with accepted values up to the gauge limit of 100 kPa (at 100 °C). A gas chromatograph / mass spectrometer was recently purchased and is being integrated with the vapor pressure apparatus.

■ Gas flow measurement research at NIST in support of the semiconductor industry created a quartz capillary flow meter with a hydrodynamic model of unprecedented accuracy. One spin-off application was use of the model with a ratio viscometer that yielded values of unprecedented accuracy (< 0.1 %) for the viscosities of argon, hydrogen, methane, ethane, and xenon at temperatures from 200 K to 400 K. Another spin-off is a capillary flow meter that provides a 0.1 sccm reference gas flow for calibrating spinning rotor vacuum gauges.

Publications

E. F. May, R. F. Berg, and M. R. Moldover, *"Reference viscosities of H_2, CH_4, Ar and Xe at low densities,"* International Journal of Thermophysics **28**, 1085- 1110 (2007).

Analysis Tools and Techniques Program

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip exceeds 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements. Those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling that allows us to bridge those areas where measurements can be done to those where knowledge is needed, but measurements cannot be done is critical. Significant improvements in tools capable of analyzing properties of defect particles in the sub-30 nm size are urgently needed. Global and local stress measurement techniques need to be developed.

Thin-Film X-Ray Metrology for Microelectronics

Technical Contacts:
J. P. Cline
D. Windover

Goals

This multi-year collaborative effort between SEMATECH, ISMI, and NIST will provide the semiconductor community with the measurement methodology and calibration capability for accurate thin film characterization using X-ray reflectometry (XRR) and high-resolution X-ray diffraction (HRXRD).

Customer Needs

In recent years, the semiconductor industry has driven scientific advancement in nanometer-scale material coatings to unprecedented uniformity in thickness, control of composition, and uniqueness of electrical and mechanical properties. Nanotechnology is the fastest growth area of industry in the United States today. Simultaneous to this rapid advance in thin film processing technologies, the X-ray diffraction user community and instrument manufacturers have collaboratively developed techniques such as XRR and HRXRD that permit the quantitative measurement of thin film characteristics, such as thickness, density profile, composition, roughness, and strain fields. With XRR and HRXRD analysis methods, structural parameter modeling by conventional methods can be an intractable problem, involving deconvolution of instrument response, data modeling theory, model selection, and model refinement/fitting, which has prevented the realization of the techniques' potential in the characterization of nano-dimensional thin film structures. This NIST-SEMATECH-ISMI effort addresses the mounting industry call for accuracy in thin film characterization (in particular for thickness, density, and roughness, determination) and epitaxial layer characterization (in particular for thickness, composition, and lattice strain). Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather, they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

NIST addresses the need for XRR and HRXRD standardization and metrology through the production of Standard Reference Materials (SRMs) which aid end users in instrument calibration (see Figure 1). However, production of SRMs requires a substantial instrumentation infrastructure, years of researcher time, and a collaborative community invested in the realization of the SRM to completion. The technical approach to SRM production can be broken into three parallel goals: 1) manufacture of a stable, robust, and well characterized calibration artifact, 2) construction of a stable, well characterized measurement apparatus for performing certification measurements, and 3) development of first principles, data analysis procedures with well-founded apriori structural model(s) and statistically verifiable parameter (and model) uncertainty estimates (see Figure 2). To meet goal 1, NIST has established close working relationships with SEMATECH, ISMI, and other industrial and academic partners for developing and manufacturing superlative calibration artifacts for use as SRM feedstock. For addressing goal 2, NIST has constructed a laboratory for X-ray work using three International System of Units (SI) – traceable HRXRD and XRR instrument known as the Ceramics Division Parallel

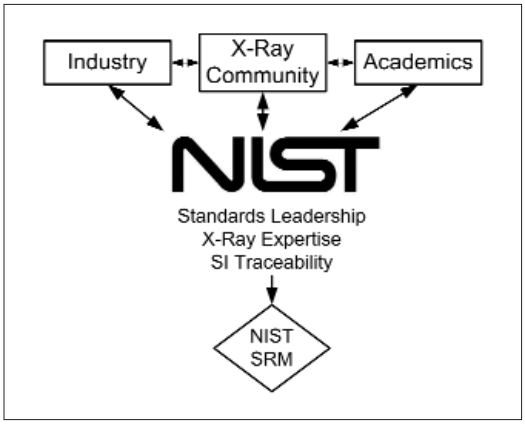

Figure1. Diagram of interactions between NIST and the X-ray community in the production of Standard Reference Materials (SRMs). NIST has many two-way collaborative interactions preliminary to the release of the final product.

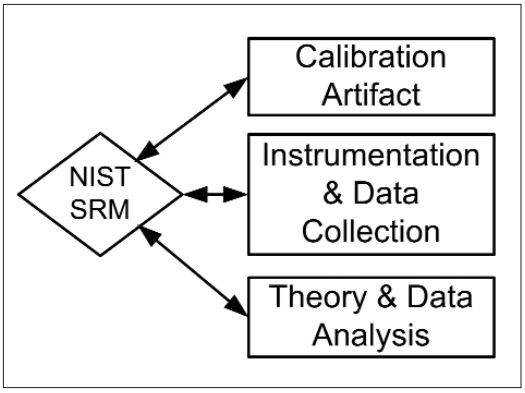

Figure 2. Essential elements of NIST's technical approach to SRM development.

Beam Diffractometer (CDPBD) which is located in the Advanced Measurement Laboratory (AML) at NIST. In reaching goal 3, NIST has collaborated with X-ray industry leaders in developing statistically-sound multivariate first principles XRR analysis (FY07). These same approaches will be applied to HRXRD analysis in the future (FY08+).

NIST XRR and HRXRD Instrumentation: the CDPBD

Over the past decade, NIST has applied considerable resources to developing the CDPBD for SI-traceable measurements of Powder XRD, Epitaxial HRXRD, and thin-film XRR artifacts for the Standard Reference Materials (SRM) program (see Figure 3). Over a similar timeframe, the Physics Laboratory developed the Physics Laboratory X-Ray Reflectometer (PLXRR) specifically for XRR characterization of semiconductor thin-film artifacts. Next year (FY08/09), we will be working with the Physics Laboratory to integrate the PLXRR into the XRR SRM effort. This will allow us cross-laboratory measurement comparisons in our certification process.

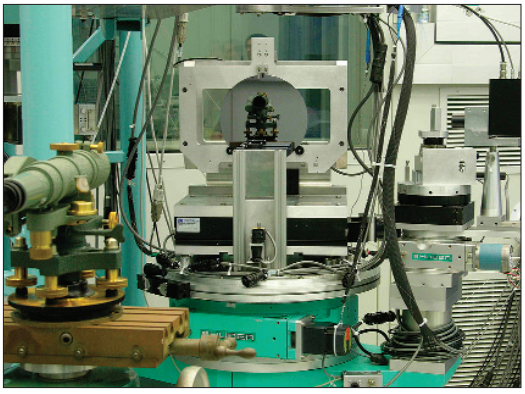

Figure 3. Ceramics Division Parallel Beam Diffractometer (CDPBD) located in the Advanced Measurement Laboratory at NIST seen during a wafer alignment procedure. The X-ray source (off image left) is collimated through a monochromator (left, behind vertical pole) and is diffracted/reflected by a wafer (center) into a detector (right). Sample and Detector rotation axes must be coplanar with the incident and diffracted/refracted X-rays. This requires external optical alignment methods using autocollimation, e.g., by a Wye level (front,left).

SI traceability in either lattice parameter (HRXRD), d-spacing, or film thickness (XRR), *d*, requires simultaneous traceability in X-ray wavelength, λ, and diffraction angle, θ, following Bragg's law of diffraction: $2d = n\lambda / \sin(\theta)$. The present NIST instrument development project involves establishing SI traceability for both the diffraction angle and wavelength measurement on the CDPBD. Establishing SI traceability of the diffraction angle requires implementing optical encoding on the two rotation stages used to move the sample and detector. The optical encoder errors are then "mapped" using an external angle

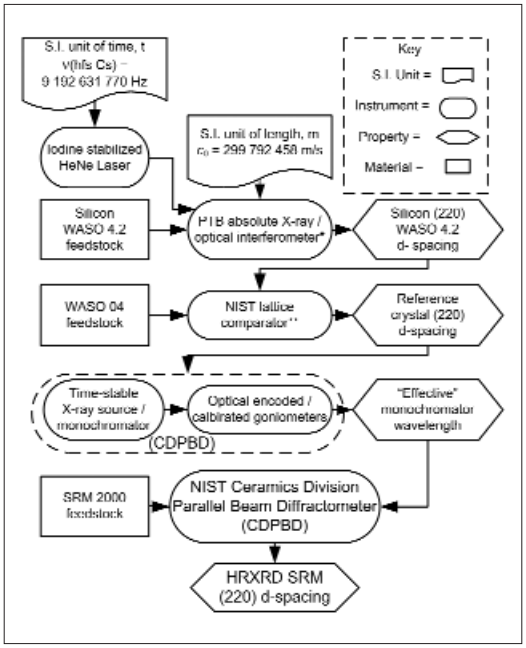

Figure 4. NIST International System of Units (SI)-traceability pathway for high-resolution X-ray diffraction (HRXRD) SRMs using the CDPBD. Measurements from X-ray/optical interferometry at Physikalisch-Technische Bundesanstalt (PTB) in Germany and lattice comparison measurements at NIST provide femtometer-scale expanded uncertainty in lattice spacing (d-spacing) measurements for the SRM.

reference to generate SI-traceable relative uncertainties for each axis. The rotation stages presently have accuracy bounds of ± 2.0 μrads (± 0.4 arc seconds). Calibration experiments and collaboration with encoder manufacturers are currently under way to achieve an approximate order of magnitude improvement in accuracy. Establishing SI traceability in wavelength involves constructing a stable, well modeled optics assembly to convert angular and energy divergent radiation from an X-ray source into parallel, monochromatic radiation for use in diffraction. The CDPBD uses a monochromator with Si (220), 2/4-bounce channel-cut crystals to filter the rotating anode Cu source into a source of highly parallel, single energy X-rays. SI traceability in X-ray wavelength from our source will be performed using an SI-traceable reference crystal (whose d-spacing has been measured with relative standard uncertainty of 3 in 10^{-8}). The X-ray wavelength for our instrumentation currently has a relative standard uncertainty of ≈ 1 in 10^{-5} (FY06). For the certification of the HRXRD SRM this year (FY07) we developed a "sequential delta-d method" for reducing the uncertainty of d-spacing of HRXRD measurements due to instrument alignment effects through the use of a WASO 04 reference crystal from the Avogadro Project (See Figure 4). This has allowed for d-spacing measurements with femtometer-scale expanded uncertainties on the CDPBD. Further improvements in angle and wavelength metrology should further improve the instrumental limits of the NIST instrumentation for HRXRD and XRR measurements (FY08+). An enhancement currently being incorporated into the CDPBD is a NIST constructed spherical air bearing for the goniometer assembly to allow translation and goniometer tilt to be orthogonal for alignment of XRR and HRXRD measurements (see Figure 5). NIST's studies of instrumental alignment parameters and their effect on structural model uncertainty will be used to establish guidelines for instrument response modeling on commercial instrumentation using future HRXRD and XRR SRMs.

The HRXRD SRM effort was started nearly a decade ago with collaborations between the NIST Materials Science and Engineering Laboratory (MSEL), the NIST Physics Laboratory, Bede Metrology, and Applied Materials. The approach was to use a commercially viable SiGe epitaxial process as a feedstock structure for a HRXRD SRM (see Figure 6, next page). The structure was

Figure 5. Spherical air bearing for CDPBD goniometer, seen during assembly. Spherical male/female components with 0.7 m radius of curvature for goniometer tilt (top), and kinematic air bearing assembly for goniometer translation (center, right).

deposited on a 200mm wafer and then sectioned into 25mm specimens after performing HRXRD measurements for certification. Structures were produced in FY01 and NIST instrumentation capable of SI-traceable determination of Si substrate d-spacing became available last year (FY07). The mature, temporally stabilized SiGe feedstock was then measured using transmission and reflection geometries to provide information on both the Si substrate d-spacing and the SiGe epitaxial surface structure.

Due to the extended duration of this SRM project, completion of target certification was subdivided into two phases to provide timely product rollouts for the community. The premise of the first phase of this SRM was to provide an SI-traceable d-spacing with low expanded uncertainty to aid in basic instrument calibration. If one assumes that the wavelength is relatively stable (possible with an epoxy-mounted channel cut monochromator), then SRM 2000 will provide correction for the diffractometer angle. The first phase of

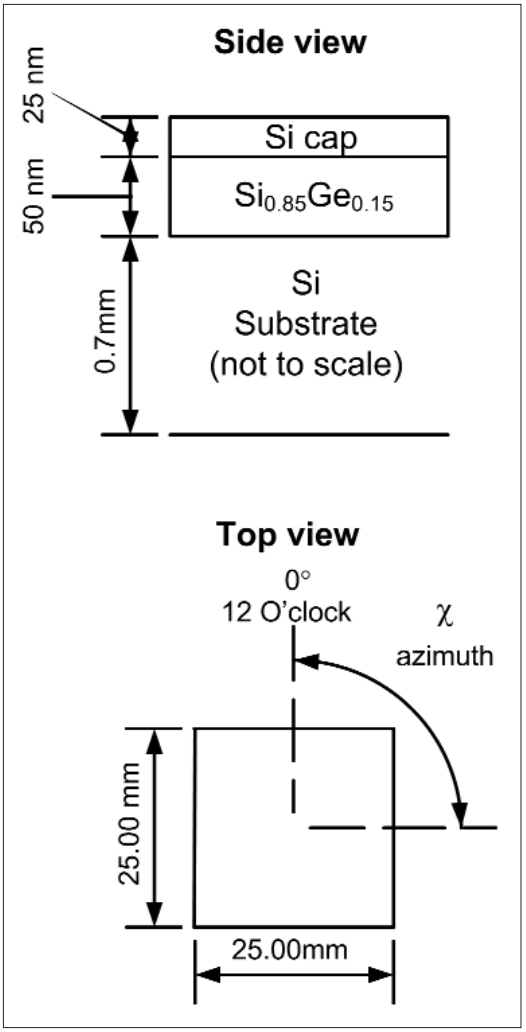

Figure 6. HRXRD SRM 2000. The multilayer structure (top) is deposited onto 200mm double polished wafers and has been sectioned, post-measurement into 25mm x 25mm specimens for sale to end users (bottom). The thicknesses and concentrations here are the nominal deposition values. The first phase of the SRM certification involves only the substrate Si lattice parameter.

the certification was the HRXRD tech transfer for this year (FY07/08). The second, yet to be completed, certification phase will provide information on a SiGe epitaxial layer for calibration of instrument response (how well the X-ray source is behaving) and short range angle determination (how well the goniometer is behaving) near the (004) Si substrate peak. This calibration information would be most useful in quantitative strain determination using HRXRD. The difficulty here involves determination of the correct structural model for the deposited epilayer. We are currently working with instrument vendors at Bede, Bruker, and Panalytical and with NIST Synchrotron Methods staff to address this modeling issue (FY08+).

XRR SRM development

The XRR effort involves two parallel characterization projects being performed on identical, temporally stable, multilayer artifacts supplied by SEMATECH. The NIST project consists of in-house XRR and HRXRD characterization with International System of Units (SI)-traceable measurement instrumentation and SI-traceable, first principles data modeling including Bayesian analysis providing refinement of instrumental and model parameters as well as structural model selection. In parallel to this NIST measurement project, SEMATECH will measure or have measurements performed using commercial "in-line" XRR instrumentation and NIST will analyze these data with commercial software to study the limitations of commercial instrumentation and software modeling. Combining results from both studies will ultimately allow accuracy traceability and error estimation for commercial instrumentation. This work will also address theoretical XRR modeling limitations and compare software model refinement and model selection approaches. The multi-year collaboration will provide the community with total error budget estimates for a given XRR structural analysis approach and instrumentation. This work will take approximately three years to address the issues discussed [FY 05, 06, and 07]. The progress in FY05 included a comprehensive, first principles development of the XRR theory necessary for traceable modeling of data and a first round of measurements on artifacts by commercial and NIST instrumentation. FY06 work explored the application of an approximate Bayesian model selection method to compare the relative probability of different structural models for measured XRR data. Preliminary results with simulated XRR data have shown success in determining the initial structural model used to generate the simulated data. FY07 deliverables will include the development of an XRR prototype SRM to clarify instrument response issues and provide calibration of instrumentation at SEMATECH.

NIST XRR Study – The standard NIST approach for reducing uncertainty in a measurement technique involves the generation of a Standard Reference Material (SRM). Figure 1 shows the three

parallel research aspects needed for the development of an XRR SRM: (1) the manufacture of a robust thin film calibration artifact with a high degree of temporal stability and contamination and/or oxidation resistance, (2) the development of SI-traceable measurement instrumentation, and (3) the creation of an SI-traceable, first principles data analysis approach. Figure 2 shows the current status of steps required to address these aspects for our XRR SRM project.

Our collaborative effort with SEMATECH allows us to examine semiconductor industry relevant structures as potential candidates for an XRR calibration artifact. NIST has also engaged other national metrology institutes (NMIs) in an effort to assess the temporal stability of international NMI pre-standards. Both PTB of Germany and NMIJ/AIST of Japan have provided us with structures for comparative XRR analysis. This cooperative study will help gauge which thin films structures provide stable, well-defined, refinement parameters suitable for SI-traceable modeling.

NIST is currently developing first principles, SI-traceable XRR software to analyze data and refine model and instrument response parameters. XRR analysis is essentially an "inverse problem" in which we select input parameters for a "guessed" structural model. This model is then used to simulate data that is compared with measured data and "Goodness of Fit" parameters are determined. This process is repeated until a "best fit" or best "Goodness of Fit" is found and the "best fit" model parameters become the "refined" model parameters used to describe the real structure. Three major questions limit the effectiveness of this current XRR modeling approach: (1) How do we accurately simulate the data using a structural model? (2) How do we know which structural model describes the measured structure? (3) How do we accurately compare simulated and measured data? The NIST software development effort will attempt to answer each of these questions.

To address the model data simulation issue, we have developed XRR modeling based on the elementary Parratt formalism of discrete layer structures and assuming perturbation-based roughness convolution while keeping the minimum number of layers necessary to describe a structure. This approach will in the future combine XRD, HRXRD and XRR in the same fundamental modeling theory and allow for SI traceability in derived refined parameters (FY08+). To address the question of model accuracy, we are implementing a Bayesian/Maximum Entropy analysis approach to determine the probability that a given structural model correctly describes a given data set. This model selection component is essential to determining the validity of initial structural assumptions in any XRR analysis. Addressing the third question is of considerable interest. Commercial refinement approaches attempt to optimize a solution through a "chi squared" or other minimization criterion by using e.g., genetic algorithms. This approach attains fast solution times most compatible with process-line requirements, at the loss of statistical data required for parameter uncertainty calculations. NIST, in collaboration with several companies, is developing a statistical sampling based method using a Markov Chain Monte Carlo (MCMC) formalism to generate SI-traceable uncertainty estimations. The MCMC approach is necessary for developing formal Bayesian model selection methods (FY08+) to complement existing Approximate Bayesian approach.

NIST/SEMATECH XRR Study – The NIST/SEMATECH project consists of measurements and analysis from commercial instrumentation to allow comparison and calibration transfer from NIST SI traceable measurements and analysis.

The NIST/SEMATECH project combines measurements with commercial "in-line" XRR instrumentation with complimentary compositional analysis results as feedback for comparison with NIST measurements performed in parallel on the same artifacts. The measurement and modeling work at NIST will provide SI-traceable XRR measurements and parameter analysis for artifacts and potential candidate SRMs. The collaboration work with SEMATECH allows interface and calibration transfer between NIST SI-traceable measurements and "in-line" instrumentation. NIST will then use results from NIST SI-traceable measurements, SEMATECH commercial measurements and modeling, and NIST SI-traceable XRR modeling, to quantify error bounds and overall error budgets on the accuracy and precision possible from commercial instrumentation and commercial modeling software.

Quantity	Reference value	Expanded Uncertainty *U(i)* for k=2
d_{SRM}	0.1920161 nm (at 22.5 C)	0.87 fm

Table 1. Certified reference values for SRM 2000 Si Substrate d-spacing (220).

Calibration and accuracy determination of commercial instrumentation are the primary goals of this collaboration. To achieve these goals, we need to develop accurate instrument response functions for the commercial instrumentation being calibrated. The instrument response function for commercial instrumentation may be the dominant term in the overall accuracy budget for XRR measurements. To address instrumentation effects on accuracy, work must be performed with different commercial XRR system geometries to discover the mechanical alignment parameters that dominate the error budgets of each system. This will require cooperation from instrument vendors to provide the necessary information or provide detailed instrument response functions directly. The incorporation of instrument response parameters into NIST modeling will allow for comparison between traceable measurements at NIST and measurements on commercial instrumentation in the field. The NIST instrument response function information will be developed through our instrument traceability study discussed earlier. We can then combine specific instrument "corrections" to the accuracy error budget and use a calibration artifact such as a temporally stable thin film structure measured on the commercial instruments and at NIST to provide instrument calibration and stability monitoring (FY07+ deliverable).

HRXRD and XRR Project Deliverables – The final project results available to SEMATECH will include HRXRD and XRR uncertainty estimations based on NIST HRXRD and XRR software and the calibration artifacts necessary for optimizing the performance of commercial "in-line" and laboratory XRR instruments. Theoretical uncertainty estimations provided by NIST software and simulated structural data will determine the limitations of XRR applicability for arbitrary multilayer systems on commercial XRR instrumentation (FY08+). Calibration artifacts measured on NIST SI-traceable instrumentation will allow routine system monitoring, alignment calibration, and instrument response function comparisons to ensure commercial instrument precision and stability. These deliverables will dramatically improve the precision and accuracy of conventional HXRXRD and XRR characterization of multilayer structures which exhibit well-established composition and uniformity (FY08+ deliverables).

DELIVERABLES:

- NIST analysis of HRXRD SRM measurements. 4Q 2007
- NIST release of HRXRD SRM certification. 2Q 2008
- NIST development of XRR pre-standard structure. 2Q 2008
- NIST analysis of NIST XRR pre-standard measurements. 4Q 2008

Accomplishments

■ In FY05, the CDPBD moved to equipment space in AML at NIST which provides instrument temperature stability of ± 0.02 °C. Preliminary calibration of the angle measurement has been assessed for uncertainty determination (accuracy determination has been completed) and improvements using a new compensation approach (being developed through a joint National Metrology Laboratory effort with PTB) will be implemented (FY07). First principles XRR theory development with emphasis on justifying approximations present in commercial XRR software was completed (FY06) and a dynamical scattering based model has been implemented with Monte Carlo Markov Chain (MCMC) methods for structural parameter refinement and formal parameter uncertainty analysis (FY07). A pre-standard XRR test structure has been requested from ISMI for NIST SI-traceable measurement in this year (FY08) with SRM development in the future (FY09+).

■ *FY07 Technical transfer: NIST HRXRD pre-standard wafer and measurements SEMATECH and X-ray industry partners* – In FY07, we measured our HRXRD feedstock wafers and provided a wafer and sectioned specimens to SEMATECH along with NIST HRXRD data for collaborative studies. We also provided sectioned specimens to all the major X-ray in-

strument vendors for internal calibration studies and for independent, complementary measurements on the feedstock. The collaboration between NIST and SEMATECH in Thin-film X-ray Metrology on previous XRR projects has facilitated this sharing of pre-standards with the semiconductor community and with semiconductor tool manufactures at the early stages of SRM production to better achieve the results that the community needs as fast as possible.

■ *FY07/8 Technical transfer: NIST HRXRD SRM certification to industry* – In FY07, we completed the first phase of certification analysis for our HRXRD SRM (see Table 1). The SRM and the certification reports have been provided to the SRM Program for packaging and release of SRM 2000 for sale to end users and tool manufacturers. This SRM development has involved collaboration with the semiconductor industry (Applied Materials and SEMATECH) and with X-ray tool manufacturers (Bede, Bruker, Panalytical, Rigaku, and others) providing NIST with valuable feedback on our approach during the multiyear certification process. The SI-traceable nature of SRM 2000 has allowed us to provide the semiconductor and nanotechnology industries with a nanometer-scale length standard (d-spacing) with femtometer-scale expanded uncertainty, thereby serving as the most accurate, commercially available, nano-scale "meter stick" available today.

COLLABORATIONS

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PTB, Precision Metrology – Peter Thomsen-Schmidt.

LETI – Emmanuel Nolot.

NMIJ/AIST – Toshiyuki Fujimoto.

Bede Scientific Inc. – Matthew Wormington.

Bruker AXS – Assunta Vigliante & Arnt Kern.

Coruscavi – David L Gil.

Jordan Valley Semiconductors – Dileep Agnihotri.

Panalytical – Martijn Fransen.

Rigaku MSC – Joe Formica

Technos International – Meredith Beebe

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High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

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Goals

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES) and an X-ray absorber fabricated on a micromachined Si^3N^4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator. We are presently simplifying this refrigerator to reduce system costs and increase the accessibility of microcalorimeter technology.

Customer Needs

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council (ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

"Promising new technology such as high-energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMS located in the clean room." 2003 International Technology Roadmap for Semiconductors.

Technical Strategy

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Arrays of X-ray microcalorimeters for increased collection area and count rate have been demonstrated and their energy resolution is comparable to single sensors. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg, Maryland for collaborative use in studying problems of interest to the industry (Fig. 1), and to work with other partners in disseminating the technology.

DELIVERABLES:

- Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Provide support for partners working to commercialize microcalorimeter technology and make it more widely available to the semiconductor industry.

2. The adiabatic demagnetization refrigerator that provides 0.1 K operating temperatures is a crucial part of a microcalorimeter system. To date, adiabatic demagnetization refrigerators have been precooled to 4 Kelvin with liquid nitrogen and helium. However, the use of liquid cryogens is an obstacle to potential microcalorimeter users. Consequently, it is desirable to precool the adiabatic demagnetization refrigerator with a push-button mechanical cryocooler whose only consumable is electricity.

- Design and build an adiabatic demagnetization refrigerator cooled by a pulse tube mechanical cryocooler. Understand and minimize the electrical and mechanical effects of the cryocooler on microcalorimeter and electron microscope operation.

Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive 3He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES:

- Demonstrate successful operation of a X-ray microcalorimeter cooled by a tunnel-junction refrigerator that could be coupled to a simple ^{3}He refrigerator.

4. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated and been used to successfully read out eight microcalorimeters under X-ray illumination. Significant increases in multiplexer bandwidth and pixel-handling capacity are possible based on evolutionary design improvements.

DELIVERABLES:

- Demonstrate improved SQUID multiplexer performance and multiplexed operation of increasing numbers of microcalorimeters under X-ray illumination. Characterize multiplexer performance.

Accomplishments

■ We designed and built an adiabatic demagnetization refrigerator that is precooled by a mechanical cryocooler. This simple and compact system is operated by the push of a button and requires no liquid cryogens. Because the cry-

ocooler achieves a base temperature of 2.8 Kelvin, lower than that of liquid helium, the operating time of the demagnetization refrigerator below 0.1 K is significantly extended. In addition, we have demonstrated undegraded operation of a high resolution microcalorimeter in the electromagnetic environment of the cryocooler and its control electronics. We have also characterized the effects of the mechanical vibration of the cryocooler on other instruments such as a scanning electron microscope. Through a combination of vibration reduction measures, we have almost completely eliminated distortion of the microscope image due to the cryocooler. A photograph of the pulse tube cooled – demagnetization refrigerator undergoing vibration testing on an electron microscope is shown in Fig. 2.

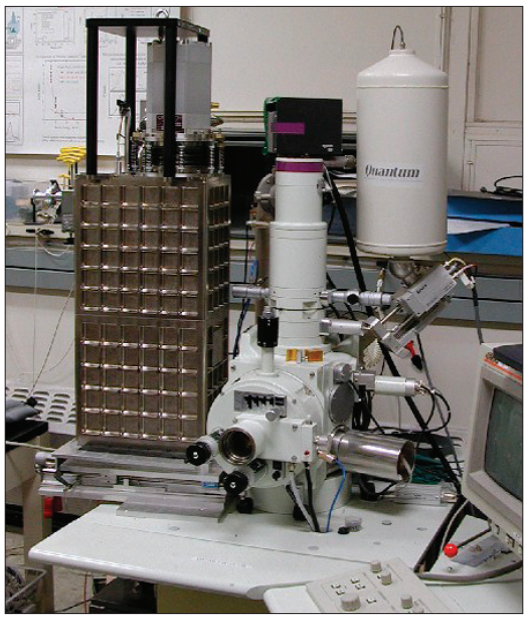

Figure 2. Cryogen-free adiabatic demagnetization refrigerator (left) undergoing vibration testing on a scanning electron microscope.

■ We developed a new generation of microcalorimeters that incorporate additional normal metal regions to suppress internal noise. In addition to being more stable and easier to bias, the energy resolution of these microcalorimeters is significantly improved. We demonstrated an energy resolution of 2.4 eV FWHM at 5.9 keV. and 2.0 eV at 1.5 keV; these figures are over 30 times better than the best high resolution semiconductor-based detectors currently available.

■ We continue to support the microcalorimeter system installed on a CSTL scanning electron microscope in Gaithersburg, Maryland. We have also provided support to the company STAR Cryoelectronics who are working to commercialize microcalorimeter technology. We tested X-ray microcalorimeters fabricated by STAR Cryoelectronics and demonstrated an energy resolution better than 15 eV at 6 keV (Fig. 3).

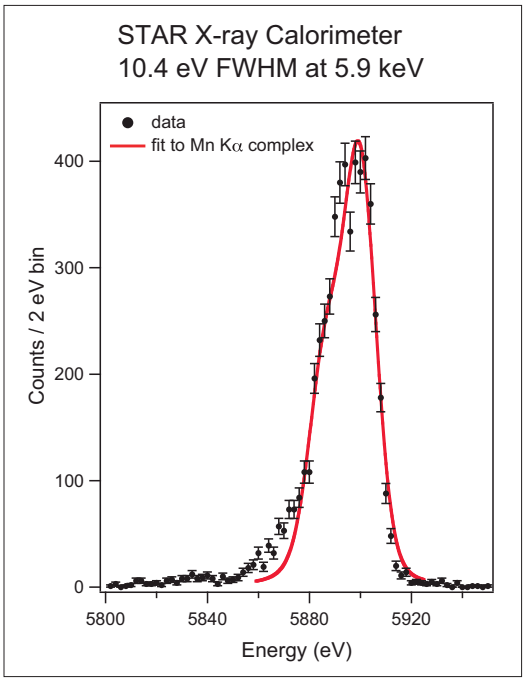

Figure 3. x-ray spectrum from commercial, star cryoelectronics microcalorimeter with better than 15 ev resolution at 6 kev.

■ We demonstrated the ability to read out 16 total TES microcalorimeters in two columns with an average energy resolution of 2.86 eV FWHM (Fig. 4).

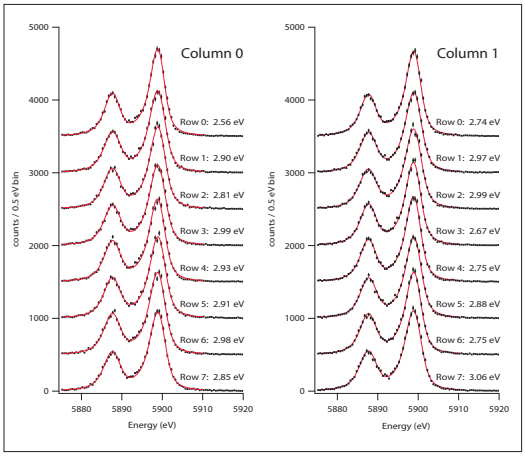

Figure 3. Spectra from 16 microcalorimeter array showing 2.86 ev resolution at 6 kev.

■ Combining this result with closed-form calculations and a new Monte-Carle software package that performs a detailed simulation of our SQUID multiplexer, we can reliably predict the future performance of the multiplexer system. In particular, with only evolutionary improvements to the basic architecture, our time-division SQUID multiplexer will be able to readout 32 detectors per channel with 4 eV resolution or better. Planned improvements include increased open-loop system bandwidth, well-matched pulse rise and fall times, lower SQUID noise, and optimization of the coupling between microcalorimeters and SQUIDs. We have built a test apparatus to house and read out up to 128 microcalorimeter pixels and are preparing to demonstrate multiplexed operation of a 4 x 32 high-resolution microcalorimeter array (Fig. 5).

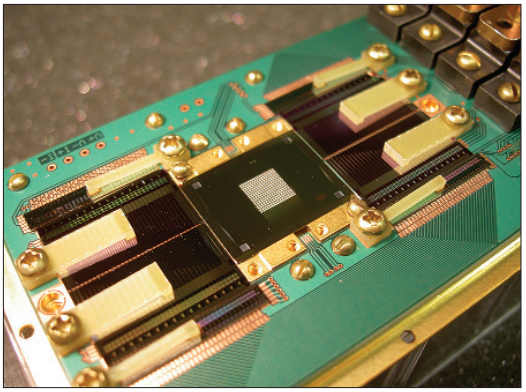

Figure 5. 128 pixel microcalorimeter array and multiplexed readout circuitry.

■ We have successfully developed an on-chip solid-state refrigerator to cool X-ray microcalorimeters from 300 mK to 100 mK. This refrigerator can greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators can be replaced by small and inexpensive 3He systems coupled to the solid-state refrigerator. The device is a superconducting analog of a Peltier cooler. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. Recently, we demonstrated solid-state refrigerators able to cool X-ray microcalorimeters over useful temperature ranges, for example, from 260 mK to 160 mK (Fig. 6). We operated the X-ray microcalorimeter and demonstrated an energy resolution near 12 eV at 5.9 keV, a record for the 260 mK starting temperature of the integrated device. This work has been featured twice on the cover of *Applied Physics Letters* and once on the cover of *Physics Today*.

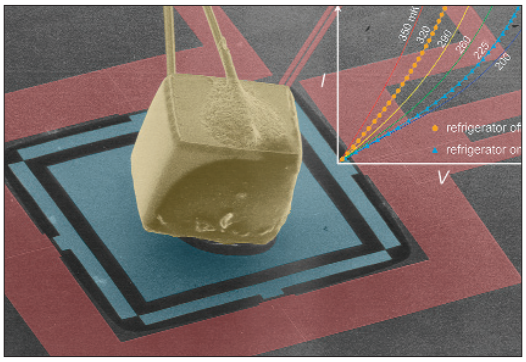

Figure 6. Colorized micrograph of solid-state refrigerator. A cube of germanium (yellow) located on a suspended, micromachined membrane is cooled by four pairs of normal-insulator-superconductor tunnel junctions. The ratio of the volumes of the germanium and the junctions is the same as the ratio of the volumes of the Statue of Liberty and an ordinary person (about 11 000). Macroscopic wires (at upper left) contact the germanium to measure its esistance; these are cooled as well.

■ We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 7). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the data collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.

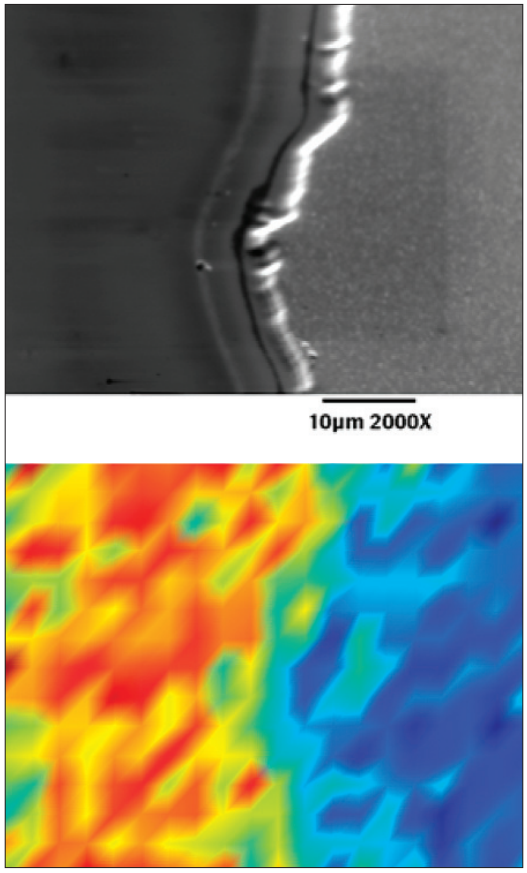

Figure 7. SEM photo (top) of an aluminum fi lm partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al Kα peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ~0.2 eV.

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Device Design and Characterization Program

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as Multi-Gate FETs (MUGFETs), fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube, spintronic, and phase change and molectronic device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. With all of these changes taking place, NIST has established the Center for Nanoscale Science and Technology (CNST), a multidisciplinary center composed of a research program and the Nanofab, a fee base, shared use user facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.

Device Characterization and Reliability

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Goals

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced and emerging CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, defect identification and defect generation mechanism, physical models for wear-out, and methodologies to determine energy band diagrams and barrier heights for advanced gate dielectric stack systems.

A specific focus is to increase the understanding of the relationship between gate metal, gate dielectric, and channel materials, their interface properties, and device electrical and reliability measurements.

Customer Needs

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (i.e, the polysilicon gate, the SiO_2 dielectric, and the silicon substrate) that was the key enabler of integrated circuit technology for half a century, must now be entirely replaced with new materials to achieve higher performance and lower power dissipation. Higher dielectric constant materials will replace SiO_2 as a gate dielectric, metal will replace polycrystalline silicon as a gate electrode, and high mobility materials will replace silicon as a channel material. New device structures such as multi-gate transistor, raised source and drain, ultra-thin body, etc. will replace the conventional planer MOSFET. Accompanying these enormous changes are new and highly complex reliability issues that must be addressed.

Consumer electronics has been the main driving force for the industry. Everyday life is increasingly relying on electronics. Many functions in modern living demand increased reliability of electronics beyond the traditional standards. Some cannot tolerate any failures. These demanding reliability requirement posts new challenges that the IC industry now must face.

The characterization of current advanced and future CMOS transistors is a major measurement challenge. It is currently not possible, for example, to reliably measure the channel mobility directly on the minimum size transistors. Thus it is difficult to know if the transistor's performance is limited by series resistance or by channel mobility. It is not possible to measure CV directly on such transistors; thus many of the basic transistor parameters must be obtained indirectly. Advanced MOSET structures may not have a way to contact the substrate, precluding the use of standard electrical characterization techniques.The issue of variability, which is a major issue for advanced CMOS technology, cannot be quantified easily without the ability of making these measurements.

The need for new measurement capability is not limited to measuring the ever smaller devices. Measuring faster is also required. High performance is one of the driving forces for continued scaling. High-performance circuits have tight tolerance on transistor parameters. It is recently becoming clear that the transient shift of transistor parameters that can cause circuit failure occurs more easily in advanced CMOS technologies than in older generations of CMOS. It also is becoming clear that reliability assurance requires that the transistor be characterized at operational speed. However, the measurement of transistor parameters at full operational speed is not currently possible. This is a major deficiency that needs to be addressed.

Device degradation is intrinsically a stochastic process. Reliability measurements must have good statistics to be useful. This is much more so in advanced CMOS due to variability issues. How to produce useful reliability data is itself a challenge that urgently needs a solution.

Technical Strategy

The main focus for this project is to develop device and reliability characterization methodologies for advanced and emerging CMOS technology.

We continue to improve electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage, Vt, instability, defect generation rates, spatial and energetic defect profiles, and long term degradation such as time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from

our collaborators. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization methods.

We will develop new measurement techniques. For example, optical-electrical combination techniques to quantify defects, defect energetics and defect positions. Such techniques are also good for band-alignment study of the gate stack. It can also be used to investigate the interface region specifically. Coupling with pure electrical techniques, a much better picture of what is happening can emerge. Another example is a specialized technique to detect a single defect to enable us to investigate how a single defect affects the behavior of a nano-scale transistor. We are particularly interested in developing new ultra sensitive CV measurement techniques to measure minimum size transistors directly. Another direction of measurement technique development is ultra-high speed measurements of transistor parameters. Finally, we will explore ways to improve the statistical quality of reliability data.

DELIVERABLES:

- Study NBTI mechanism on pMOSFETS using ultra-fast ID-VG measurement that is synchronized to the end of stress with and without precisely controlled delay. 2Q 2008
- Develop an ultra-fast and ultra-sensitive capacitance probe to measure CV curve of minimum size transistors directly, as well as to study transient CV shifts after the stopping of electrical stress. 3Q 2008
- Develop a new electro-reflectance measurement technique for the investigation of defect generation in the high- /SiO2 stack. 3Q 2008
- Extend the 1/f noise measurement from the current ~10 kHz upper limit to microwave frequency to enable the direct comparison of defects measured using charge-pumping technique for high-k /SiO2 stack. 4Q 2008
- Conduct time-dependent dielectric breakdown study of SiO2/SiC system. 4Q 2008
- Conduct electrical characterization and reliability investigation of an advanced transistor having high- gate dielectric and alternative channel materials such as InGaAs. 4Q 2008

Accomplishments

Investigation of the origin of the fast transient after NBTI stress

Experiments conducted at NIST on transistors with 1.6 nm nitrided oxide gate dielectrics have shown that the fast transient threshold (V_{TH}) shift after the stopping of NBTI stress is a sensitive function of the stress voltage (Fig. 1). This is a classic high-field stress behavior and not really related to the traditional NBTI mechanism. The trend of using very high stress fields for NBTI studies in recent years has mixed the NBTI phenomena high-field stress phenomena, causing a lot of confusion. From the well-know high-field stress phenomena, we know that both hole- and electron-trapping will take place. We also know that hole-detrapping is very efficient once the stress voltage is removed. This is the commonly observed relaxation of degradation phenomena. The good news is that hole-trapping is a strong function of stress voltage, and at the operation voltage, hole-trapping and detrapping is negligible. Thus the commonly observed relaxation phenomenon is probably not a reliability issue. On the other hand, we observed a transient improvement in transconductance (G_M) (Fig. 2) to a level better than before stress. This surprising result provides further evidence that high-field stress phenomena are at work during the "NBTI" stress. The improvement is due to electron-trapping. The trapped electrons detrap over time and the improvement eventually goes away, leaving only degradation.

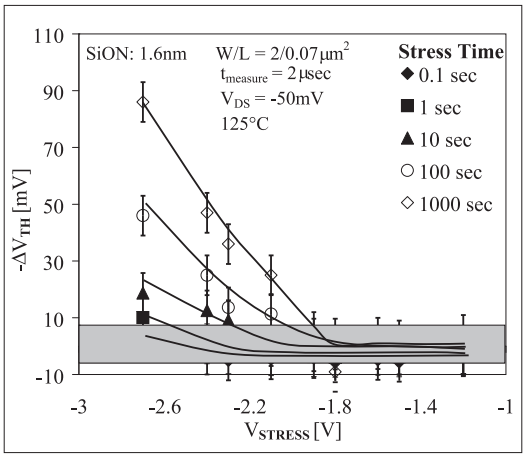

Figure 1 ΔV_{TH} as a function of stress voltage for various stress times. It is clear that the fast NBTI degradation only occurs for exceedingly high stress voltages and longer stress times. The box centered about 0 mV represents 1 standard deviation error bar. The lines are only a guide for the eye.

We are the first to make this observation and to report it. Our unique ability to extract GM reliably from a very fast measurement, plus the ability to control very precisely the time delay between a long stress cycle and very fast measurements, are the two most important factors that enable us to observe this new kind of transient. This phenomenon requires more detailed studies to be carried out before its full impact can be clarified. Details of the study will be presented at the 2008 IEEE International Reliability Physics Symposium in Phoenix, AZ, and the 2008 VLSI Technology Symposium in Hawaii.

Traps generation in ALD HfO2/SiO2 Stacks under electrical stress Using Low Frequency Noise Characteristics in combination of frequency dependent charge-pumping

Using low frequency (LF) noise as well as frequency-dependent charge-pumping current measurements, the traps created and their location in the gate dielectric stack as a function of stress polarity were studied in n-type Metal-Oxide-Semiconductor Field-Effect-Transistors (nMOSFETs) with various HfO_2 or interfacial layer (IL) thicknesses. Both techniques give a spatial profile of the traps in the gate dielectric stack, but with different penetration depth (Fig. 3). The combination of the two allows one to put together a complete defect profile in the dielectric stack. It was found that traps are created by electrical stress in the high-k layer. It was also found that trap creation is more dominant near the anode, and thus dependent on the stress polarity. This result is in conflict with results obtained from fast I_D-V_G measurement and Stress-Induced-Leakage-Current (SILC) measurement, both reported in the literature. The question of whether traps are created in the high-k layer under moderate electrical stress has far reaching consequence for future CMOS reliability. Although not our intention, our result adds more fuel to the controversy. This work will be reported in the 2008 IEEE International Reliability Physics Symposium in Phoenix, AZ.

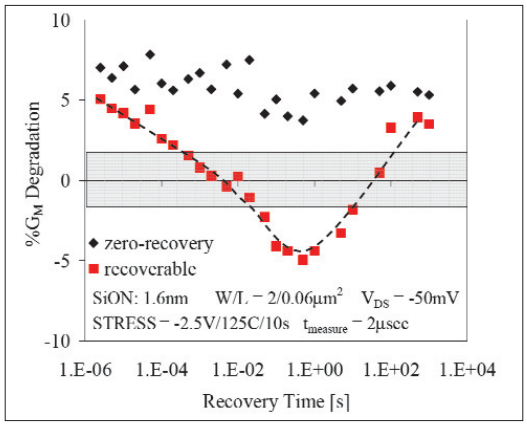

Figure 2 "Recoverable" $\%G_M$ degradation as a function of recovery time. "Zero-recovery" data are also shown for comparison. As the recovery time increases, the recoverable G_M transitions from degradation to improvement and then returns to degradation. The box centered about 0 % represents 1 standard deviation error bar. The lines are only a guide for the eye.

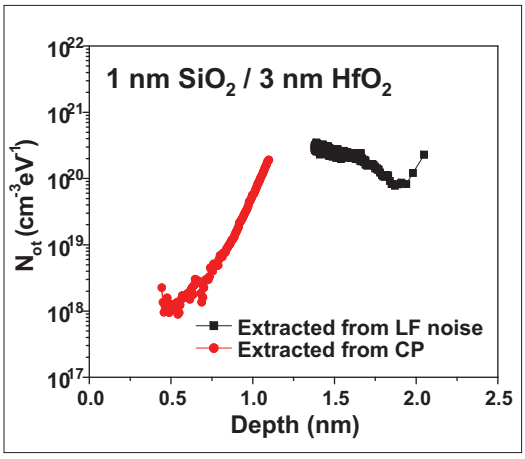

Figure 3 Extracted charge traps in the dielectric stack as a function of distance from the substrate (channel). The two measurement techniques cover completely different depth regions. Together, they almost cover the whole thickness.

Standards Committee Participation

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

Professional Committee Participation

General Chair, 2008 IEEE International Reliability Physics Symposium (JSS).

Technical Committee Vice Chair, 2008 IEEE International Reliability Physics Symposium (KPC).

Tutorial speaker, 2008 IEEE International Reliability Physics Symposium (KPC).

Technical Program Committee Chair 2008 IEEE International Electron Device Meeting (JSS).

Technical Committee, 2008 IEEE International Conference on Integrated Circuit Design & Technology (KPC).

Technical Committee, 2008 Nano Science & Technology Institute Nanotech Conference (KPC).

Chairman of Dielectric Working Group, JEDEC JC14.2 Committee on WLR (JSS).

Management Committee IEEE Integrated Reliability Workshop (JSS).

Special Member of Graduate faculty, University of Maryland (JSS).

Special Member of Graduate Faculty, Rutgers University (KPC).

Guest editor for Special Issue IEEE Tran. on Device and Materials Reliability (JSS & KPC).

Editor, IEEE Transactions on Electron Devices (JSS).

Collaborations

IBM, Alternative Gate Dielectrics.

Micron, Boise, ID, Characterization of metal gate dielectric systems.

ARL, Characterization of defects and reliability of SiC gate dielectric systems.

GE, Reliability characterization of SiC gate dielectric systems.

Intel, Characterization of high-κ/InGaAs systems.

SEMATECH Characterization of metal gate high-κ systems.

Rutgers University, Characterization of high-κ gate dielectrics.

University of Maryland, College Park, ultrathin gate oxide reliability, combinatorial analysis of advanced gate stacks.

U. Texas at Austin, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics.

U. Texas at Dallas, high-κ gate dielectric systems.

Purdue, high-k on III-V.

Recent Talks/Publications

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"Additional Insight into Device Transient Behavior from Fast-GM Measurements,"* IEEE Electron Dev. Lett., submitted.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates,*"The Fast Initial Threshold Voltage Shift: NBTI or High-Field Stress?"* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA, accepted for presentation.

H. D. Xiong, Dawei Heh, Shuo Yang, Xiaoxiao Zhu, Moshe Gurfinkel, Gennadi Bersuker, D. E. Ioannou, Curt A. Richter, Kin P. Cheung, and John S. Suehle, *"Stress-induced defect generation in HfO2/SiO2 stacks observed by using charge pumping and low frequency noise measurements,"* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA, accepted for presentation.

Curt A. Richter, Hao D. Xiong, Xiaoxiao Zhu, Wenyong Wang, Vincent M. Stanford, Qiliang Li, D. E. Ioannou, Woong-Ki Hong, and Takhee Lee, *"Measurements for the reliability and electrical characterization of semiconductor nanowires",* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA, invited paper.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates,*"Electron Trapping: An Unexpected Mechanism Of NBTI AND ITS Implications,"* 2008 VLSI Technology Symp., Hawaii, USA, accepted for presentation.

Kin P. Cheung, and John S. Suehle, *"The Challenge of Measuring Defects in Nanoscale Dielectrics,"* invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

D.H. Hill and R.A. Bartynski, N.V. Nguyen, Albert C. Davydov, and Deane Chandler-Horowitz, and Martin M. Frank, *"The relationship between local order, long range order, and sub-bandgap defects in hafnium oxide and hafnium silicate films",* Applied Physics Letters, submitted.

Oana D. Jurchescu, Behrang H. Hamadani, Hao D. Xiong, Sungkyu K. Park, Sankar Subramanian, Neil Zimmerman, John E. Anthony, Thomas N. Jackson, and David J. Gundlach, *"Correlation between microstructure, electronic properties and flicker noise in organic thin film transistors",* Appl. Phys. Lett., in press.

M. Gurfinkel, H.D. Xiong, K.P. Cheung, J. Suehle, J.B. Bernstein, Yoram Shapira, A.J. Lelis, D. Habersat, N. Goldsman, *"Characterization of transient gate oxide trapping in SiC MOSFETs using fast I-V techniques,"* IEEE Trans. Electron Dev. accepted.

Y. Wang, K. P. Cheung, R. Choi, B.-H. Lee, *"An Accurate Capacitance-Voltage Measurement Method for Highly Leaky Devices,"* IEEE Trans. Electron Dev. submitted.

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Nanoelectronic Device Metrology

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Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable new nanoelectronic information processing technologies to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. Specifically, the NEDM is developing the precise metrology and measurement methods required for the systematic characterization of emerging nanotechnologies such as Si-based nanoelectronic, single-electron devices for one-electron logic, nanowire and carbon nanotube based transistors, and molecule-based devices. This task involves determining the critical metrology needs for these exploratory technologies.

Customer Needs

Mainstream CMOS, which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is approaching fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) (http://public.itrs.net/) shows no known solutions in the short term for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. This need is so strong that a consortium of companies in the SIA has established the Nanoelectronics Research Initiative (NRI). NIST is teaming with the NRI to accelerate research in nanoelectronics.

Two promising beyond-CMOS technologies that each takes a very different fabrication approach are molecule-based devices and Si-based quantum electronic devices. Molecule-based devices are based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

Molecule-based devices is a field that many predict will have important technological impacts on the computational and communication systems of the future. In these systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (*e.g.,* Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology. Finally, there is a large potential set of customers for ultra-sensitive charge electrometry of biological systems. Many diseases result from changes in protein structure or folding. We will investigate whether such changes can be elucidated through capacitive coupling to nearby nanotransistors.

Before bulk carbon nanotubes can fulfill their promise for multifunctional (electronic, electrical, structural, thermal) composites, better methods are needed for purification, dispersion and identification of raw nanotube materials. Predicted nanotube behavior may be compromised by the presence of impurities and molecular defects. Simple, inexpensive and scalable methods are preferred for characterizing bulk material in the presence of impurities and defects. In addition, reproducible measurement results are difficult due to physical contact between the metrology instrument and the nanomaterials. We are working toward purification and dispersal by laser processing rather than wet chemistry. In addition, we continue to pursue non-contact metrology of electronic and optical properties.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Because these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

Technical Strategy

The NEDM task's technical strategy is to develop innovative measurement methods for specific emerging nanoelectronic systems spanning a range of technologies. By collaborating with NRI-sponsored researchers, NIST will be able to ensure that its programs focus on developing critical measurement tools likely to accelerate advances in this visionary, high risk area of research. Following are brief descriptions of the

NEDM's strategies for developing the critically needed measurement tools to enable successful advances in nanoelectronics.

Develop the electrical and physical metrology of Si-based nanoelectronics. The focus of this task is the basic building blocks of silicon quantum electronic devices (*e.g.,* quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined. Test structures and improved electrical test methodologies are being developed in addition to new test structures. In particular the NEDM is (1) critically assessing and improving single-electron devices based upon Si-nanowires, (2) developing advanced capacitance measurement techniques for critical small (aF-scale) capacitances in nanoelectronics devices such as nanowires and (3) applying improved noise characterization to determine technical validity of innovative nanoelectronic structures and probe-scattering dynamics.

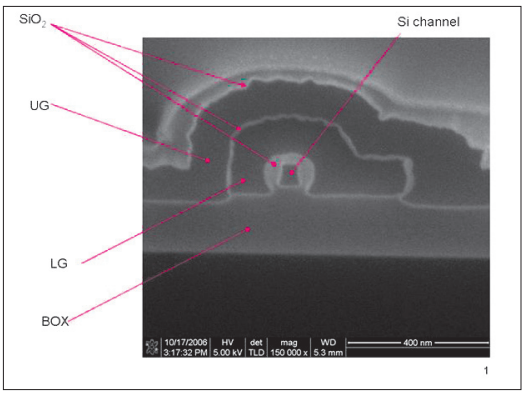

Figure 1. Cross-sectional micrograph of tunable-barrier devices fabricated by the NIST NEDM Project.

DELIVERABLES:

- Fabricate and characterize SiNW devices (such as high-performance transistors and charge trapping memory devices) incorporating high-k gate dielectrics such as HfO_X. Prepare and submit manuscript 2Q 2008.
- Optimize fabrication process for tunable-barrier Si single-electron devices. 4Q 2008
- Assess Coulomb blockade behavior versus small dimensions of tunable-barrier devices – is it possible to achieve both high-temperature operation and reliable, low noise device performance? 3Q 2008
- Apply signal processing methods to develop improved noise characterization methods for use on semiconductor nanowire devices. Prepare and submit manuscript. Prepare and submit manuscript 3Q 2008
- Fabricate a capacitance test chip, in conventional CMOS technology, that will produce small-scale capacitance and be accessible by probe station and scanning probe microscope. 3Q 2008

Determine the ultra-sensitive charge electrometry capabilities of Si-nanotransistors through measuring there sensitivity and its relationship to device structure. A longer term strategy is to assess how the sensitivity is affected by biological structures in solution.

DELIVERABLE:

- Assess proof-of-principle by detection of DNA denaturation/renaturation transition using Si nanotransistor. 3Q 2008

Develop robust molecular test structures in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models.

DELIVERABLE:

- Integrate molecular-based devices with CMOS circuitry to create an on-chip hybrid CMOS/molecular device circuit. 3Q 2008
- Experimentally test the feasibility of nanolaminated Au as a top contact for MolE devices. 4Q 2008

Determine the factors that govern the barriers to electron and/or hold injection of molecular films on solid surfaces. Determine the interface dipole and change-to-surface work function of molecular films on solid surfaces. A longer term goal is to determine the factors that influence the energy level alignment of molecular layers on semiconducting surfaces.

DELIVERABLE:

- Deconvolution of the interfacial electronic structure of monolayers chemisorbed on metals using ultraviolet photoemission spectroscopy and controlled molecular synthesis. 2Q 2008
- Determine the valence electronic structure of molecular films on selected semiconducting surfaces. 4Q 2008

To establish a quantitative characterization toolbox for practical measurements of bulk nanomaterials building upon non-contact probes recently pioneered at NIST. This toolbox will provide rapid,

quantitative methods for identifying CNT properties. Existing measurement tools are neither practical nor useful for current and future large-scale production of nanomaterials. These protocols often rely on physical contact between the test probe and the material under study. However, physical contact between probes and nanomaterials may alter the material property of interest, for example differentiating bulk resistance from contact resistance, or even the material itself. Advanced, cost effective analytical techniques are needed so that manufacturers, product developers, and regulatory agencies can truly "see" what they have. Photons, being massless and chargeless are an ideal, non-contact probe of nanoscale properties.

DELIVERABLE:

- Apply the method of resonantly coupled photoconductive (RCPCD) lifetime measurements to determine carrier dynamics of bulk carbon nanotube material. 1Q 2009
- Demonstrate $LiNbO_3$ resonator as a common platform for non-contact metrology methods of optical and electrical properties of bulk CNTs. 4Q 2008
- Develop laser processing methods for purifying CNTs. Document importance of pulsed UV laser treatment over UV lamp exposure. Document the role of ambient atmosphere in photo-physical purification processes; for example, oxygen, nitrogen, vacuum or ozone. 4Q 2008
- Demonstrate theoretical role of π-plasmons in 248 nm laser processing by density functional theory calculations. Document binding energies with respect to impurities and defects on CNTs. See Figure. 4Q2008

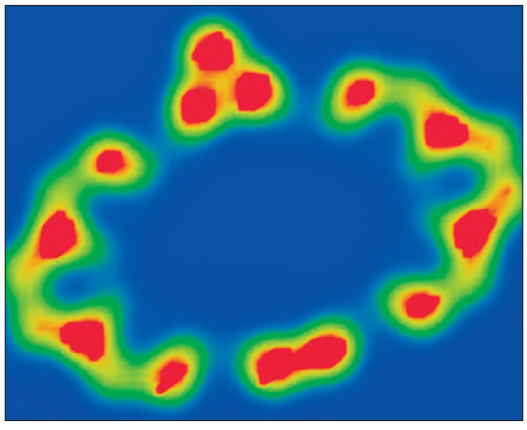

Figure 2. An oblique section of a carbon nanotube with a covalent cyclopropane modeled by density functional theory. The modeling provides a mean to examine predicted binding energies in the presence of impurities and defects. Optical probes such as our 248 nm excimer laser are a mean to examine the theory by experimental methods.

Accomplishments

■ *NIST Team Proves Bridge from Conventional to Molecular Electronics Possible* Molecular electronic devices (see Figure 3.) were fabricated by using silicon of the same crystalline orientation as that used in standard microelectronics (CMOS) technology, Si (100). This breakthrough demonstrated that a single layer of organic molecules can be assembled on the same sort of substrate used in conventional microchips. The ability to use a silicon crystal substrate that is compatible with the industry-standard CMOS (complementary metal oxide semiconductor) manufacturing technology paves the way for hybrid CMOS-molecular device circuitry — necessary precursor to a "beyond CMOS" totally molecular technology — to be fabricated in the near future.

Because the probable first step in the realization of molecular electronic devices will involve their integration with existing CMOS technology, it is imperative that molecular devices be fabricated using CMOS compatible materials, such as 100-oriented silicon. It was demonstrated that organic monolayers can be assembled on Si (100) that are comparable in quality, aliphatic monolayer coverage, and extent of substrate oxidation to those assembled on the more extensively studied, but CMOS-incompatible, Si (111) crystal face. Monolayers assembled on the CMOS-compatible Si (100) were characterized via spectroscopic monolayer characterization, as well as through the fabrication of Si (100)-based molecular electronic devices that exhibited molecule-dependent electrical characteristics.

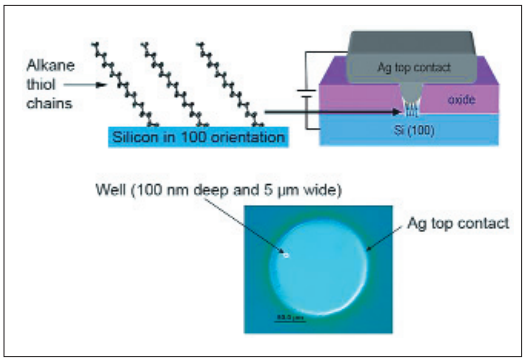

Figure 3. Molecular Integration with Si(100): Side and top views of a Si(100) molecular test structure. Above are schematics showing a cross-section of the full device and a close-up view of the molecular monolayer attached to the CMOS-compatible silicon substrate. Below is a photomicrograph looking down on an assembled device indicating the location of the well.

■ *IETS Used to Probe Molecular Layers of Metal-Molecule-Silicon Devices* In collaboration with researchers from Purdue, we demonstrated for the first time the use of IETS to probe transport properties of molecular layers in integrated metal-molecule-silicon (MMS) devices with molecules assembled directly to silicon contacts. The results provide direct experimental confirmation that the chemical integrity of the monolayer is preserved and that the molecules play a direct role in electronic conduction through the devices.

Molecular electronics has drawn significant attention for nanoelectronic and sensing applications. A hybrid technology where molecular devices are integrated with traditional semiconductor microelectronics is a particularly promising approach for these applications. Key challenges in this area include developing devices in which the molecular integrity is preserved, developing in situ characterization techniques to probe the molecules within the completed devices, and determining the physical processes that influence carrier transport. Traditional techniques for analyzing monolayer quality on silicon substrates such as Xray photoelectron spectroscopy (XPS) and scanning probe techniques are surface-specific. Certain spectroscopic measurements of buried molecular layers can be performed, but they require device areas on the order of mm^2, which are unsuitable for integrated metal-molecule semiconductor (MMS) devices in the micro- or nano-scale. The recent advance by EEEL-Purdue researchers has utilized the IETS technique for the first time to examine the transport in solid-state MMS devices with dimensions in the micro scale. Their experimental results not only successfully confirmed the organic species incorporated in the samples, but also revealed certain effects from the silicon electrode, presenting valuable information on the physics influencing carrier transport in these molecule/Si hybrid structures. The NIST study has established IETS as a critical nondestructive experimental method for the investigation of integrated semiconductor devices with active organic components and will assist in the development of future feasible silicon–based molecular electronic devices.

■ *Lack of charge offset drift in tunable-barrier Si single-electron devices demonstrated.* We have demonstrated that the recently tested tunable-barrier single-electron devices (fabricated at NTT in Japan) exhibit the same advantage as the previously measured fixed barrier ones: there is no time-dependent drift in the operating characteristics of these devices, in contrast to metal-based single-electron devices. This demonstration allows us to continue working with the tunable-barrier devices, which have both advantages of superior flexibility and stability in time.

■ *Robustness of lack of charge offset drift in Si single-electron (SE) devices demonstrated.* By fabricating Si-based SE devices at a second foundry (Cornell University in USA), and by showing a lack of charge offset drift in these devices as well, we have demonstrated that the lack of drift is a robust property of the Si device system, as opposed to being due to the processes in a particular foundry. This robustness adds to our expectations that these devices are amenable to integration.

■ *Spin-polarized Inelastic Electron Tunneling Spectroscopy of a Molecular Spintronic Device Investigated by EEEL Researchers*. Researchers at NIST have fabricated and characterized molecular-monolayer magnetic tunnel devices. Molecular spintronic systems were fabricated by sandwiching a self-assembled monolayer of octanethiol between two ferromagnetic electrodes in a nanopore (Fig. 1), demonstrating that single molecules can be used as the ultimate building blocks for spintronic devices. By using inelastic electron tunneling spectroscopy (IETS), Wenyong Wang and Curt Richter have obtained the first unambiguous experimental evidence of the existence of molecular species in such magnetic tunnel junctions. Tunneling spectroscopy was also utilized to investigate the spin-polarized inelastic electron tunneling processes in the molecular devices. The measurements revealed that inelastic scattering due to molecular vibrations is likely the main cause of an observed junction magnetoresistance bias-dependence. These results illustrate that such inelastic scattering events must be accounted for when predicting the performance of practical molecular spintronic devices. Molecular electronic devices with spin-dependent tunneling transport behavior offer an innovative and extremely enticing direction towards spin electronics, from both fundamental and technological points of view. Due to the weak spin-orbital and hyperfine interactions in molecules, the spin coherence over time and distance could be preserved much longer in molecular nanosystems than in traditional

semiconductors, which makes them a suitable playground for spin manipulations.

■ *Investigation of new "barrier" capacitance.* In the tunable-barrier devices, the barriers are produced electrostatically by small "finger" gates; these electrostatically-defined barriers, which are a few tens of nm in size, have not been previously investigated. As a first step in developing the metrology of characterizing such small barriers, we have shown that through Coulomb blockade measurements, it is possible to measure the "barrier" capacitance across these quantum tunneling regions. These capacitances (Fig. 5) range in value down to just a few aF, and such a measurement is only possible with Coulomb blockade studies. We are beginning a collaboration in order to compare our results with simulations; our hope is that this metrology study will allow validation of the simulation models.

■ *Nano-gap capacitors.* We have investigated the standard theory for the breakdown at small separations (below about 5 μm). In this regime, the standard theory uses Fowler-Nordheim tunneling in vacuum, along with a surface roughness-induced field enhancement; this field enhancement is typically a factor of about 100. By combining electrical breakdown measurements with AFM measurements of surface roughness, we have for the first time been able to quantitatively test this theory. We find that the roughness in our smooth Au films is much smaller than necessary for the standard theory to be correct. We conclude that the standard theory cannot explain our experiments, and by extension is suspect in most of the measurements done to date.

■ *Laser induced purification of single wall carbon nanotubes (SWCNTs).* We have further investigated the purification of as-prepared single-walled carbon nanotubes (SWCNTs) by exposure to ultra-violet (UV) light of various wavelengths in different atmospheres. Our initial work demonstrated the excitation of the collective electron oscillations of the π-plasmon in the nanotubes by the 248 nm photons results in non-thermal removal of carbon impurities. Our recent results from 193 nm pulsed laser light and 254 nm continuous wave (CW) light supports the importance of resonance of photon energy with the π plasmon of sp^2 bonded carbon atoms, as well as demonstrates the importance of atmosphere, and the pulsed nature of the light. Analysis of Raman spectroscopy data has shown that the carbon impurities are more efficiently removed by the pulsed light for the same number of photons than by the CW light for roughly the same wavelength. We continue to investigate the photothermal, photophysical, and photochemical influences for the mechanism of purification of SWCNTs. We have considered differences in the thermal transport, including thermal conductivity, specific heat and thermal diffusivity of carbon nanotube compared with the thermal transport properties of impurity carbons. We have found that upon pulsed heating the nanotubes experience a smaller temperature increase than do the other carbons impurities, and this difference enables the selective oxidation of the impurities carbons. The importance of the resonance of the π-plasmon of sp^2 carbon with the incident photons has also been a large focus of our work. The production of hot electrons and the simultaneous decrease in electron density as electrons are excited into an antibonding state of the carbon sp^2 bond is also considered. We continue to work closely with our theoretical collaborators at the Colorado School of Mines in order to provide a theoretical understanding to our experimental findings.

■ *Rapid and inexpensive identification of bulk carbon nanotubes.* The photoconductive recombination lifetimes of CNT thin films as a function of wavelength were measured by resonant-coupled photoconductive decay (RCPCD) method. The carrier recombination lifetime is a fundamental property of carbon nanotubes which is typically determined by contact-based techniques or spectroscopic methods. The RCPCD measurement is based on a pump-probe technique in which an optical pump and a low frequency microwave probe are employed and is well suited to characterization of bulk and extrinsic material properties. Our results demonstrate the role of purification and the effect of the interaction of nanotubes and polymers in thin films of multi-walled carbon nanotube and single-walled carbon nanotubes. Possible mechanisms describing the interaction of photoexcited carriers in the nanotube polymer composites are currently under investigation. We have reported the wavelength dependence of photoconductive lifetimes at meetings of the American Vacuum Society and the Materials Research Society. Raman spectroscopy and UV-VIS absorption measurements provide further identification and characterization of nanotube samples to enable correlation of nan-

otube properties with the efficiency of charge transport.

A dielectric resonator-based measurement method for determining the electrical conductivity of carbon nanotubes at microwave to millimeter frequencies has been demonstrated. This measurement method is not limited by the metal conductor contact resistances or impedance mismatch commonly encountered in the measurement of single nanotubes. The measurement of carbon nanotubes yielded conductivities of approximately 0.08×10^7 S/m.

■ *Valence level alignment and identification of the charge carriers of molecules on metal surfaces.* We have systematically studied the valence level alignment for two bonding chemistries as a function of metal work function. Using ultraviolet photoemission spectroscopy we measured the energies of the highest occupied delocalized state for three thiol-linked molecules on Ag, Cu, Au, and Pt, which span a work function range of over 1 eV. These results showed that alignment of the occupied electronic structure is independent of the metal work function, but is dependent on the electronic structure of the molecule. We also observed a linear dependence on the change of the metal work function, where the higher work function metals exhibited a larger work function change. Taken together these data suggest that the molecule plays a larger role than the contact material in molecule-based devices. For the second bonding scheme we used isocyanide chemistry. Here we observed a shift of the occupied valence structure to deeper (higher) binding energies compared to those observed with thiol that is independent of the metal work function. This shift suggests that the charge carrier (holes vs. electrons) can be controlled using molecule-metal bonding chemistry. To test this we assembled molecules in crossed-wired molecular junctions on Ag, Au, and Pt and observed that the transition from direct tunneling to field emission is correlated with the unoccupied valence states in isocyanide-bound monolayers. In other words, the charge carriers are electrons for isocyanide-linked films; whereas, the carriers are holes in thiol-bound monolayers. These data show that photoemission spectroscopies can be utilized for prediction of some transport properties.

■ *Validating the unoccupied valence electronic structure of molecules on metals.* The metal-molecule interface is key to understanding and controlling charge transport in nanoscale junctions. Here, the occupied and unoccupied valence electronic structure of a chemisorbed molecular layer on metals was measured using a combination of ultraviolet photoemission, two-photon photoemission (2PPE), and inverse photoemission (IPE) spectroscopies. By using both 2PPE and IPE the ionization processes between the two complimentary techniques was able to be determined. We observe that 2PEE and IPE give a very nuanced picture of the unoccupied electronic structure of the interfacial region. The excitation mechanism of each technique must be properly understood in order to reliably predict the unoccupied states involved in charge transport. Using both techniques we were able to assign and calculate the unoccupied electronic structure, and detail the electronic processes that arise in each measurement.

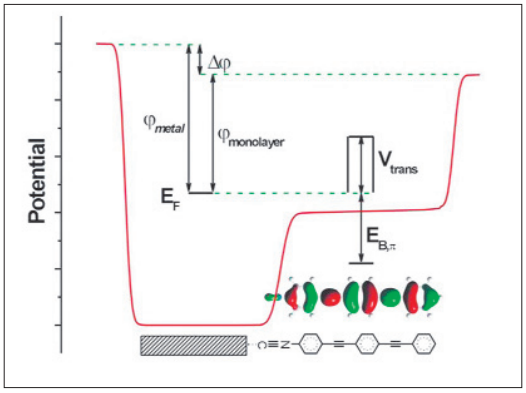

Figure 4. Schematic of electrostatic potential of a molecular chemisorbed on a metal surface.

■ *System Developed to Precisely Align Single Nanowires.* A system has been devised for manipulating and precisely positioning individual nanowires on semiconductor wafers. This technique, allows the fabrication of sophisticated test structures to explore the properties of nanowires, by using only optical microscopy and conventional photolithographic processing in lieu of advanced (and expensive) tools such as focused ion or electron beams. The smallest-diameter nanowires today are built in a "bottom-up" fashion, assembled atom-by-atom through a chemical growth process such as chemical vapor deposition. This is essentially a bulk process; it produces haystacks of jumbled nanowires of varying lengths and diameters. To control the positioning of nanowires, NIST engineers modified a standard probe station used to test individual com-

ponents in microelectronic circuits. The station includes a high-resolution optical microscope and a system for precisely positioning work surfaces under a pair of customized titanium probes with tips less than 100 nanometers in diameter. In a two-step process, silicon nanowires suspended in a drop of water are deposited on a special staging wafer patterned with a grid of tiny posts, and dried. Resting on the tops of the posts, selected nanowires can be picked up by the two probe tips, which they cling to by static electricity. The test structure wafer is positioned under the probes, the nanowire is oriented by moving either the probe tips or the wafer, and then placed on the wafer in the desired position. The technique's fine level of control allows the precise placement of single nanowires to create elaborate structures for testing nanowire properties. This capability has been demonstrated by building a multiple-electrical-contact test structure for measuring the resistance of a nanowire independent of contact resistance, and a simple electromechanical "switch" suitable for measuring the flexibility of nanowires.

■ *Interfaces in Molecular-Monolayer/SiO2 Based Molecular Junctions Characterized.* The results of dc-current-voltage (IV) and ac-capacitance-voltage (CV) measurements have been correlated with optical vibrational spectroscopy of Au/monolayer/SiO2/Si structures to establish an improved understanding of the interactions at the buried metal/monolayer and dielectric/silicon interfaces. Towards the goal of observing and characterizing electrical device behavior based upon intrinsic molecular effects, the role of test structures and their interfaces must be understood and eventually effectively controlled. A novel backside-incidence Fourier-transform infrared-spectroscopy technique previously developed by members of the NIST research team was used to characterize buried metal/molecule interface to probe the interaction of the top-metallization with the organic monolayers. Both the spectroscopic and electrical results indicate that Au has a minimal interaction with alkane monolayers deposited on SiO2 via silane chemistry. An intriguing negative-differential-resistance and hysteresis is observed in the IV measurements of Au/alkane/SiO^2/Si devices. It is unlikely that this behavior is intrinsic to the simple alkane monolayers in these structures. Based on the results of extensive electrical characterization, the observed IV features are attributed to charge trapping and detrapping at both the alkane/SiO^2 and the Si/SiO^2 interfaces. These data illustrate that the dielectrics and other materials used when fabricating molecular devices must be made at the highest level of control to avoid impurities and defects which are likely to lead to spurious device behavior.

■ *Two-dimensional Electrostatics to Enhance Channel Modulation in Dual-gated Silicon Nanowire Devices.* We have experimentally observed enhanced channel modulation in dual-gated silicon nanowire (SiNW) field-effect transistors (FETs). In this work, SiNW FETs were fabricated using electron-beam lithography to investigate the electrostatic control of current in semiconductor nanowire devices. These novel top- and bottom-gated FETs are based upon simple top-down test structures that rely upon self-aligned Schottky-contacts to enable the electronic properties of SiNWs to be readily studied. Improved device performance is observed for the dual-gated SiNW FETs when compared to simultaneously fabricated large area control FETs. The SiNW devices (with widths down to approximately 60 nm) exhibit an on/off current ratio greater than 106, which is more than three orders of magnitude higher than that of control devices prepared simultaneously having a large channel width (5 μm). In addition, the top gate is found to suppress ambipolar conduction effectively, which is one of the factors limiting the use of nanotube or nanowire FETs for complimentary logic applications. Two-dimensional numerical simulations have confirmed an important physical insight illustrated by this work: due to the reduced dimensionality of SiNWs, electrostatic control is enhanced when compared to larger channel width devices.

■ *Comparison of charge offset drift in metal-based and Si-based single electron transistors (SET)* . We have completed a study comparing the charge offset drift in metal-based and Si-based SET transistors. To date, there has been no reproducible way to eliminate the charge offset drift in metal-based SET devices, while Si-based devices have been characterized that exhibited minimal charge offset drift. The long-term charge offset behavior appears to be correlated with an observation in the short-term noise: two-level fluctuators in the Si-based devices are completely stable with respect to time, thermal cycling, etc.; in contrast, two-level fluctuators in the metal-based devices are notori-

ously "fragile." We have devised a model that comprehensively explains these results: in the metal-based devices, the defects that produce the drift are interacting strongly, as if they are in a glassy environment. These interactions are the underlying source of the long-term drift, and of the lack of stability in individual two-level fluctuators. This analysis leads us to suggest that a new fabrication process in which the metal films are deposited with low stress will improve the performance of the metal-based devices.

■ *Novel approach to investigate buried metal-organic interfaces for molecule-based devices.* We have developed and used a novel approach to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique developed at NIST takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of a technologically relevant metal electrode. The samples as prepared encapsulate the organic layer in exactly the same manner as fully fabricated devices. IR and electrical samples were fabricated simultaneously, allowing direct comparison of the spectroscopic results with electrical device performance. Two different chemical processes were utilized to attach nm-thick alkane films to the Si substrates: a conventional silanization process for films on thin oxides and a novel process previously optimized at NIST for direct attachment to silicon. Molecules on silicon are of interest as active electronic layers and for surface engineering. Monolayers bound directly to silicon are expected to have less interfacial capacitance than those on oxides, be more amenable to further processing, and be resistant to degradation die to the nature of the strong covalent bond. Results were presented at the 7th International Molecular Electronics conference and published.

■ *New reactor for growing doped Si, Ge, and SiGe nanowire heterostructures.* A. Davydov and S. Krylyuk have designed a versatile CVD system for fabricating Si and SiGe alloy thin-films and nanostructures. The system includes hot-wall horizontal reactor with 4 independently controlled temperature zones and automated gas delivery system. The reactor is designed to be capable of growing Si and SiGe alloys on round or square 1" substrates at atmospheric or reduced (down to 1.3 Pascals (10 mtorr)) pressure. The system design utilizes SiH4 gas as a Si source, solid Ge or germanium halides as Ge-sources and solid sources for p (boron-based) and n-type (phosphorus based) doping. To achieve rapid growth process interruption/restoration without exposing system to the outside atmosphere (*e.g.,* for realization of abrupt interfaces in fabricated heterostructures, such as p/n junctions in Si, Ge, and SiGe multi-layers), the reactor design includes adjacent "preservation zone" to be maintained at the growth temperature and pressure in inert atmosphere. All parts of the system have been manufactured and/or purchased and the assembly of the system is in progress. The system is planned to be operational for growing Si nanowires and thin films in 4Q of 2007. Capabilities for growing Ge and SiGe using GeH4 gas as well as utilizing gaseous sources for n- and p-doping can be added as necessary in FY 2008 (funding permitted). The new CVD system will enhance the NEDM's capability of fabricating Si and SiGe nanostructures with desired structural and electronic properties for nano-metrology needs.

COLLABORATIONS

Colorado School of Mines, Prof. Mark Lusk, Ab initio studies of pi plasmon role in bundling, functionalization and optical properties of carbon nanotubes.

Colorado School of Mines, Richard Ahrenkiel, Resonantly coupled photoconductive decay lifetime measurements of CNTs and CNT-polymer composites.

George Mason University, Prof. Qiliang Li, Novel nanowire devices and test structures.

Gwangju Institute of Science and Technology, Korea, Prof. Takhee Lee, Scattering processes in ZnO nanowire.

Hewlett-Packard, R. Stanley Williams et al., Interface properties of molecular electronic test structures.

NTT, Akira Fujiwara, Si-nanowire metrology.

National Renewable Energy Laboratory, A. C. Dillon, Optical properties of CNT materials.

NIST Division 817, Dean Jarrett, Electrostatic biosensing.

NIST Division 838, Dr. James Kushmerick, Molecular charge transport.

Princeton University, Prof. Antoine Kahn, Validating the unoccupied valence electronic structure of molecules on metals.

Purdue University, Prof. David Janes, Hybrid Si-molecular devices and test structures.

Rice University, Prof. James Tour, Valence level alignment and identification of the charge carriers of molecules on metal surfaces.

University of Maryland, Prof. Ellen Williams.

University of Notre Dame, Prof. Greg Snider, Si single-electron device fabrication.

University of Texas, Prof. Eric Vogel, Si nanowire field effect transistors.

Virginia Polytechnic Institute and State University, R. L. Mahajan, laser treatments of CNT materials.

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures.

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Power Semiconductor Device Metrology

Technical Contacts:
A. Hefner

Goals

The goal of the project is to develop electrical and thermal measurement methods, measurement equipment, and theoretical models in support of the development and application of advanced power semiconductor devices.

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient power generation, transmission and distribution. Rapid technical advances are occurring in the development of new power semiconductor materials, fabrication processes, and device designs to address these needs. With the introduction of these new materials and designs come new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC material and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the commercialization of SiC power Schottky diode products in the 400 V to 1200 V range and to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize industry and military power generation, transmission, and distribution by extending the use of switch-mode power conversion technology, with its superior efficiency and control capability, to high voltage applications.

"In 2002, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: "his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in ... more efficient/compact power supplies, and higher efficiency power distribution/transmission systems."

Several industry and government programs are currently under way to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is to develop half-bridge power semiconductor modules with 15 kV, 110 A, 20 kHz switching capability. The recently awarded WBST-HPE Phase 3 effort (http://www.darpa.mil/baa/baa06-30.html) anticipates that this semiconductor technology will enable the HV-HF switching required for a Solid State Power Substation (SSPS). The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements, and the Department of Energy has identified HV-HF power devices as an enabling technology for alternative energy sources and energy storage systems, as well as transmission and distribution systems.

Technical Strategy

The strategy of the NIST project is to support the measurement infrastructure of the power semiconductor and energy systems technology industries by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of power semiconductor devices. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters. The NIST project also establishes the theoretical foundation required for development of advanced power semiconductor devices, and develops circuit simulation models for emerging power semiconductor devices to aid in the rapid adoption and effective utilization of new technologies. NIST is taking a lead role in developing the device metrology and performance metrics necessary for industry and

government HV-HF semiconductor device development efforts and in the evaluation of potential future impacts power semiconductor technologies requiring future investment.

Metrology High-Voltage High-Frequency Switching Devices

The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements. NIST has recently developed unique world-class laboratory facilities for characterization of HV-HF SiC power switching devices including: a) 25 kV variable-pulse-width curve tracer, b) 15 kV 100 A 50 ns inductive and resistive load switching tester, c) 4 kV, 50 A, 10 ns diode reverse recovery tester, d) pulsed and multi-channel long term diode forward current stress and monitoring systems, e) high-speed high-power Temperature Sensitive Parameter module package measurement system, and f) rapid thermal cycling/shock module package stress system.

Support Programs to Develop HV-HF Semiconductor Devices and Applications

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable SSPS for future Navy warships. Conventional distribution approaches being considered for the next generation of aircraft carriers employ a 13.8 kV a.c. power distribution that is stepped down to 465 V a.c. by using large (6 ton and 10 m^3) 2.7 MW transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phase 2 and 3 programs for 2005 through 2009. A new NIST/DOE program was recently established to analyze advanced power electronic component technologies needed for 300 MW Power Conversion Systems (PCS) to enable future Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas. The extremely large PCS is required to convert the 700 V, 1000 A DC power output of one thousand fuel cell modules to the 345 kV AC power transmission level.

DELIVERABLES:

- Participate in coordinating the effective utilization of DARPA HPE Phase 2 devices in the SSPS power converter developed by the HPE Phase 3 contractor team. 2Q 2009
- Perform analysis to identify advanced high-megawatt PCS technologies requiring investment to meet the goals of the DOE Solid State Energy Conversion Alliance (SECA) and FutureGen programs for near-zero emission central station fuel cell power plants. 4Q 2008
- Provide leadership in Chairing an Interagency Task Force and in establishing an industry roadmap for High Megawatt Power Converters. 2Q 2008

Characterize Electrical Performance of DARPA HPE Device Deliverables

NIST continues to serve as the exclusive device deliverable evaluation lab for the DARPA WBST HPE Phase 2 program providing data and analysis critically important to evaluate contractors and plan future programs. NIST evaluates device performance and provides feedback to contractor and DARPA program manager as well as the potential component users in government and industry. The NIST characterization data and analysis has continually identified critical technology advancements required to meet DARPA program goals such as recommendations to improve surface passivation, reducing internal gate resistance, improving *p-i-n* power diode (diode made with p-type to intrinsic to n-type semiconductor junctions) speed, transitioning program goal from *p-i-n* to Schottky diodes, and specific design parameter targets for MOSFET and IGBT (insulated gate bipolar transistor) designs. The NIST HV-HF characterization results are routinely used in by DARPA in planning documents and by the device developers in publications.

DELIVERABLES:

- Apply NIST HV-HF power device test systems to evaluate the performance of the 10 kV, 100 A, 50 ns half-bridge power modules produced by the DARPA WBST-HPE program and asses the potential for enabling advanced commercial and military power generation, transmission, and distribution systems. 2Q 2008

SiC Power Device Models for HV-HF Power Converter Simulation

Accurate and robust circuit simulator models for HV-HF semiconductor devices are needed

to evaluate the impact of the new semiconductor technology on power converter system performance. NIST develops the generic physics-based models for the SiC power semiconductor devices that are provided in commercial circuit and system simulation software. In addition, NIST also develops model parameter extraction methods needed to measure the physical and structural parameters of specific devices. The NIST model parameter extraction tools have recently been used to characterize SiC power MOSFETs and diodes introduced by the DARPA WBST-HPE Phase 2 program. These models were used as a virtual prototype to perform simulations of a 2.7 MW SSPS by the DARPA/ONR/Navsea WBST HPE Government Independent Panel providing the basis for the HPE Phase 3 Broad Area Announcement. The models are also to be used as part of the NIST/DOE advanced PCS technology evaluation and for use in the plug-in hybrid-electric and electric vehicle power train.

DELIVERABLES:

- Develop and apply models of advanced component technologies for high megawatt power conversion systems to determine technologies requiring substantial federal investment to meet the DOE SECA and FutureGen program goals for central station fuel cell power plant PCS requirements.4Q 2008
- Develop electro-thermal module model for ultra-high efficient inverter module to be used in hybrid vehicle soft switching inverter and perform parameter extraction and model validation for the devices and package elements of the modules. 1Q2009

Metrology for SiC Device Degradation and Reliability

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for devices with minority carrier injection is the degradation in the electrical characteristics after prolonged forward bias conduction. The degradation occurs from latent material defects such as Basal Plane Dislocations (BPDs) that result in the formation and growth of stacking faults activated by excess-carrier recombination. NIST has recently developed automated stress and degradation monitoring systems to assess degradation of SiC devices. The monitoring methods include forward conduction voltage drop, switching reverse recovery characteristics, and pulsed thermal imaging of current uniformity.

DELIVERABLES:

- Identify and document performance and reliability qualification specifications for SiC power semiconductor devices and evaluate status of SiC devices being developed for AFRL, ARL and DARPA/ONR programs. 4Q2008

Accomplishments

■ *NIST played a key role in planning and coordinating activities of the DARPA HPE program on high voltage SiC power devices including:* Evaluated contractor performance for DARPA WBST HPE Phase 2. Participated in planning and writing Broad Area Announcement (BAA) for DARPA WBST HPE Phase-3 programs and presented status of SiC power devices at the Phase 3 Industry Bidder Briefing day. Also presented the status of the DARPA HPE program at GomacTech in 2005, 2006, 2007, and 2008 and presented the status of HV-HF semiconductor devices at the IEEE Industry Applications Society Meeting (this paper received the 2006 William M. Portnoy Award). Served as Member of DARPA/ONR Solid State Power Substation (SSPS) Government Independent Design Panel. Participated in planning ONR Mantech SiC Power Device manufacturability program.

■ *NIST leading industry and other Federal Agencies in coordinating activities in High Megawatt Power Conversion Systems.* Planned and held the first High Megawatt Converter workshop at NIST with participants from major government and industry programs requiring advanced power converter technologies for high megawatt power conversion systems. Hefner (NIST) appointed as the Chairman of the Interagency Task Force for High Megawatt Power Conversion systems. Served as panel member for DOE Program on SiC-based Inverters in Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas. NIST played a key role in reinitiating the of Interagency Advanced Power Group (IAPG) Electrical Systems Working Group (ESWG) to coordinate federal programs in high-megawatt PCS technology (meeting held at NIST on April 21-25, 2008). NIST also held a High-Megawatt Power Converter Technology R&D Roadmap Workshop on April 8, 2008, to provide guidance in developing the PCS technology for grid connectivity of Alternate/Clean Energy sources and associated grid converters for distributed generation.

■ *High voltage clamped inductive and resistive switching test bed developed.* A low parasitic inductance 15 kV switching test system for clamped inductive and resistive SiC MOSFET switching characterization was developed and integrated into the 25 kV safety-interlocked curve-tracer system. A low parasitic capacitance temperature-controlled test fixture with 20 kV voltage isolation and 350 °C maximum controllable temperature was also included to enable investigation of HV-HF device characteristics at elevated operating temperature. The hardware is controlled by the NIST virtual curve-tracer instrumentation software.

■ *NIST unique HV-HF device metrology demonstrated unprecedented performance of DARPA WBST-HPE:* The NIST high voltage curve tracer and the NIST high-voltage high-frequency (HVHF) switching test systems were used to demonstrate the unprecedented performance of DARPA WBST-HPE MOSFETs, *e.g.*, 10 kV, 12 A, 50 ns inductive load switching shown in Fig. 1. Typical high voltage silicon devices require several microseconds to switch at 6.5 kV maximum. Significant advances in materials, device design and HV-HF metrology were required for this achievement.

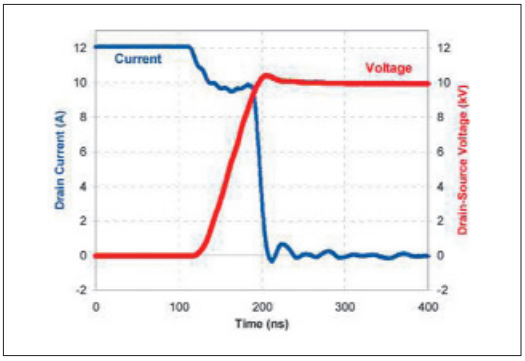

Figure 1. NIST measurement of the unprecedented performance of the SiC power MOSFETs switching at 10 kV, 12 A and 200 °C in less than 75 ns.

■ *NIST contributed to device design required to improve 10 kV SiC rectifier reverse recovery speed:* NIST provided guidance on techniques for improving the reverse recovery time (switching speed) of 10 kV SiC rectifiers developed by the HPE program. The guidance included structure changes to control the plasma distribution during reverse recovery in PiN diodes as well as the recommendation that the program be refocused toward Junction Barrier Schottky (JBS) diodes. NIST characterized the reverse recovery performance of the various

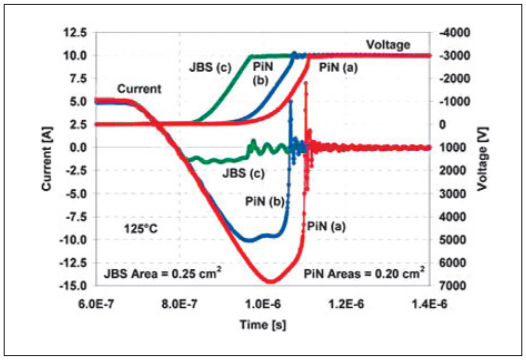

Figure 2. Comparison of reverse recovery time for two different 10 kV SiC PiN diodes, (a) and (b), and a 10 kV JBS SiC diode (c), all at 125 °C.

diode designs that were produced using the NIST 4 kV, 50 A, 10 ns diode reverse recovery tester. Results indicate that the reverse recovery charge (area under the negative portion of the current waveform shown in Fig. 2 is reduced using plasma engineering but only the JBS diode is capable of 20 kHz operation.

■ *NIST HV-HF SiC models were used to simulate system performance:* NIST's metrology, device modeling, and parameter extraction tools have resulted in software models for the HV-HF devices that are being produced by the DARPA WBST HPE program. These models are being used by industry and government to simulate the performance of future power distribution and conversion systems enabled by the new HV-HF semiconductor device technology. Fig. 3, Fig. 4, and Fig. 5 show the comparison of the model with measured results. These models were used to optimize the 100 A, 10 kV half bridge power mod-

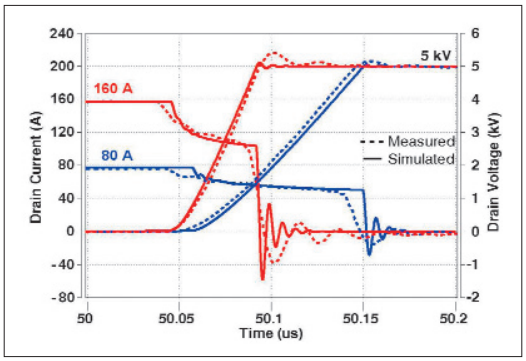

Figure 3. Comparison of scaled measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms for a 100 A, 10 kV SiC MOSFET. Both tests were performed at 25 °C with a clamp voltage of 5 kV and drain currents of 80 A (blue) and 160 A (red), respectively

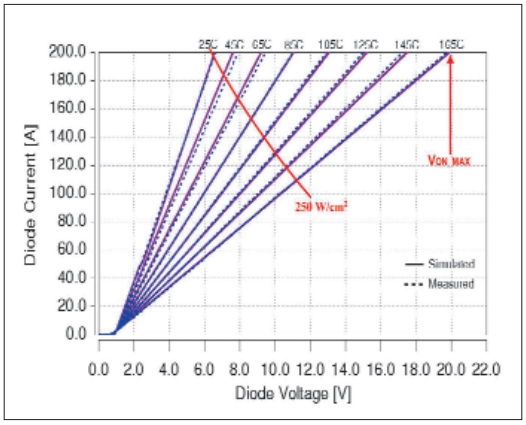

Figure 4. Comparison of scaled measured (dashed) and simulated (solid) forward conduction characteristics at 25 °C, 45 °C, 65 °C, 85 °C, 105 °C, 125 °C, 145°C, and 165 °C for a 100 A, 10 kV SiC junction barrier Schottky (JBS) diode.

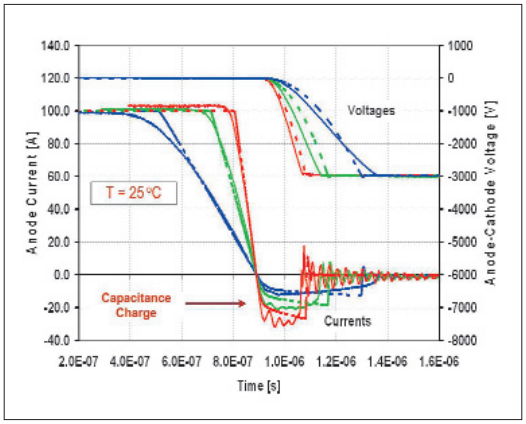

Figure 5. Comparison of scaled measured (solid) and simulated (dashed) reverse recovery at 25 °C for a 100 A, 10 kV SiC JBS diode.

ule and to design the SSPS HPE Phase 3 and are being used to simulate various PCS architectures to help identify technologies that need to be developed to reduce the cost of future PCS systems for alternate/clean energy systems.

■ *Extended capabilities of IMPACT parameter extraction software.* The capabilities of the parameter extraction software, IMPACT, were extended to include MOSFETS (in addition to IGBTs) and three prototypes of SiC material (in addition to Si). The parameter extraction hardware was also extended to enable capacitance versus gate- and drain-voltage characterization up to 5 kV.

■ *Demonstrated a HV-HF isolated gate drive circuit for 10 kV, 100 A SiC MOSFET/JBS power modules for the first time.* The new high-voltage

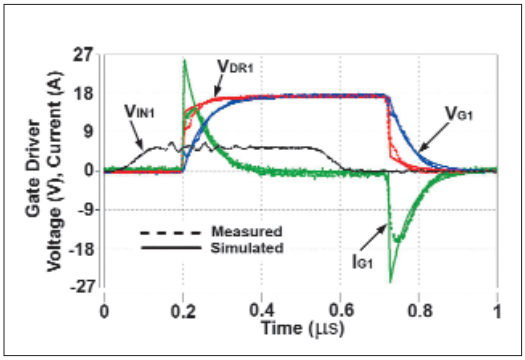

Figure 6. Gate driver current and voltage simulated (solid) and measured (dashed) waveforms.

isolated gate drive circuit for characterization of high-voltage, high-frequency 10kV, 100A SiC MOSFET/JBS half-bridge power modules to be used in the SSPS has been developed. This new gate driver has many features that include 30 kV voltage-isolation required for use as a high-side MOSFET driver in a 13.8 kV AC stacked converter configuration. The gate drive circuit enables gate resistance of less than 0.5 Ω required to achieve 100 ns switching for the modules as shown in Fig. 6. The gate drive circuit has less than 5 pF common mode capacitance enabling it to be used as a high side gate driver for a 5 kV in 50 ns switch without excessive common mode current (conducted EMI).

■ *Characterized static and dynamic performance of the first 50 A, 10 kV SiC MOSFET/JBS power module ever made.* Fig. 7 shows the measured 10 kV, 50 A SiC MOSFET output characteristics at 25 °C, and Fig. 8 shows the inductive-load switching turn-off waveforms for the 10 kV, 50 A SiC MOSFET in the power module.

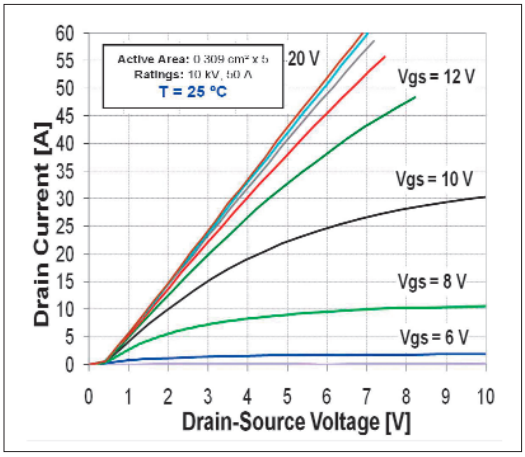

Figure 7. Measured output characteristics at 25 °C for a 10 kV, 50 A SiC MOSFET

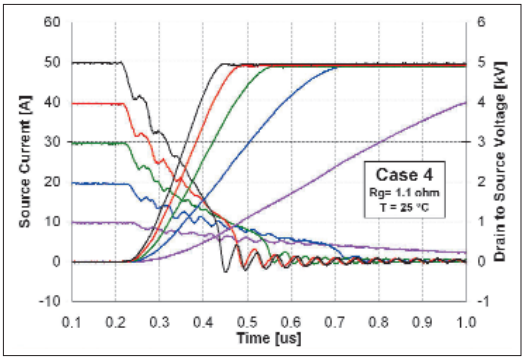

Figure 8. Measured inductive-load switching turn-off switching waveforms at 25 °C for a 10 kV, 50 A SiC MOSFET.

■ *Developed physics-based, transient, electro-thermal simulation capability for high-voltage, high-current SiC bipolar power devices.* A Physics-based TCAD simulations capability has been developed by NIST for high-voltage, high-current SiC power semiconductor devices. This capability has been applied to the electro-thermal study of SiC power thyristors operating under high-current, pulsed-power conditions as shown in Fig. 9. The use of electro-thermal, physics-based device and circuit modeling is fundamental in the study of the operating limits of SiC power devices.

Collaborations

Synopsys Inc., SiC power device modeling and parameter extraction for IGBT library component models.

CREE, Characterization and application of SiC power devices.

Northrop Grumman Corp., Characterization and application of SiC power devices.

Virginia Tech., Silicon and SiC power device utilization.

Powerex, Power semiconductor device packaging.

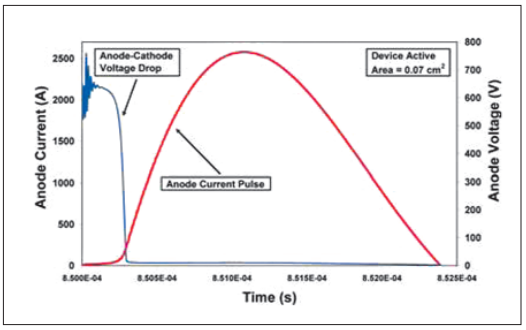

Figure 9. SiC thryristor anode voltage and anode current pulsed-power waveforms.

DARPA/ONR/Navsea, SiC power devices for SSPS and other applications.

GE CRD, SiC power devices for robust integrated power electronic systems.

University of Puerto Rico Mayagüez, Electro-thermal simulation of power electronic systems.

University of Wisconsin Madison, SiC power system simulation.

Purdue University/Carnegie Mellon University/Vanderbilt University/Auburn University, Development of process technologies for SiC power device.s

Electric Power Research Institute, power semiconductor devices for solid state intelligent universal transformer.

Department of Energy, electric vehicle power electronics and power converters for 300 MW fuel cell generation plant.

Stanford University, numerical simulation of SiC power semiconductor devices.

Army Research lab, Pulsed power semiconductor devices.

Publications

J. M. Ortiz-Rodríguez, M. Hernández-Mora, T. H. Duong, S. G. Leslie, and A. R. Hefner, *"Thermal Network Component Models for 10 kV SiC Power Module Packages,"* to appear in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

T. H. Duong, J. M. Ortiz-Rodriguez, R. N. Raju, and A. R. Hefner, *"Electro-thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module,"* to appear in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

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Madelaine Hernández-Mora, Adwoa Akuffo, Colleen Hood, José M. Ortiz-Rodríguez, and Allen Hefner, *"Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability,"* to be appearing in 2007 IEEE Power Electronics Specialists Conference (PESC), Orlando, FL.

Allen R. Hefner and Sharon Beermann-Curtin, *"Status of the DARPA WBST High Power Electronics Program in SiC Device Development and Technology Transition,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2007, March 19-22, 2007, Lake Buena Vista, FL.

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Organic Electronics Metrology

Technical Contacts:
D. DeLongchamp
D. Gundlach
L. Richter

Goals

Organic electronic devices are increasingly incorporated into commercial prototypes and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need has emerged for new diagnostic probes, tools, and methods to address new technological challenges. Organic electronics adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of measurement methods to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provide the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics.

Customer Needs

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high volume manufacturing, incorporation on flexible substrates, and designed functionality. Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification tags. Market estimates range from $10 billion to $30 billion (B) globally by 2010 to 2015, with applications in displays, logic, and lighting. Organic light emitting diodes for displays and lighting form the first generation of products, projected to grow from approximately $0.5 B today to $3 B in 2010. Market expansions to $250 B by 2025 have been estimated should major technology and business barriers be overcome. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. Without this knowledge, guided improvements in materials, processing, and device design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces in organic devices is critical to proper interpretation of carrier transport behavior. Identifying and controlling specific contributions to performance variation requires metrology unavailable to device manufacturers and spanning multiple disciplines that include device physics, chemistry, and materials science.

Technical Strategy

The initial focus of the NIST program is on the organic field effect transistor (OFET) because it is the basic building block of circuitry. The fundamental framework, characteristics, and issues that arise during OFET development are transferable to other organic electronic devices because performance in most other devices is also dominated by the microstructure, chemistry and resulting electronic structure at interfaces. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics: unique measurements of organic materials and interfaces for both structure and chemistry and electronic properties; and the development of an integrated measurement test platform to correlate device performance with the processing conditions, microstructure, and primary chemical structure of organic semiconductors.

1. Interfacial structure and chemistry fundamentals: The basic OFET consists of thin layers (20 nm to 50 nm thick) of disparate materials including the organic semiconductor, dielectric, electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance.

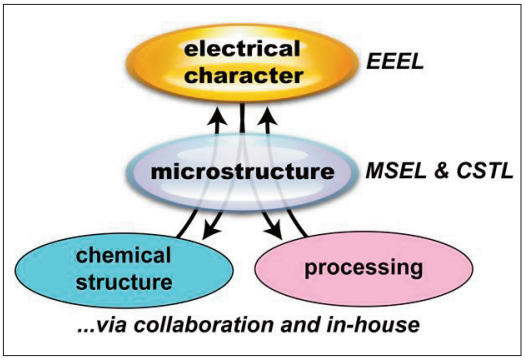

Figure 1. Project paradigm

Correlation development is organized by the paradigm shown in Figure 1, where the microstructure and electronic consequences of variations in chemical structure and processing are precisely measured, and then fed back to our customers to inform further development.

We are developing a suite of powerful measurement methods including X-ray, neutron, optical probes, and electrical tests to characterize critical organic interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET electrical performance. Near-edge X-Ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements and measure the orientation of interfacial molecules. Spectroscopic ellipsometry (SE) is a powerful tool to study the electronic state of molecules and evaluate how the transition dipoles of electronic excitations are oriented with respect to film geometry. Polarized infrared absorption (IR) spectroscopy provides both configuration and orientation information for many chemical moieties common to organic electronics materials. Specular and grazing X-ray diffraction (XRD) measurements measure long range positional order to describe unit cell configuration and domain size information. Scanning probe techniques such as atomic force microscopy provide surface morphology information to assess domain shape, size, and spacings. Finally, small-signal capacitance-voltage analysis of the contact and channel properties of OFETs provides unprecedented insight to the electronic structure, charge trapping, and transport at the semiconductor-gate dielectric interface, and is complimentary to DC electrical measurements which are widely used to evaluate material and device performance.

DELIVERABLES:

- Complete structural and electrical measurements of liquid crystalline semiconducting polymer films cast and heated upon dielectrics with controlled nanoscale radii of curvature. 2Q 2008
- Complete detailed structure measurements of controllably oriented single crystals of a liquid crystalline poly(thiophene). 3Q 2008
- Complete NEXAFS, XRD, polarized IR, SE, and AFM measurements of liquid crystalline semiconducting polymer films as a function of the side chain attachment point. 4Q 2008
- Complete structural and electrical measurements on single crystals and thin films of solution processable small molecule semiconductors. 4Q 2008

2. In situ measurement platform: The highest charge carrier mobilities of semiconducting polymers are obtained only after the film is heated through a mesophase transition. Detailed microstructure analysis of the polymer film during the mesophase transition is critical to determining optimal chemical structures for future generations of polymer semiconductors.

We are developing methods for performing structure measurements described in section 1 on samples while they are heated through a mesophase transition. NEXAFS and polarized IR will monitor the configuration and orientation of the side chains. XRD will measure the thermal expansion of the lattice and the growth and orientation of ordered domains. Polarized optical microscopy will determine the degree of spatial reorganization of the film through changes in the birefringence. NEXAFS and SE will monitor the orientation of the polymer backbone. Transistor measurements will assess the combined effects of thermal disorder, film reorganization, and the thermal activation of charge carriers. The combination of each of these measurements will be used to determine the packing arrangement of the polymer in the mesophase and identify the key structural elements of the molecule responsible for the mesophase, and the mechanism whereby heating to the mesophase increases carrier mobility.

DELIVERABLES:

- Determine the nature of the second mesophase of liquid crystalline semiconducting polymer films, and elucidate the state of the side chains and backbone within it. 3Q 2008

- Develop MEMS-based calorimeter to assess the thermodynamics of phase changes and nonequilibrium structure development in very thin films (<100 nm). 4Q 2008
- Determine influence of dynamic disorder (phase changes and non-equilibrium structure) on charge injection and transport. 4Q 2008.

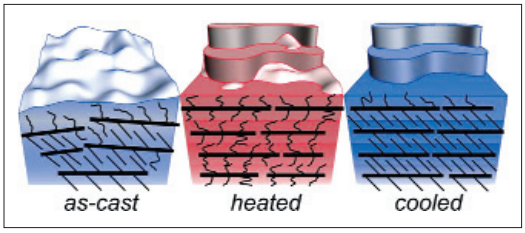

Figure 2. pBTTT annealing mechanism

Accomplishments

A strategy was developed to successfully determine the molecular mechanism of performance enhancement in the thermal annealing of the currently highest-performing polymer semiconductor, poly (2,5-bis(3-tetradecylthiophene-2-yl)thieno[3,2-b]thiophene) (pBTTT-C14), in collaboration with Merck Chemicals. Microstructure development throughout a heating cycle was characterized in-situ by specular XRD to follow changes in the film order perpendicular to the substrate, while a combination of in-situ polarized absorption spectroscopies (IR, visible, and X-ray) were applied to determine changes in the configurations and orientations of the side chains and conjugated backbone. This combined approach allowed characterization of virtually all aspects of film structure as they change with temperature. We found that the overall layer structure dramatically improved upon entering the mesophase at ≈ 140°C. Surprisingly, high levels of backbone order, -stacking, and field effect mobility were maintained throughout the transition. The polarized IR measurement revealed that the molecular mechanism of the performance enhancement was the melting of the alkane side chains, which must be completed before the layers can reorganize. This requirement is consistent with the significant level of side chain interdigitation in the crystalline phase. Crystalline and interdigitated side chains can be regarded as rigid links extending vertically that constrain the lateral motions of backbones and packed backbone layers. Only when the side chains are completely melted can the backbones freely move, to eliminate packing defects in a smectic-like liquid crystalline state. Upon cooling, the side chains recrystallize to capture and maintain the high level of layer order/alignment achieved in the mesophase (Fig 2). Side chain interdigitation therefore provides a general mechanism to achieve and then preserve layer order, because it both allows "repairs" to defective or small crystals that form during solidification from solution and then “locks in” the order. Further advances in polymer semiconductor synthesis must consider the interplay among 1) the backbone / side chain interactions driving layer order, 2) side chain crystallinity and interdigitation (influenced by attachment density and possibly attachment point) that provide a mechanism for three-dimensional crystallization, and 3) the mesophase and its smetic-like structure that permits lateral domain growth.

We previously reported that pBTTT-C14 forms large and well-oriented terraced domains after it is cast and annealed upon flat substrates, but significant detrimental morphology changes occur upon dielectrics with root-mean square (RMS) roughness greater than 0.5 nm. This critical RMS roughness implies that there exists a condition at which pBTTT domains can no longer conform to the nanoscale curvature of the substrate. To precisely determine this critical condition, we developed model dielectrics with controlled radii of curvature using imprint lithography. Characterization by AFM, scanning electron microscopy (SEM), and field-effect carrier mobility measurements revealed that features with a radius of curvature between 12 nm and 20 nm can interrupt domain growth during terrace formation. This critical nanoscale radius provides a precisely quantified guideline for acceptable dielectric characteristics, to facilitate the design of new high-performance flexible circuits.

Systematic evaluation of transistor geometry revealed that polymer semiconductor charge carrier mobility varies with channel length, and the highest mobilities occur in the shortest channels. A detailed analysis of the temperature dependence of the current-voltage characteristics for transistors with different channel lengths showed that the transistor current was not contact limited for temperatures less than 300 K and proved that the mobility was field-dependent, following a Poole-Frenkel-like behavior. The field dependence was strongest for the most ordered films. These results have important implications for channel and dielectric scaling, and may improve the accuracy of organic transistor models for robust circuit design.

Collaborations

Polymers Division, MSEL – Jan Obrzut, Youngsuk Jung, Tatiana Psurek, Leah Lucas, Eric Lin, Joseph Kline.

Semiconductor Electronics Division, EEEL – Curt Richter, Oleg Kirillov, Behrang Hamadani, Oana Jurchescu.

Ceramics Division, MSEL – Daniel A. Fischer, Joseph Woicik.

Surface and Microanalysis Science Division, CSTL – Andrew Moad.

University of California, Berkeley – Kanan Puntambekar, Clayton Mauldin, Jean Fréchet, Vivek Subramanian

Palo Alto Research Center – Michael Chabinyc, John Northrup.

Queen Mary University - Martin Heeney, Natalie Stutzmann.

Imperial College- – Iain McCulloch.

Stanford Synchrotron Radiation Laboratory – Michael Toney.

Corning – Sue Gasper, He Mingqian.

Northwestern – Antonio Facchetti, Tobin Marks.

University of Kentucky – John Anthony.

Penn State University – Tom Jackson.

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DeLongchamp et al., *"High Carrier Mobility Polythiophene Thin Films: Structure Determination by Experiment and Theory,"* Adv. Mater. 19, (2007) 833-837.

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Micro- and Nano-Electro-Mechanical Technology Metrology

Goals

The objective of this project is the development of test structures, test methodologies, and standard reference materials (SRMs) for the characterization of Micro-Electro-Mechanical and Nano-Electro-Mechanical Technology (Micro-nano technology (MNT) fabrication processes. MNT is the extension of MEMS (Microelectromechanical Technology Systems) to include nanometer-scale technology. Full characterization of an MNT process requires accurate measurement of a large set of material properties, including Young's modulus, residual stress, thermal coefficients, surface roughness, density, and Poisson's ratio; dimensional metrology; and device parameters. Ideally these measurements should be quick, performed in the manufacturing line, with measurements at multiple locations across each wafer to allow characterization of process variation.

Customer Needs

Two NIST U.S. Measurement System (USMS) workshops have been held relating to MNT metrology.

The first USMS Workshop was held in Pittsburgh, PA on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions approximately seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" MEMS. The concept of fabless MEMS is one in which a company can produce devices via a foundry rather than their own, expensive (over $100 million), fabrication facility. This is similar to the IC foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop was published in the MEMS Industry Group (MIG) 5-year anniversary report.

The second USMS Workshop was held on March 15, 2006, during Pittcon, in Orlando, Florida. This meeting was targeted at metrology needs for microfluidics applications. Representatives from seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

Technical Strategy

Overview: The MNT Metrology Project is currently championing MNT standardization efforts in three venues: ASTM, SEMI, and NIST. Highlighting the need for MNT standardization is the number of companies and other organizations participating in these standards activities.

ASTM: The first four MNT standards (on in-plane lengths, residual strain, strain gradient, and terminology) and associated publications originated in the ASTM E08.05.03 Task Group on Structural Films for MEMS and Electronic Applications. Also within this task group, a standard is being developed for determining Young's modulus, ultimate strength, and fatigue for a surface micromachining process.

SEMI: The MNT standardization efforts being actively pursued in SEMI's North American MEMS Standards Committee include recently-published SEMI Standard MS1-0307 on wafer-to-wafer bonding alignment targets, SEMI MS2-0307 on step height measurements, SEMI MS3-0307 on MEMS terminology, SEMI MS4-1107 on Young's modulus measurements, and SEMI MS5-1107 on critical wafer bond toughness. Other SEMI MNT standardization efforts include a a proposed guide for the design and materials for interfacing microfluidic systems (Doc 4213A), specifications for microfluidic interfaces to electronic device packages (Doc 4214A), a guide for evaluating hermeticity of MEMS packages, and work on a draft standard for stiction.

An additional activity in SEMI's MNT standardization effort is the identification of standards related to MNT technology. SEMI is attempting to identify these standards and incorporate them into SEMI's "Living Standard." This Living Standard, which will list MNT standards from all standardization bodies and be maintained by the

Technical Contacts:
J. Marshall
C. McGray
R. Allen

"Having seen your proposed work and timetable for producing the (MNT 5-in-1) SRM, we support your work in this area and see value in the semiconductor and MEMS arena."

Mark Crockett,
Applied Materials

"We have more than 100 unique MEMS customers, from Fortune 500 companies to small university labs, and believe the proposed (MNT 5-in-1) standard would be of high interest to all of them."

Erik Novak,
Veeco

North American MEMS Standards Committee, will serve to guide industry and researchers to existing standards and highlight areas where standards may be needed.

NIST: Currently, there are five major standardization thrusts at NIST in the MNT Project:

1. Publications that support select ASTM and SEMI standards and that include the SED MEMS Calculator Web pages.

2. The development of the MNT 5-in-1 Standard Reference Materials (SRMs).

3. The development of the SEMI standard MS5, Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures and the development of the Micro-Chevron SRM utilizing this standard test method.

4. Dimensional metrology for microfluidics.

5. Cutting edge robotics research and development leading to standardization efforts.

Specific details associated with each of these activities are presented in the Accomplishments section.

DELIVERABLES:

Deliverables associated with ASTM and SEMI standards activities:

- Participation on the planning committee for SEMI's International MEMS Workshop to be held at SEMICON West 2008. 3Q 2008
- Draft "Living Standard" and easy-to-access SEMI Standards Web page incorporating, for example, a compilation of all MNT standards and pertinent links for purchasing. 3Q 2008
- Deliverable associated with publications that support select ASTM and SEMI standards and that include the SED MEMS Calculator Web pages:
- Updated SED MEMS Calculator Web pages for increased compatibility with the MNT 5-in-1 SRM(s). 3Q 2008
- Deliverables associated with the development of the MNT 5-in-1 SRMs:
- Poster paper presentation on the current status of the MNT 5-in-1 SRMs for the Solid-State Sensors, Actuators, and Microsystems Workshop, Hilton Head, SC. 2Q 2008
- Viability checks of the MNT 5-in-1 SRM chips for use in a Step Height and Young's Modulus Round Robin. 4Q 2008
- Completed User's Guide for a Step Height and Young's Modulus Round Robin. 4Q 2008

Deliverables associated with the development of the Micro-Chevron SRM:

- Presentation of an invited paper "Wafer Bonding Standardization" describing the development of the SEMI standard MS5-1107, Wafer Bond Strength Measurement at the 2007 Conference on Wafer Bonding for MEMS and Wafer Level Integration in Halle, Germany. 1Q2008
- Organize an international round robin to provide precision and bias results for MS5-1107. 3Q2008
- Prepare modifications of MS5-1107 to reflect results from international round robin. 4Q2008 (or 1Q2009)

Deliverable associated with dimensional metrology for microfluidics:

- Prototype test chip for microfluidics dimensional metrology. 4Q 2008

Deliverable associated with cutting edge robotics research and development which will lead to standardization efforts:

- Organize an exhibition of nanogram-scale robotics capability to help define the events for the 2009 competition. 3Q 2008

Accomplishments

■ The standards recently published in SEMI are for Young's modulus, residual stress, residual-stress gradient, and critical wafer-bond toughness. The parameters are expected to undergo round robin testing in order to validate the standards. These parameters are described below:

■ *Young's modulus:* SEMI standard MS4-1107 obtains Young's modulus from resonating cantilevers and fixed-fixed beams oscillating out-of-plane. It applies to films, such as found in MEMS materials, which can be imaged using a non-contact optical vibrometer or comparable instrument.

■ *Residual stress and its gradient:* SEMI standard MS4-1107 also provides for residual stress and stress gradient calculations. These calculations require the Young's modulus value obtained in the standard and values for residual strain (ASTM E 2245) and strain gradient (ASTM E 2246). High values of residual stress lead to failure mechanisms in ICs such as electromigration, stress migration, and delamination. Knowledge of the residual stress values can be used to improve the yield in CMOS fabrication processes.

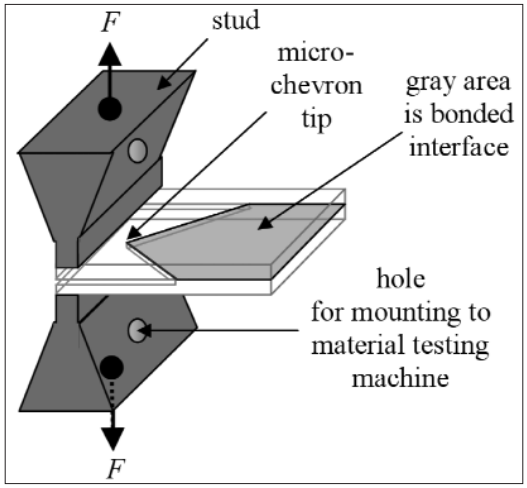

Figure 1. Studs mounted to a micro-chevron test structure.

■ *Critical wafer bond toughness:* SEMI standard MS5-1107 uses micro-chevron test structures which consist of two materials, typically two silicon wafers bonded together. The main characteristic of the test structure is the wedge-like structure (which gives it its name) in the bond interface. Studs or blocks are glued to either side of the test structure and positioned in the material testing machine where the test structure is pulled apart (see Fig. 1). The maximum load is measured and the critical wafer bond toughness is calculated, which is a measure of the wafer bond strength. This draft standard can be used to determine a preferred bonding technique and it can be used to obtain on-wafer spa

■ *Thickness:* SEMI Standard MS2-0307 on step heights was recently published. Step height measurements are incorporated in an electro-physical technique to find the thicknesses of all the layers in a 1.5 µm commercial CMOS foundry process. Figure 2 shows a test chip design with thickness test structures along the top edge of the chip. A design rendition of a sample thickness test structure is given in Fig. 3a, with its cross section given in Fig. 3b.) Relatively low values for combined standard uncertainty u_c (between 0.20 nm and 150 nm for a given processing run) have been found. In addition, an earlier version of this technique has been supported via the successful optimization of the Young's modulus values for the various layers in the process.

As a rule of thumb, the electrical approach (that obtains thicknesses from capacitance, sheet resistance, and resistivity values) is preferred for thicknesses with u_c values less than or equal to 0.035 µm. This corresponds somewhat to the layers, such as the poly2-to-poly1 oxide and the poly2 layers, which tend to be fabricated earlier in the processing sequence. The capacitances for the oxide layers fabricated earlier in the processing sequence are typically higher and thus easier to measure accurately. For capacitances less than or equal to 24.7 aF/ m^2, the physical approach (that obtains thicknesses from step height measurements) is preferred.

The electro-physical technique is detailed in a 39-page paper.

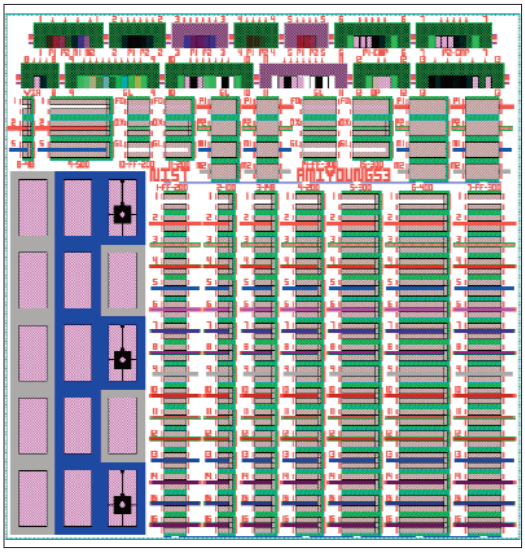

Figure 2. CMOS test chip design incorporating thickness test structures, cantilevers, fixed-fixed beams, and tensile test structures.

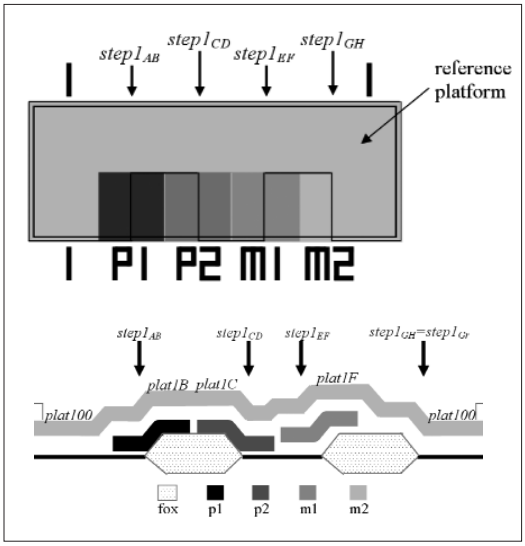

Figure 3. For a thickness test structure: a) a design rendition and b) a cross section.

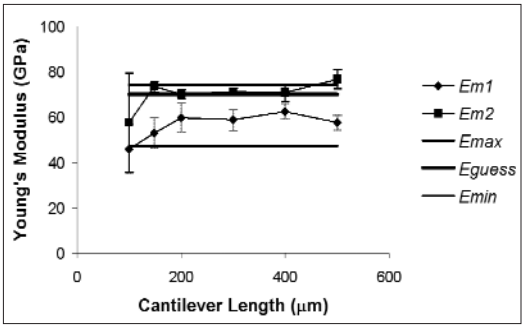

Figure 4. Optimized Young's modulus values for metal1 and metal2 versus length.

■ *Young's modulus:* The test chip design given in Fig. 2 includes cantilevers ranging in length from 100 μm to 400 μm. Plots of Young's modulus versus length for each layer exhibit phenomenal results. *The optimized Young's modulus results are stable as a function of length and within the realm of acceptability!* Figure 4 shows these plots for metal1 and metal2. The data points given at L=500 μm represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds represent values given in the literature. The line represented by *'Eguess'* is the initial value used in the optimization. An initial result from tensile tests done by David Read at NIST-Boulder found an average metal1 and metal2 Young's modulus value of 63 GPa, which falls nicely between the metal1 and metal lines in Fig. 4.

■ *SED MEMS Calculator Web pages:* The SED MEMS Calculator Web site includes data sheets on which calculations can be performed that go hand-in-hand with select MEMS standards or standards-related work. The most recent additions to this web site include data sheets for a) step height calculations, b) thickness calculations for all the layers in a 1.5 μm CMOS process, and c) Young's modulus calculations.

■ A proposal was crafted for the development of the MNT 5-in-1 SRMs. Currently, there are two different MNT 5-in-1 SRM designs; one for a surface-micromachining MEMS process at MEMSCAP (see Fig. 5) and the other for a bulk-micromachining CMOS MEMS process via MOSIS (see Fig. 6). The prototype MNT 5-in-1 SRMs are expected to double as the Young's modulus and step-height round robin test chips. The five parameters will be in-plane length, residual strain, strain gradient, step-height, and Young's modulus. The first three parameters have been standardized in ASTM as E 2244, E 2245, and E 2246. The fourth and fifth parameters recently became the MS2-0307 and MS4-1107 standards in SEMI.

The five measurements will be taken at NIST on the 5-in-1 SRM and delivered to the customer in order for them to compare their in-house measurements with those taken at NIST, thereby validating their use of the documentary standards.

Customers, including design companies, equipment manufacturers, and fabrication services, have expressed support for this SRM.

This is an interlaboratory effort, involving several of NIST's laboratories.

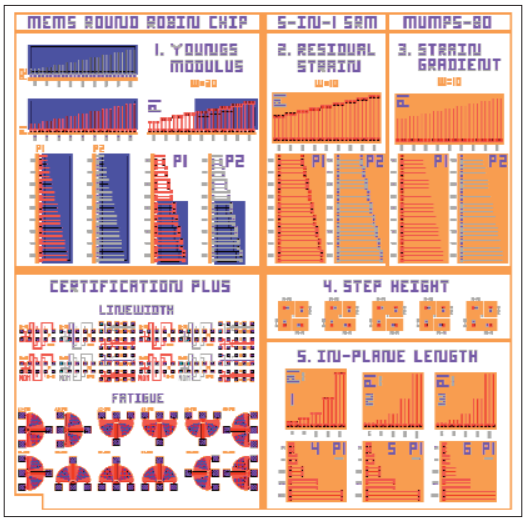

Figure 5. MNT 5-in-1 design for a surface-micromachining MEMS process.

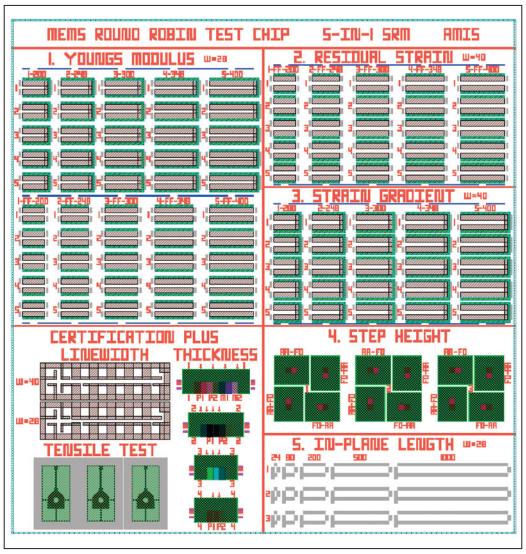

Figure 6. MNT 5-in-1 design for a bulk-micromachining CMOS MEMS process.

■ A proposal was crafted for the development of a micro-chevron SRM for the calibration of critical wafer bond toughness. A micro-chevron test structure (see Fig. 1) would be used in this destructive test.

Wafer-wafer bonding is a mainstay for MEMS design and fabrication. MEMS components, such as acceleration sensors, gyroscopes, micropumps, or microvalves that are increasingly found in smart automotive and navigation control systems or in medical devices typically use wafer bonding technologies. Due to being subjected to mechanical stresses, the industrial applications of these components require both a high mechanical strength and reliability of the wafer-bonded interface. For a knowledge of the strength determining factors (such as fatigue and stress corrosion) of wafer bonding, for quality control, and for the development of new bonding technologies, a method for determining the strength of such bonds is important to producers and users of MEMS devices, of wafer bonding equipment, and of wafer materials.

■ In the area of dimensional metrology for microfluidics, the MNT Metrology Project has undertaken development of dimensional metrology test structures and techniques. The goal of this work is standard test structures, methods, and analysis techniques such as exist for semiconductor devices.

■ In the area of microrobotics, the MNT project held the first-ever competition between nanogram-scale microrobots. The competition was held in association with the 2007 RoboCup International Championships in Atlanta, GA in July, 2007. The competition produced novel microrobotic technologies and MEMS actuators, and received extensive press coverage from CNN, MSNBC, ABC News, and 117 affiliates of the Associated Press. In addition, the event was reported on the front page of DoC website. The competition revealed technological challenges and metrology needs, including the following:

1. Environmental control for microrobotics stations.

2. Techniques for imaging trapped charge in dielectric surfaces and films.

3. Assessment of contact mechanics in sliding-mode micromechanical actuators.

4. Integrated control of magnetic fields in microrobot operating environments.

5. Bandwidth multiplexing for capacitively-coupled microrobotic devices.

Collaborations

Collaborators for publications that support select ASTM and SEMI standards and that include the SED MEMS Calculator Web pages

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. P. Thomas Veriner

University of Maryland, College Park, MD, Dr. Don L. DeVoe

Collaborators for the development of the MNT 5-in-1 Standard Reference Materials (SRMs)

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. P. Thomas Veriner

MEMSCAP Inc., 4021 Stirrup Creek Drive, Suite 120, Durham, NC, Buzz Hardy

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read

Pennsylvania State University, University Park, PA, Dr. Christopher L. Muhlstein

Collaborators for the development of the Micro-Chevron SRM:

BayTech Group, 30 Winsor Way, Weston, MA, Winthrop A. Baylies

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read

Univ. of Wisconsin, Dr. Kevin Turner

Fraunhofer Inst. (Germany), Dr. Joerg Bagdahn

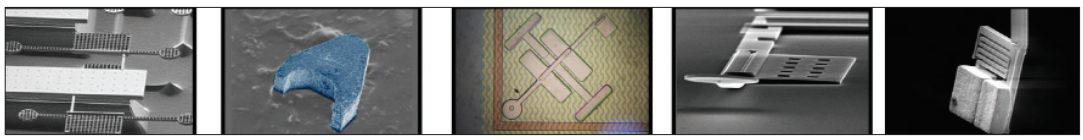

Figure 7. The five micro robots that competed in the 2007 RoboCup International Championships Nanogram Demonstration League in July 2007.

NIST Gaithersburg, Materials Science and Engineering Laboratory, Ceramics Division, Dr. George Quinn

Collaborators for dimensional metrology for microfluidics:

NIST Gaithersburg, Chemical Science and Technology Laboratory, Dr. Barbara Jones

Collaborators for the cutting edge robotics research and development which will lead to standardization efforts

Carnegie Mellon University, Nanorobotics Laboratory, Dr. Metin Sitti

Carnegie Mellon University, Electrical and Computer Engineering Department, Dr. Gary Fedder

U.S. Naval Academy, Dr. Samara Firebaugh

ETH Zürich, Dr. Brad Nelson

Simon Fraser University, Dr. Ash Parameswaran

Publications

SED MEMS Calculator Web site: www.eeel.nist.gov/812/test-structures/MEMSCalculator.htm.

J. C. Marshall, D. L. Herman, P. T. Vernier, D. L. DeVoe, and M. Gaitan, *"Young's Modulus Measurements in Standard IC CMOS Processes using MEMS Test Structures,"* IEEE Electron Device Letters 28 (11), 960-963 (2007).

J. C. Marshall and P. T. Vernier, *"Electro-physical Technique for Post-fabrication Measurements of CMOS Process Layer Thicknesses,"* NIST Journal of Research, vol. 112, no. 5, 2007, p. 223-256.

SEMI MS5-1107, *"Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures,"* November 2007.

SEMI MS4-1107, *"Test Method for Young's Modulus Measurements of Thin, Reflecting Films Based on the Frequency of Beams in Resonance,"* November 2007.

SEMI MS2-0307, *"Test Method for Step-Height Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* March 2007.

MEMS Industry Group (MIG) 5-Year Anniversary Report, *"Standardization and the Study of the U.S. Measurement System for Micro Nano Technologies,"* September 2006.

J. C. Marshall, R. I. Scace, and W. A. Baylies, *"MEMS Length and Strain Round Robin Results with Uncertainty Analysis,"* NISTIR 7291, January 2006.

ASTM E 2444–05, *"Standard Terminology Relating to Measurements Taken on Thin, Reflecting Films,"* January 2006.

ASTM E 2246–05, *"Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* December 2005.

ASTM E 2245–05, *"Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* December 2005.

ASTM E 2244–05, *"Standard Test Method for In-Plane Length Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* December 2005.

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NIST's Center for Nanoscale Science and Technology Nanofab

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A. Novembre

Goals

The CNST Nanofab is a national, shared access, shared cost, user facility that provides for the measurement and fabrication of nanoscale structures, including electronic devices, magnetic devices, MEMS, bio-devices, prototypical nanoscale test structures, measurement instruments, and standard reference materials. It provides:

Access to expensive nanoscale measurement and fabrication tools, technologies, and expertise in a shared-access, shared-cost environment to both NIST and external users.

A venue to foster collaboration in nanotechnology across NIST's laboratories and with NIST's external partners in industry, academia, and other government agencies.

A workplace that enables CNST and others to help remove the measurement barriers that are delaying or preventing the implementation of new products based on nanotechnology.

Customer Needs

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in a variety of nanotechnologies in the face of heightened global competition, NIST has established the Center for Nanoscale Science and Technology (CNST). Its mission is to provide science and industry with the necessary measurement methods, standards, and technology to facilitate the development and productive use of nanotechnology from discovery to production. A key component of the CNST is the Nanofab, a national, shared access user facility that provides an economical means to access the expensive tools required to measure and fabricate nanostructures. The CNST Nanofab is located in two of the five buildings (see Fig. 1) in the Advanced Measurement Laboratory (AML) at the Gaithersburg, Maryland campus.

Technical Strategy

The AML location provides the CNST with superior vibration, temperature and humidity control, and air cleanliness. The Nanofab cleanroom has approximately 740 m^2 of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment (capable of processing 150 mm wafers) that is now fully operational (Fig. 2). This includes wet chemical wafer cleaning stations, KOH/TMAH silicon wet etch station, acid wet etch station, photoresist and e-beam resist processing stations, furnaces (two banks of four tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, six reactive ion etchers (SF_6/O_2, F_2 Metal, Cl Metal, deep Si, deep SiO_2, III-V), one XeF_2 isotropic silicon etcher, four metal deposition tools (one thermal, one e-beam, two sputterers), contact lithography (front- and back-side alignment), critical point dryer, microwave plasma asher, atomic layer deposition, wafer bonder, photomask laser writer, parylene deposition, dicing saw, wire bonder, nanoimprint lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, two AFMs, stress measurement, table-top SEM). A state-of-the-art e-beam lithography system with mask making capability has been in operation since November 2007.

Figure 1.Main entrance to the AML showing the CNST Nanofab on the left.

Figure 2. Oxidation and annealing furnace banks.

The Nanofab is operated as a shared access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, are permitted to independently operate the equipment. As of May 1, 2007, the CNST Nanofab is accessible to users from outside NIST, such as academia and industry. The tools are operated in a manner such that a wide variety of materials can be processed. The tools are benchmarked periodically, generally on a monthly basis, to ensure process stability and repeatability. A set of standard processes are available and process development assistance is offered by the Nanofab staff when required. Additionally, the CNST Nanofab is unique in that it is located in close proximity to the CNST Research Division, the NIST Laboratories, and the NIST Center for Neutron Research which contain both a wealth of measurement science expertise and a vast array of state-of-the-art and advanced prototype tools.

DELIVERABLES:

- Deep SiO_2 etcher, III-V etcher and ALD to be operational in 3Q2008

Metrology for Spintronic Devices

Technical Contacts:
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W. Rippard

"Imaging and metrology of magnetic structures are at the heart of the systematic development and characterization of magnetoelectronic materials and devices"

WTEC Panel on SPIN ELECTRONICS Final Report August 2003 (p.18)

Goals

The overall goal of the Metrology for Spintronic Devices program is to develop the metrological tools that will enable the development of electronic devices that exploit the electron spin degree of freedom in addition to its charge. Present spintronic devices include magnetic random access memory (MRAM), which has the possibility of becoming a "universal" memory element, hard-disk drive read heads, and other highly-compact magnetic memory devices, such as those based on current induced domain-wall motion in magnetic wires. In addition, spintronic devices also present an avenue towards replacing conventional complementary metal oxide semiconductor (CMOS) technology as device dimensions shrink into the deep nanometer regime, development of entirely new device structures such as nanoscale microwave components for on-chip spectral analysis, nanoscale timing elements, and microwireless communication architectures. In each case, a fundamental understanding of the interactions between a spin-polarized current and ferromagnetic metals and semiconductors is a necessity. The particular goal of this project is to develop the metrology and perform the fundamental measurements to enable the development of these spin-based devices.

An additional goal is to enable the development of magnetoelectronic and spintronic devices by using Scanning Electron Microscopy with Polarization Analysis (SEMPA) to directly image the nanoscale magnetic structure and correlate the magnetic structure with device performance.

Customer Needs

MRAM elements have been incorporated into products commercially available from late 2006. Although no public roadmap for MRAM exists, companies such as IBM and Freescale Semiconductor expect that the present circuit architecture, which relies on switching (writing) using applied magnetic fields, will not be viable beyond the 65 nm lithography node. These limitations arise because the scaling laws associated with the stability of the magnetic structures used in MRAM devices: As the device dimensions are decreased, the magnetic elements are required to have increased stability against thermal fluctuations. This, in turn, will require larger writing fields, which cannot be supported in the present device architecture. It is expected that a new switching mechanism will be required for scaling MRAM devices below the 65 nm node. One way to circumvent this scaling limitation is to switch the elements through the use of spin-polarized currents flowing through the memory elements to switch (write) them via the spin transfer effect. While this switching mechanism is largely expected to allow continued scaling of MRAM elements, it has been experimentally demonstrated only within the last six years, and the present understanding of the effect remains only qualitative. In order to enable the continued scaling of MRAM devices, the fundamental metrology and measurement of the intrinsic scaling laws associated with the spin transfer effect are a necessity. In particular, methods to definitively relate threshold switching currents to fundamental materials properties need to be developed, materials damping parameters need to be measured as a function of device size, and tunnel junction characteristics need to be understood at the atomic scale.

The performance, and ultimately the commercial viability, of magnetoelectronic devices such as Magnetic Random Access Memories (MRAM) or magnetic field sensors depend on understanding and controlling their magnetic nanostructure. Nanoscale magnetic features such as domains, domain walls, anisotropy dispersion, edge effects, grain structure, and defects critically affect device performance. Imaging these magnetic nanostructures requires techniques with high spatial resolution and high magnetic sensitivity that do not disturb the tiny amount of magnetic material used in a device. SEMPA has 10 nm spatial resolution, 1000 Fe atom sensitivity, and is nondestructive while imaging. Furthermore, SEMPA images the magnetization directly allowing direct comparisons with computer generated micromagnetics simulations of ideal devices.

More generally, many semiconductor devices encounter scaling limitations as the device dimensions shrink into the deep nanometer regime. For instance, present CMOS scaling laws indicate that the devices will encounter both quantum mechanical and fabrication limitations below the 10 nm length-scale. One potential avenue towards circumventing this roadblock is spin-based devices, which afford the possibility of fast operation, low power-dissipation, and general compatibility with CMOS-based device fabrication. Furthermore, novel effects which occur

only at the nanoscale in hybrid ferromagnetic systems can also be exploited to provide new functionality in nanoscale devices. These devices point a way to creating new nanoscale systems such as on-chip spectral analysis, nanoscale microwave generators, as well as nanoscale microwave mixers, phase discriminators, and chip-to-chip wireless communication schemes. However, as with the spin-based memory devices, in order for these spin-enable devices to be commercially realized, the fundamental measurement techniques required to understand the interactions between spin polarized electrons and ferromagnetic materials need to be developed and implemented.

Technical Strategy

The technical strategy is to develop the metrology and perform the fundamental measurements to characterize and understand the effects of spin-polarized currents in spin-based magnetic nanostructures. Particular attention will be paid to the intrinsic scaling laws associated with device switching times in both all-metallic and magnetic tunnel junction MRAM structures, as well as the thermal contributions to the critical current densities. These measurements will help to provide a basis for scaling of MRAM devices below the 65 nm node. Our technical work will also focus on evaluating the potential of nanoscale spintronic devices for replacing/augmenting CMOS in the deep nanometer regime. One potential method to transmit information without charge is through the use of spin waves. Our work will focus on understanding the generation, transmission, and phase control of localized nanoscale spin wave oscillators.

1. Develop methods to measure damping in magnetic nanostructures, particularly as a function of oxidation.

DELIVERABLES:

- Measure damping in NiFe magnetic nanodot arrays with sizes ranging from 200 nm to 50 nm. Measurements will be performed on both intentionally oxidized structures and ones capped to prevent oxidation. Compare results with continuous films. Complete measurements in 1Q 2007 and submit results in 2Q 2007
- Develop metrology to electrically excite and detect FMR resonance in individual nanoscale devices made to continuous films and patterned films. Complete measurements in 2Q 2007 and submit results in 3Q 2007

2. Perform magnetic imaging of tunnel junction device under active bias.

DELIVERABLES:

- Develop infrastructure and fabrication techniques to allow Lorentz imaging and simultaneous electrical characterization of magnetic tunnel junction devices under active bias. Complete measurements in 2Q FY 2007 and submit results in 3Q 2007

3. Determination of thermal contributions to linewidths of spin transfer oscillators.

DELIVERABLES:

- Develop infrastructure to measure the linewidth of spin transfer oscillators as a function of temperature (300 K to 10 K) and applied field strength in order to directly determine thermal contributions to oscillator linewidth (phase noise). Complete infrastructure upgrade in 1Q 2007 and complete measurements in 3Q 2007

SEMPA is already an established tool for imaging magnetic nanostructures in simple ferromagnetic structures. As structures are reduced in size to the nanoscale, the fabrication process can affect the magnetic properties, but to date there has not been a systematic investigation of this. Further, special protocols and instrumentation need to be developed for imaging the magnetization in samples that are operationally as close as possible to commercial magnetoelectronic devices. In particular, sample preparation techniques that expose the ferromagnetic element directly to the SEMPA probe need to be developed for a wide range of samples including insulating ferromagnetic oxides and delicate multilayers. Of course these cleaning procedures must not disturb the magnetic structure under investigation. Finally, since a critical question is the behavior of magnetic nanostructures in a functioning device, our recently developed instrumentation now makes possible magnetic imaging while the device is electrically active i.e., while applying magnetic fields or measuring magnetoresistance.

1. Investigate the effect of fabrication method on magnetic structure of nanoscale magnetic elements.

DELIVERABLES:

- SEMPA images of arrays of permalloy magnetic elements (lines, squares and ellipses) ranging from 50 nm to 2 micrometer prepared by FIB, dry etching, and liftoff. 3Q 2007

2. Develop new sample cleaning capability to allow SEMPA imaging of a wider range of sam-

ples including insulating oxides and very thin film multilayers.

DELIVERABLES:

- Integrate electron cyclotron plasma source with the SEMPA system to provide an atom source producing thermal energy neutral atoms, a downstream plasma mode providing low energy ions and neutrals, and a broad beam ion source. 4Q 2007

Accomplishments

■ *High-Speed, Current-Induced Switching for MRAM Devices:* In collaboration with Hitachi Global Storage Technologies (HGST) and Freescale Semiconductors we have demonstrated that sub-nanosecond (290 ps) switching of nanoscale MRAM devices is possible via the spin transfer effect. To date this is the shortest switching time that has been reported in the literature. The inverse switching time (i.e., the switching frequency) at room temperature is linearly proportional to the current applied to the device. This finding is in accordance with the behavior expected from theoretical considerations and indicates that the measured room-temperature switching threshold is strongly affected by thermal fluctuations in the nanoscale devices. By extrapolating the measured switching current to zero applied pulse width, the *theoretical* value of the intrinsic device critical current can be determined. However, this theoretical method of determining the intrinsic switching thresholds (i.e., those related to materials properties and device size) from stochastic, thermally activated switching events had not been experimentally verified. By extensively comparing the thresholds for current driven switching at room temperature and 4 K for a range of applied field values, we have been able to verify the extrapolation methods used to infer the intrinsic switching current, identify thermal contributions to the switching threshold, and determine the materials/device parameters that are responsible for setting the intrinsic switching threshold. These measurements will allow for improved device design and reliability for future MRAM at the 65 nm node and beyond.

■ *Damping in Magnetic Nanostructures:* One of the critical parameters in determining the threshold switching current in magnetic devices is the magnetic damping parameter; the larger the damping in the system, the larger the current required to switch the device. While the material dependent damping parameters have been routinely measured in macro/microscopic devices, very little is known about how damping is affected when device sizes are decreased to the nanometer length scale. As device dimensions are decreased, the surfaces of devices become increasingly important. This is particularly the case for damping in magnetic nanostructures. Nanomagnetic devices will typically have oxidation of the ferromagnetic materials on at least some of their sides, and ferromagnetic oxides are well known sources of damping. Recently some researchers have shown indirect evidence that the magnetic damping in magnetic nanostructures can be increased by more than a factor of ten relative to that of macroscopic devices. We have recently developed the metrology capabilities to *directly* measure the magnetic damping in a variety of magnetic systems over a wide range of device sizes. Our new optical method of measuring damping on arrays of devices has shown that, at room temperature, the oxidation has a negligible effect and shape variations in the nanoscale devices increases the apparent damping by only about a factor of two. We have also developed a new method to electrically measure the damping parameter in single devices having dimensions below 100 nm. These measurements, while still being perfected, corroborate those from the large arrays.

■ *Noise and Current Induced Switching in Magnetic Tunnel Junction Devices:* Currently, typical spin transfer based MRAM structures are based on all-metallic structures. These structures have resistances on the order of 5 ohms to 10 ohms and are poorly impedance matched to standard semiconductor circuitry. While this impedance mismatch will become less severe as device dimensions are decreased, it will likely be necessary to implement magnetic tunnel junction (MTJ) devices. However, in general, there is also an increase in noise, particularly at low frequency, when incorporating tunnel junctions into device structures, which can degrade device performance and read-out fidelity. The low-frequency noise is associated with defects and atomic scale variations in the barrier. We have successfully measured and characterized this excess noise in high-quality aluminum oxide magnetic tunnel junctions with dimensions on the order of several micrometers and used Lorentz transmission electron microscopy (TEM) imaging to investigate the correlation between electronic noise and the structural properties of the

barrier. More recently we have upgraded the TEM instrumentation and fabricated devices so that the magnetic devices can now be imaged with Lorentz microscopy under active bias. This allows us to image directly the magnetic fluctuations in a device while simultaneously measuring its electrical characteristics. Through these simultaneous measurements we can discriminate between intrinsic magnetic fluctuations in the MTJ devices from those associated with electrical defects in the barriers.

■ *Nanoscale Generation of Spin Waves for Communication Architectures:* At present, spintronic devices are being considered as potential replacements for future generation CMOS devices. The basic advantage of the spintronic devices is that they provide the potential to perform both communication and computation through spin instead of charge, and so may be able to perform these operations with comparatively low power dissipation. Several proposed communication and computation architectures are based on the local generation and subsequent propagation of spin waves, Fig. 1. Previously, we have shown that nanoscale magnetic devices are able to generate coherent, gigahertz frequency spin waves. However, the currents required to generate them was relatively high and their propagation away from their source was only theoretical. We have performed the metrology to show directly that in the correct geometry the spin waves can coherently propagate more than 0.5 μm away from their point of generation, putting fairly lenient geometrical constraints on potential device considerations. Furthermore, by incorporating CoFeB materials in these devices we have been able to lower the currents required for the creation of spin waves by roughly a factor of three. This represents a significant advance towards viable device applications.

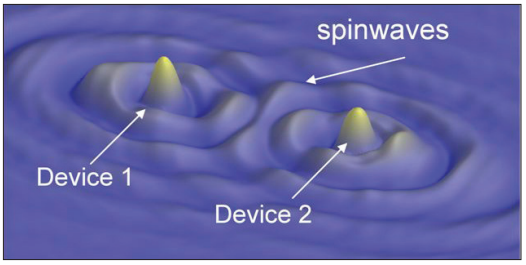

Figure 1. Micromagnetic simulation showing spin wave interactions between two closely spaced nanoscale oscillators.

■ *Nanostructured Magnetic Arrays to Control Motion of Magnetic Flux Quanta:* SEMPA images of a close-packed array of triangular magnetic elements contributed to a multi-institution research effort focused on the control of the vortex motion in superconducting materials. The magnetic elements form an array of asymmetric pinning potentials underlying the superconducting material, which creates a ratchet effect causing a rectified vortex motion (in one direction) when excited by an ac current. This offers interesting possibilities for manipulating flux quanta in fluxonics devices. Fig. 2 (a) shows an array of such triangles in the as grown state. In the lower part of Fig. 2, a higher resolution image of the as-grown magnetization of one of the triangles (b) is compared to the ordered state (c) after applying an in-plane field. The magnetic state of the underlying periodic array of magnetic triangular structures determines the ratchet dynamics of the magnetic flux quanta in the superconductor.

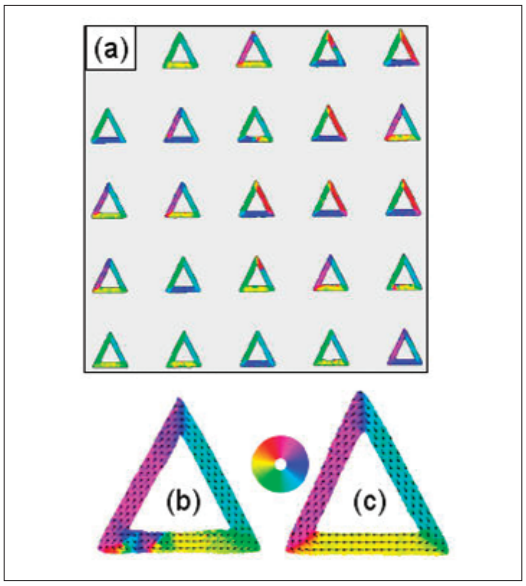

Figure 2. Magnetization (direction given by color wheel) of an array of triangular elements for control of magnetic flux quanta in a superconductor.

■ *Spin Momentum Transfer Switching in Magnetic Nanowires:* Current-driven domain wall motion offers the exciting prospect of manipulating magnetization in magnetic devices without applying an external magnetic field. As the spin-polarized electrons of an electron current in a ferromagnet pass through a domain wall, there is a torque on the electrons tending to align their spin magnetic moments with the magnetization direction. Conservation of angular momentum requires a reaction torque, known as the spin transfer torque,

from the electrons to the magnetization that displaces the domain wall in the direction of electron flow. We have constructed custom sample holders for SEMPA to allow us to image the magnetization in a nanowire while a current is flowing. SEMPA images showing current induced domain wall motion are shown in Fig 3. In the top two panels, (a) and (b), the vortex wall is "pinned" and there is no change on increasing the current from 0 to 4 mA. In Fig. 3 (c), when 5 mA is applied, the wall is seen to have moved to the left in the direction of electron flow. The wall makes a large jump about 80 % of the way through the image which is scanned from top to bottom. The image (d) taken immediately after (c) shows that the wall has moved to the left to be stopped by the next pinning site. Not much is known about the pinning sites, but it is thought that pinning can be caused by structural defects or chemical inhomogeneities. At present, when pinning sites dominate the domain wall motion, the wall moves from one randomly located pinning site to the next. If the extrinsic defects that cause pinning can be eliminated or controlled such that they can be tailored to do a particular job, current induced domain wall motion could have wide applicability in spintronic devices.

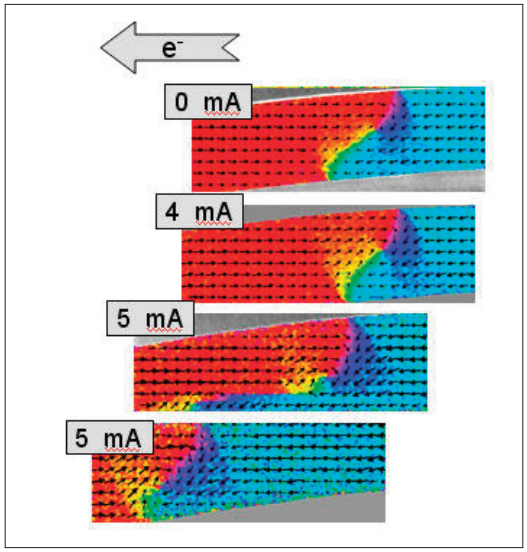

Figure 2. Magnetization (direction given by color wheel) of an array of triangular elements for control of magnetic fl ux quanta in a superconductor.

Collaborations

IBM, MRAM device imaging and thermal induced noise in tunnel-junction based MRAM devices.

Freescale Semiconductor, MRAM device imaging and incorporating magnetic tunnel junctions into MRAM devices.

Hitachi Global Storage Technologies, high-speed switching in all-metallic MRAM devices.

Seagate Technologies, phase-locking mechanisms in spintronic microwave oscillator arrays.

U. S. Army Research Laboratory, delivery of magnetic nanoscale spin wave oscillators.

U.S. Army Research Laboratory, imaging magnetic sensors.

Future Opportunities

Nanoscale spintronic devices also provide an opportunity for the development of dense non-volatile memory elements as well as new spin-enabled nanoscale microwave devices, such as microwave sources and mixers for timing, communications, and spectral analysis applications. In addition, they also provide one potential avenue towards replacing/augmenting conventional CMOS devices in the deep nanometer regime. As such, we expect that spintronic devices hold the potential to have a great impact on the semiconductor industry, particularly as device dimensions shrink into the nanoscale. The goal of this project is to provide the fundamental metrology and measurements to enable the development of this wide range of devices and applications.

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BioElectronics Metrology

Technical Contacts:
D. R. Reyes
J. J. Kasianowicz
M. Gaitan

Goals

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal over the next five years is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

Customer Needs

Cell-based assays are a primary tool used by the pharmaceutical industry to measure therapeutic drug efficacy and cytotoxicity. These time-consuming and labor-intensive assays currently involve millions of cells in each culture reservoir. This leads to some inherent measurement biases since the collective response only represents the average for the whole population and, for example, cells at different stages of development will respond differently to stimuli. A true paradigm shift is to utilize micro- and nano-fabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS. Single-cell assays will isolate the parameters affecting cell response and allow the various subpopulations present in bulk cultures to be distinguished. Single-cell assays, when multiplexed, will allow for more rapid identification of drugs and drug targets.

Technical Strategy

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in-vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, in varied buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in-vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We focused our initial research efforts on the study of retinal (neuronal) cells, and currently, we are working with other mammalian cells such as fibroblasts (NIH-3T3), epithelial cells, and sperm cells.

DELIVERABLES:

- Develop electronic patterning of cells using integrated dielectrophoresis-force transducers for morphogen-controlled cell differentiation studies. 4Q 2008
- Determine the feasibility of electronically measuring the growth and viability of cells anchored to electrodes coated with polyelectrolyte multilayers. 1Q 2009
- Develop novel microfluidic devices with integrated microwave transmission lines for applications in forensic DNA analysis. 2Q 2009
- Develop electronic tools to capture and release nanoparticles including biomolecules and cells. 3Q 2009

Accomplishments

We developed a method to monitor NIH-3T3 fibroblast cell growth on gold electrodes using impedance spectroscopy. In this measurement technique, individual cells are represented as resistive and capacitive elements, which increase the impedance of the system as the number of cells increase. The two-electrode system was fabricated using photolithographic techniques and is comprised of thin-film gold electrodes with an underlying TiW adhesion layer. The system was then passivated with an oxide layer, which was etched through to define and expose the electrode active areas. Fibroblast cells (NIH-3T3) were able to grow directly onto the gold surface, and as they adhered and multiplied, the impedance of the system increased. Cells preferentially grew on the bare gold surface and not on the oxide. However, the oxide surface can be rendered biocompatible with the use of polyelectrolyte multilayers (PEMs), leading to successful measurements of cell growth with impedance spectroscopy (Fig. 1). Thus, the fabricated cell confluence detector demonstrates the ability to monitor cell adhesion and growth with impedance measurements. Future work will focus on the use of this system to monitor cytotoxic effects, of a variety of chemicals, using impedance spectroscopy to detect cell detachment from the surface.

We designed and fabricated a microchip, which enables us to study the metrology problems associated with pH determination within planar microfluidic networks, *e.g.* Lab-on-a-Chip (LOC) systems. The work was motivated by the realization that LOC systems might enjoy more widespread commercialization if reliable and accurate electronic chemical sensors are more closely integrated with the microfluidic networks. The chip comprised is 1) of an ion-sensitive field-effect transistor (ISFET) fabricated on a silicon substrate, 2) an on-chip Ag/AgCl quasi-reference electrode (RE), and 3) a microfluidic network molded in the transparent elastomer, poly(dimethylsiloxane) (PDMS) (Fig. 2). Thus, both ion-sensitive field-effect transistor (ISFET)-based and fluorescence intensity (FI)-based pH measurements were conducted simultaneously with the chip. Since two independent pH measurements are used on the same device, the mH+ chip can be used to quantitate the accuracy and precision of microfluidic pH determinations. The utility of the chip was demonstrated with comparisons of the dynamic range and flow rate dependence of the ISFET-based and FI-based pH measurements. Additionally, ISFET-based measurements clearly resolved step changes in pH as small as 0.26 pH unit in flowing solution. Sample plugs of less than 100 microliters were needed for the measurements.

A method for fabricating Ag/AgCl planar microelectrodes for microfluidic applications is presented. Micro-reference electrodes enable accurate potentiometric measurements with miniaturized chemical sensors, but such electrodes often exhibit very limited lifetimes. Our goal is to construct Ag/AgCl microelectrodes reliably with improved potential stability that are compatible with surface mounted microfluidic channels. Electrodes with geometric surface areas greater than or equal to 100 square micrometers were fabricated individually and in an array format by elec-

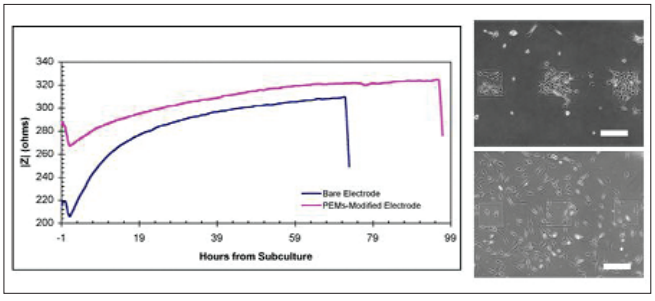

Figure 1. Magnitude of impedance of NIH-3T3 fibroblast cell growth on unmodified (blue line) and EMs-modified devices (red line) at 1000 Hz. The sharp decrease in impedance observed in both curves denote the detachment of NIH-3T3 fibroblast cells from the electrode surface after trypsin addition. (Right panel) NIH-3T3 fibroblast cells growing on unmodified gold electrodes (top) and PEMs-modified electrodes (bottom).

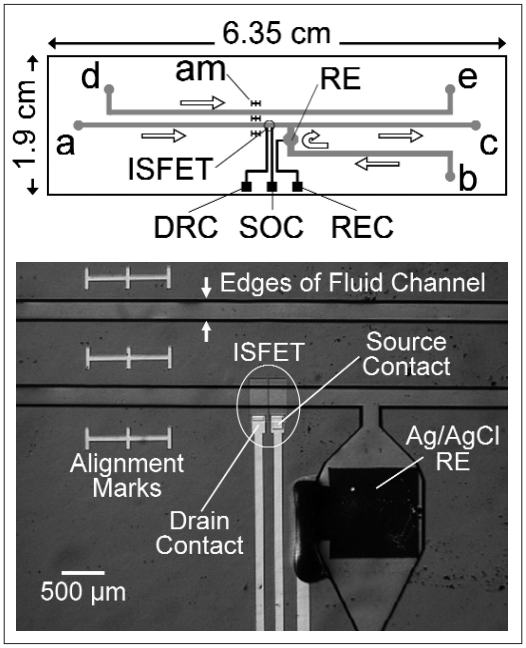

Figure 2. Schematic of mH+ layout. Overall chip dimensions are as indicated; however, other features are not shown to scale. The gray lines indicate flow channels molded into PDMS, 280 µm wide by 50 µm high. Arrows indicate the direction of fluid flow. a) test solution inlet, b) reference solution inlet, c) main outlet, d) blank inlet, e) blank outlet, am) alignment mark, RE) on-chip Ag/AgCl quasi-reference electrode, REC) reference electrode contact, DRC) electrical contact to ISFET drain, SOC) electrical contact to ISFET source. (Bottom panel) Photograph of sensing region of the mH+ device, scale as indicated. The ISFET is visible near the center of the figure, while the Ag/AgCl quasi-reference electrode appears in the lower right portion of the figure. Alignment marks and electrical contacts to the ISFET and reference electrode are made of gold.

troplating silver, greater than one micrometer thickness, onto photolithographically patterned thin-film metal electrodes (Fig. 3, left panel). The surface of the electroplated silver was chemically oxidized to silver chloride to form Ag/AgCl microreference electrodes. Characterization results showed that Ag/AgCl microelectrodes produced by this fabrication method exhibit increased stability compared with many devices previously reported. Electrochemical impedance spectroscopy allowed device specific parameters to be extracted from an equivalent circuit model, and these parameters were used to describe the performance of the microelectrodes in a microfluidic channel. Thus, stable Ag/AgCl microelectrodes, fabricated with a combination of photolithographic techniques and electroplating, were demonstrated to have utility for electrochemical analysis within microfluidic systems.

Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (µTAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). Our new approach for temperature cycling of microfluidic systems is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel (Fig. 3, right panel). This approach will have application to microwave assisted chemistries, which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibition of more uniform heating profiles. Recently, we have demonstrated, in a different microchip format, the use of microwave heating for the amplification of human DNA (PCR). We are currently working towards the integration of other processes, such as cell lysis and DNA extraction, into a microfluidic system.

We have integrated electrodes within microfluidic devices to carry out a.c. dielectrophoresis. In this trapping technique, electric fields polarize cells inducing electrostatic forces, which trap the cells against the electrode edges. We have been able to trap cells suspended from bulk cultures within microchannels when flowed past integrated, energized electrodes. We have observed that more than 85 % of cells passing the electrodes were trapped. On the other hand, when electrodes were deactivated, about 70 % of the cells were subsequently detached by solution flow. Deposition of PEMs on the electrodes renders an adhesion layer to further cell attachment. Trapping experiments carried out after PEMs were deposited over the electrodes showed that all immobilized cells remained adherent after the electrodes were deactivated. We have been using a.c. dielectrophoresis to array cells within a microfluidic channel perpendicular to flow.

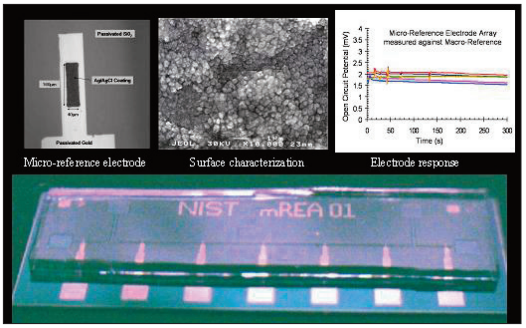

Figure 3. Photographs (left panel) of the NIST micro reference electrode array (mREA) and close-up photo of an Ag/AgCl planar microelectrode, surface, and test. The right panel is a drawing of a fluidic microwave heating assembly showing a gold coplanar transmission line patterned on glass with a poly(dimethylsiloxane) microchannel bonded over it.

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System Design and Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution poses additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing integrated circuit (IC) contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through noncontact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.

Temperature Sensor Metrology And BIST

Technical Contacts:
M. Y. Afridi
J. Geist

"For this technology (microhotplate-based gas-sensor) to be successful, temperature control is of the highest importance."

Charles J. Taylor

Goals

The purpose of this project is to develop metrology needed for microhotplate temperature sensors that are compatible with standard CMOS technologies and also provide an interface for on-chip built-in self test (BIST) for applications requiring microhotplate integrity check and self calibration. Polysilicon or aluminum layers which are readily available in standard CMOS technologies are not suitable for long-term reli-able temperature measurements due to drift in Temperature Coefficient of Resistance (TCR) value at high temperatures (250 ºC to 400 ºC). On the other hand, platinum thin film temperature sensors, which are not available in standard CMOS technologies, exhibit excellent stability over a wide temperature range, -200 to 650 ºC. There is a need to develop new post-processing steps to integrate platinum based temperature sensors into a standard CMOS microhotplate to measure microhotplate temperature, to demonstrate that the resulting temperature sensors are sufficiently stable to be accurately calibrated, and to adapt them to BIST.

Customer Needs

The customer will be any organization that requires accurate microhotplate temperatures above 250 ºC. For instance, accurate microhotplate temperature measurements are crucial for the discrimination and quantification of gas species by low-cost, microhotplate-based, metal-oxide gas sensors. The fabrication and calibration methods developed as a result of this work will be essential for the realization of many homeland security and military objectives.

Professor Charles J. Taylor of Pomona College said:

"Molecular chemisorption and chemical reactions taking place on the gas-sensor surface change the electrical properties of the sensing film, thus providing an opportunity to identify an analyte and to determine its concentration. Since chemisorption and surface reactions are tem-perature dependent, it is possible to tune sensor selectivity and sensitivity by controlling operat-ing temperature. Furthermore, using tempera-ture-programmed sensing, it is possible to iden-tify analytes based on matching data acquired at multiple temperatures to "molecular fingerprints". Without good temperature control, the matches may be ambiguous and the identity of the analyte may be lost. In addition, any studies performed where temperature is a variable in the experiment such as the deposition of materials by chemical vapor deposition onto the microhotplates, would be more difficult to reproduce without adequate temperature control."

Technical Strategy

To achieve the project goals, CMOS compatible post processing techniques will be developed to integrate different platinum based temperature sensors including resistive and platinum-rhodium thermocouples into the microhotplate structures. Also microhotplate BIST and calibration procedures will be developed and tested.

1. A series of standard CMOS microhotplates with integrated platinum temperature sensors will be developed and tested. The Microhotplate design will be compatible with BIST operation. The microhotplates will be fabricated in 1.5 μm CMOS technology through the MOSIS-AMI foundry service, post-processed in the NIST Nano-Fabrication facility, and calibrated and characterized in the EEEL SED Gas Sensor Characterization laboratory.

DELIVERABLES:

- CMOS microhotplate test structures with integrated platinum based temperature sensors. 4Q 2008

2. To develop and test BIST procedures for microhotplate integrity test and temperature calibrations.

DELIVERABLES:

- A report describing BIST performance and calibrations results for the microhotplate temperature sensors. 2Q 2009

3. An enhanced microhotplate characterization laboratory will be setup and configured to test and calibrate microhotplate temperature sensors and to measure BIST performance.

DELIVERABLES:

- A well equipped and automated laboratory setup for microhotplate characterization. 4Q 2009

4. Design analog and digital circuits to integrate control, measure, and BIST functionality for the microhotplate platform.

DELIVERABLES:

- Integrated microhotplate test structures with on-chip digital and analog electronics to control, measure, and perform BIST functionality test. 4Q 2010

Accomplishments

■ A test chip was designed and submitted to be fabricated in a standard 1.5 micron CMOS technology. The chip includes complementary temperature sensor designs to be evaluated for their performance, stability, and BIST functionality.

Publications

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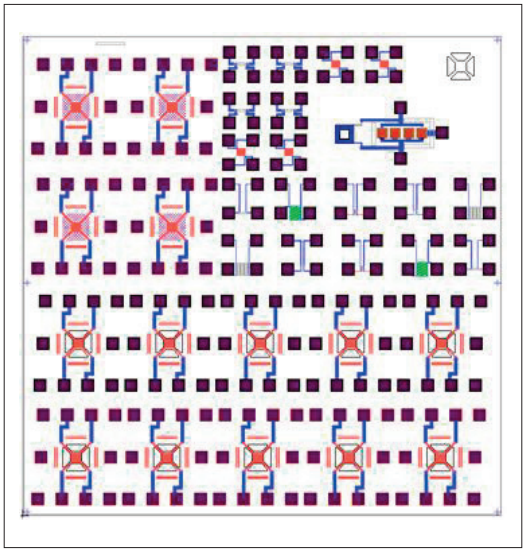

Figure 1. Layout of test structures for testing complementary approaches to microhotplate temperature sensor Built-In Self Test (BIST).

At-Speed Test of Digital Integrated Circuits

Technical Contacts:
D. F. Williams
J. Moreland
P. Kabos
P. Hale

"As electronic devices shrink into the nano-meter size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D.
Intel Corp.

Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes and developing scanning probe microscopes (SPMs) capable of precisely positioning field probes above the surface of the integrated circuit.

Customer Needs

In the device debug and characterization world, a key challenge is the development of diagnostic tools, particularly for timing information. The 2007 ITRS Metrology section points out that "Metrology was the first semiconductor technology area to work routinely in the area of nanoelectronics. This is because a variation in features size one tenth of the nominal dimension often results in significant changes in device properties." The roadmap continues "As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data." Interconnects continue to be an important aspect of the increasing density and smaller sizes of ICs. The 2007 roadmap continues "Interconnects, including all of the IC structures necessary to connect from silicon to the boards and boxes of the outside world, have become a potential performance roadblock for the continuation of the semiconductor industry on the Moore's Law curve."

With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficacy, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of DFT and test enabled diagnostics and yield learning becomes paramount (2007 ITRS Test and Test Equipment Section, page 5-6). Detecting systemic defects is one of the difficult challenges. Electrical test-based diagnostics and learning is becoming increasingly more important. Parametric related feedback is needed for: (1) device and interconnect parameters; and (2) design-process interactions. To keep pace, improvements and breakthroughs in existing tools/techniques is necessary. In-chamber (SEM) and atomic-force-microscope probing at the nanoscale are required to characterize minimum-sized transistors (4 probe points) and SRAM cells (5 or more points) at first contact level are required for circuit probing. The socket and wafer probe are also serious bandwidth bottlenecks for multi-gigahertz testing and additional R&D is needed in these areas. For key challenges the research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment. One of the challenges is that the traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40 GHz.

The critical topics in 2007 ITRS Metrology section are: the microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; dopant profile; in-situ sensors and cluster stations for process control; reference materials; correlation of physical and electrical measurements; and packaging. We are focusing our metrology methods on development of tools for materials characterization, control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. We are developing alternative scanning probing approaches that use high-impedance probes, non-contact probes, atomic-force and scanning tunneling microscopes that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implemen-

tation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit. Figure 1 shows a result of the high-speed metrology we have developed, an on-chip waveform measurement to 200 GHz.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we have constructed a universal SPM test bed for these probes. We are applying our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we plan to tie our metrology back to fully characterized electro-optic sampling measurements.

The 2007 ITRS notes that electrical test-based diagnostics and learning is becoming increasingly more important. Parametric related feedback is needed for: (1) device and interconnect parameters; and (2) design-process interactions. To keep pace, improvements and breakthroughs in existing tools/techniques is necessary. In-chamber (SEM) and atomic-force-microscope probing at the nanoscale are required to characterize minimum sized transistors (4 probe points) and SRAM cells (5 or more points) at first contact level are required for circuit probing. The socket and wafer probe are also serious bandwidth bottlenecks for multi-gigahertz testing and additional R&D is needed in these areas. For key challenges the research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment. One of the challenges is that the traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40 GHz. After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. Traceability for frequency response is provided to 110 GHz (in coax) and beyond (on wafer) through the NIST electro-optic sampling system. The 2007 ITRS roadmap points to the following three key test and measurement drivers:

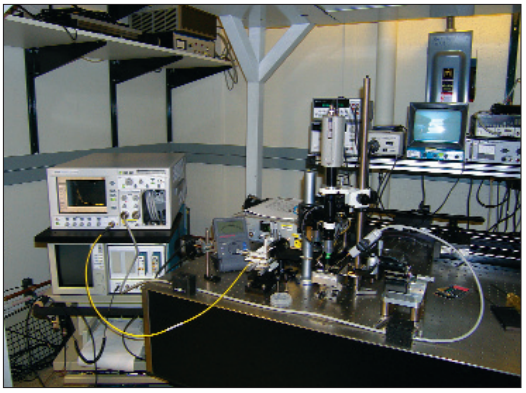

Figure 1. Three on-chip waveform measurements performed with our electro-optic sampling system.

- Increasing device interface bandwidth (# of signals and data rates)
- Increasing device integration (SoC, SiP, MCP, 3D packaging)
- Integration of emerging and non-digital CMOS technologies

Our calibration strategy is independent of the particular signals being measured and is applicable to digital, RF/microwave, and mixed signal systems, enabling the single platform measurement solutions called for in the first two of these three key drivers identified in the 2007 ITRS roadmap.

DELIVERABLES:

- Setup system and calculate known calibration waveforms with different impedance terminations. 4Q 2008
- Correlate local current measurements with the results from the pulsed source. 4Q 2008

Accomplishments

- We have demonstrated a novel frequency-domain method for measuring time-domain delay of dispersive calibration artifacts for differential delay. This frequency-domain approach can also account for pulse shape and source and load impedance effects. We have also demonstrated a

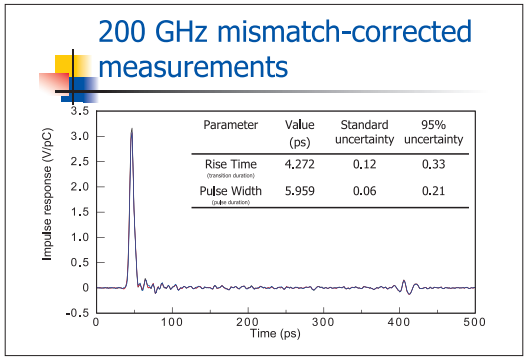

Figure 2. Measurement system used to verify the functionality of our photoconductive switches.

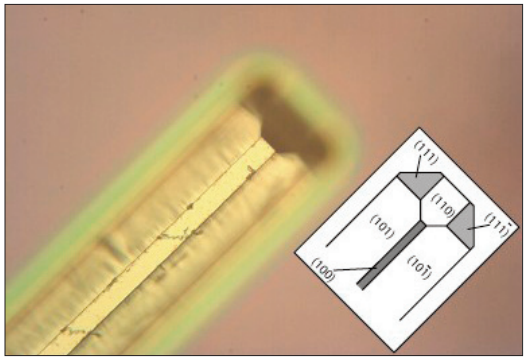

Figure 3. The Fiber-optic trench with integrated 45-degree mirror.

method to propagate uncertainty in the NIST Timebase Calibration Software through to various pulse parameters and have demonstrated differential delay calibrations of a dispersive calibration artifact with < 1 ps standard uncertainty.

■ We have developed, fabricated, and tested a noninvasive AFM scanning probe for measuring local microwave power.

■ We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements.

■ We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.

■ We have constructed an SPM universal test bed.

■ We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.

■ We have developed a procedure for testing high-impedance probes directly on our electrooptic sampling system. This system has a calibrated bandwidth of 200 GHz.

■ We have demonstrated a method for correcting oscilloscope time base jitter, drift, and distortion.

■ We have fabricated fast photoconductive switches and demonstrated a rise time of better than 5 ps, largely exceeding our goal of constructing generator chips useable to 50 GHz. We will use these to construct a portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales, Fig. 2.

■ We developed the fabrication process for creating the MEMS chips with integrated 45-degree mirrors and trenches for fiber alignment, Fig. 3.

■ We assembled the fiber optic interferometer for the measurement of the deflection of the cantilevers including the thermal feedback control.

■ We built a magneto-optic Kerr effect setup for imaging of current distributions in microwave circuits.

■ We modified a commercial AFM for measurement of mechanical resonances of micro/nano oscillators.

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Thermal Measurements and Packaging Reliability

Technical Contacts:
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J. M. Ortiz-Rodríguez
M. Hernández-Mora

Goals

Our goal is to provide the semiconductor industry with information, guidance, and tools necessary to characterize and model the behavior of features and interfaces in packaging and on-chip that are thermally stressed. Advanced temperature measurement methods are developed and transferred to industry to meet the need to characterize semiconductor device and package temperature with increased temporal and spatial resolution. Electro-thermal models and modeling methodologies are also developed and transferred to industry to meet the increased need to model the interaction of electrical and thermal behavior of the device and package.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (e.g., SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring and modeling the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs) and enables the measurement of transient current constriction failure events in RF and high power devices. This thermal imaging methodology can serve as a basis for measurement standards. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for in situ measurement of heat transfer performance degradation after various levels of thermal stress such as power cycling, thermal cycling and thermal shock.

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging and interconnects are many and display a variety of thermal responses that are not always compatible. This makes interconnect lines and package interfaces particularly vulnerable to thermomechanical fatigue failures. This project seeks to offer support through modeling and verification of the thermal performance of devices and packages and the development of new thermal measurement methods to meet the need of the semiconductor industry.

"Failures are further exacerbated by continued increases in interconnect density, number of layers, and power consumption." 2007 ITRS Interconnect, Reliability, p.41.

"Thermal-mechanical-electrical modeling for interconnections and packaging—Performance and reliability of integrated circuits is increasingly affected by interconnects and packaging. Electrical, thermal, and mechanical properties highly interact with each other and must therefore be simulated together." 2007 ITRS Modeling and Simulation, p 9.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to "Moore's Law." Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate and well-

understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

"Assembly and Packaging technologies are driven to simultaneously meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries.", 2007 ITRS Modeling and Simulation, p. 42.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: (1) predicting reliability or operating life of device, (2) measuring material/device thermal properties in situ, (3) confirming or determining the operating limits or thermal performance of a device, and (4) validating thermal models for device, chip, and system performance. Thermal measurements on small, <10 μm, structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

"Package interfaces dominate the electrical impedance, thermomechanical stress, and heat-transfer characteristics. The main opportunities are in package designs that minimize the number of interfaces and configure them to minimize electrical, thermal, and stress effects.", 2007 ITRS Emerging Research Materials, p. 35.

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs.

"Increasing power densities worsen thermal impact on reliability and performance…," 2007 ITRS Design, p. 8.

"Thermal cycling can trigger fractures that may not be foreseen".. 2007 ITRS Modeling and Simulation, p. 18.

As the power density of semiconductor devices continues to rise, modeling the interaction of electrical and thermal behavior of the device and package also increases in importance. Modeling transient heating effects has also become much more important in predicting thermal cycling effect on reliability and in understanding the impact dynamic power dissipation within devices. NIST first introduced the concept of dynamic electro-thermal semiconductor models and package thermal network component models in the early 1990's to address this need and this methodology has been used extensively by industry to model the behavior of a variety of semiconductor devices and packages.

"An increased coupling of electrical and thermal-mechanical simulation is necessary." 2007 ITRS Modeling and Simulation, p. 19.

"Simulation of heat generation and removal and thermal dissipation is even more important than for standard CMOS due to the higher power densities typically present in the wide bandgap semiconductors…", 2007 ITRS Modeling and Simulation, p. 39.

Technical Strategy

1. High speed temperature sensitive parameter (TSP) measurements are required for in situ evaluation of the heat transport through the interface of multi-layer package systems. Recently NIST developed a high speed transient thermal impedance system using a TSP for multi-chip power modules. This enables assessment of die attach and Direct Bonded Copper (DBC) isolation attach degradation after thermal cycling and thermal shock stress as well as power cycling stress. This system also enables validation of electro-thermal device models needed for electrical and thermal system design.

DELIVERABLES:

- Perform kilowatt-level power cycling on SiC power devices and modules with monitoring before and after power stress using calibrated TSP system. Perform TSP measurements on multi-chip SiC power modules to validate electro-thermal module models and to provide data that will aid in developing SiC device and package qualification standards important to other agency customers including AFRL and NASA 4Q2009

2. A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high-speed transient thermal

image measurements. NIST has modified a commercial IR system to enable measurement of high speed temperature maps of the chip surface with 1 µs temporal resolution and 15 µm spatial resolutions. The NIST system permits the measurement of the chip heat source distribution before the heat diffuses to surrounding regions and enables the measurement of transient heating events such as reduced power IC FUBs (clock gating, dynamic voltage scaling, and Vdd gating), enables the measurement of transient current constriction failure events in RF and high power devices, and measurement of current uniformity in large area power devices.

DELIVERABLES :

- Develop transient mapping stage on the 3 µm resolution commercial IR system, including hardware and software, based on the previously created 15 µm NIST high-speed transient thermal imaging system. Adapt the transient temperature acquisition procedure of the 3 um microscope to be compatible with the NIST developed high-speed imaging system. 1Q2009

3. There is a strong need to establish industry wide transient thermal measurement technique standards as described in the 2007 ITRS roadmap. NIST recently developed and tested a transient thermal calibration test structure with 1 µs temporal resolution using micro hotplates with integrated temperature sensors. The set of calibration test structures is now being expanded to develop a prototype IR transient thermal imaging calibration test chip set.

DELIVERABLES :

- Develop and apply calibrated micro- and macro-hotplate transient thermal calibration test structures to evaluate performance of NIST developed 3 µm, 1 µs high-speed transient thermal imaging system. 2Q 2009
- Develop spatial resolution calibration test structures with varying line widths down to less than 1 um. 4Q2009

4. Dynamic electro-thermal models of semiconductor packages are needed to evaluate the interaction of the electrical system with the thermal management system. NIST first introduced the concept of package and module thermal network component models in the early 1990s and has since used this methodology to develop models for several specific power module packages. Recently, the program manager and contractors of the DARPA HPE program has requested that NIST provide models for the 10 kV, 100 A SiC power models being developed by the DARPA HPE Phase 2 program (device phase) contractors so that the models can be used to design the thermal management and fault mitigation systems for the prototype future naval aircraft carrier Solid State Power Substation being developed by the DARPA HPE Phase 3 (system phase) contractor.

DELIVERABLES :

- Validate thermal model for 100 A, 10 kV SiC power modules produced during HPE Phase 3 using high-speed TSP 3Q2009.

Accomplishments

■ Development of the high-speed (1 µs) transient thermal imaging system with 15 um resolution was completed. The acquisition and data analysis capabilities of this system have been extended to include a burst method and to allow frames from different transient movies to be compared more readily. An auto-scaling capability and user definable number of frames have also been added. A thin carbon-black chip coating process was developed to improve sample emissivity without altering the chip surface thermal response time. New thermal microscope hardware has been purchased and installed to enable future upgrade of the high-speed transient thermal imaging system to 3 µm spatial resolution from its present 15 µm spatial resolution.

■ NIST developed and tested a transient thermal calibration test structure with 1 µs temporal resolution using MEMS-based microhotplates with integrated temperature sensors. This specially designed temperature-reference microhotplate structure is calibrated and used to verify the results of the transient IR thermal imaging system. Figure 1 compares the single point IR transient response with the

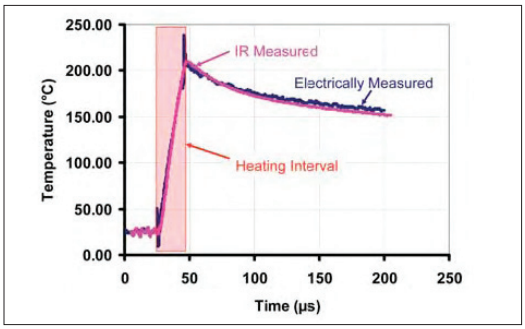

Figure 1. Microhotplate thermal response to a 20 µs heating pulse (as indicated) measured with both IR and electrical methods.

electrically measured transient response of a microhotplate structure for a 20 µs heating pulse.

■ As low-degradation rate SiC PiN (power diode made with p-type to intrinsic to n-type semiconductor junctions) diodes are beginning to emerge, the NIST transient thermal imaging system is being used to determine the current uniformity after various levels of stress up to several thousand hours of operation. Figures 2a and 2b are current uniformity images of two different SiC 10 kV, 20 A diodes operated at full rated current for 6000 hours under forward bias. The diode shown in Fig. 2a demonstrates good current uniformity after 6000 hours operation and the diode shown in Fig. 2b demonstrates highly non-uniform current conduction after 6000 hours operation (only 80 % of device is conducting). NIST has evaluated the current uniformity degradation of numerous SiC PiN diodes samples from 2005 through 2008, providing essential information resulting in the development of "degradation free" SiC power device technology. The long-term degradation process has been extended to measure SiC JBS diodes that emerged after the SiC PiN diodes with better high-power, high-frequency electrical characteristics.

■ NIST had previously developed an "in situ" method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, VGS, at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter (TSP). This TSP method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module). The high-speed TSP method was applied to compare heating response measurements with the thermal models for a commercial high power IGBT half bridge module, a commercial six-pack IGBT module, and a prototype NSF Center for Power Electronic Systems Module. Electro-thermal simulations of a full three-phase Silicon IGBT inverter have been successfully performed and compared with measured results of the power converter temperature monitors.

■ The NIST high-speed, high-current system has recently been extended to measure the transient thermal impedance of SiC MOSFETs. The transient thermal impedance data from TSP measurements is being used to validate NIST developed electro-thermal simulation model of SiC MOSFETs.

■ Electro-thermal modeling and simulation of 50 A, 10 kV multi-chip SiC power modules

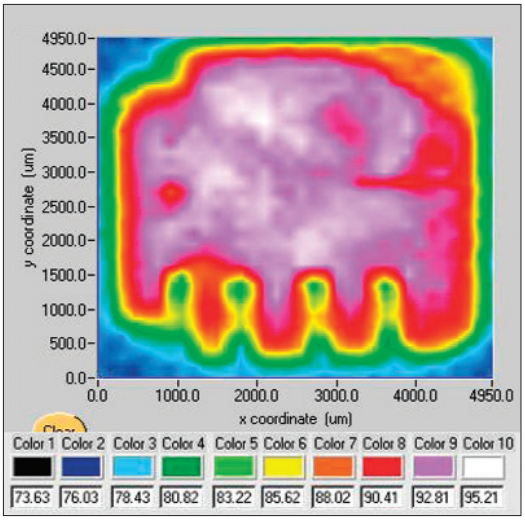

Figure 2a. SiC diode relative temperature uniformity map shows relatively uniform current conduction throughout the chip after 6000 hours stress at full current. The four green areas at the lower part of the chip are caused by wire bond shadowing of the thermal radiation.

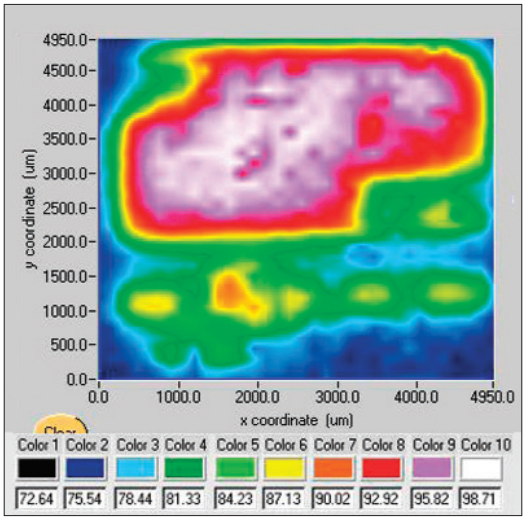

Figure 2b. Relative temperature uniformity map for a similar SiC diode shows highly non uniform current conduction after 6000 hours stress at full current. Both of these diodes are mounted on a temperaturecontrolled heatsink and the background temperature is 75 °C.

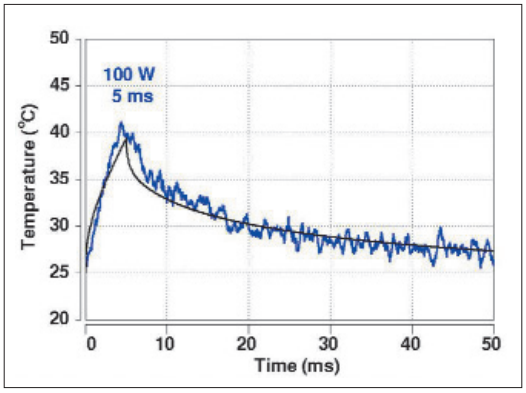

Figure 3. Thermal model validation (smooth line) versus TSP measurement (jagged line) from a 100 W, 5 ms power pulse for a SiC MOSFET package. The image shows that both heating and cooling package performances have good concordance with simulated results.

has been performed. The simulation has been used to evaluate the change in junction temperature from baseplate temperature level as the active devices are placed at different separation distances between themselves. These models and simulation have been critically important in enabling the DARPA High Power Electronics (HPE) program to optimize the first 10 kV, 100 A SiC MOSFET module ever made. The model is also being used to simulate the behavior of this module in the Solid State Power Substation being developed by the DARPA HPE program and is used in a study to assess the impact of the new technology on grid connected power converters for alternate/clean energy sources.

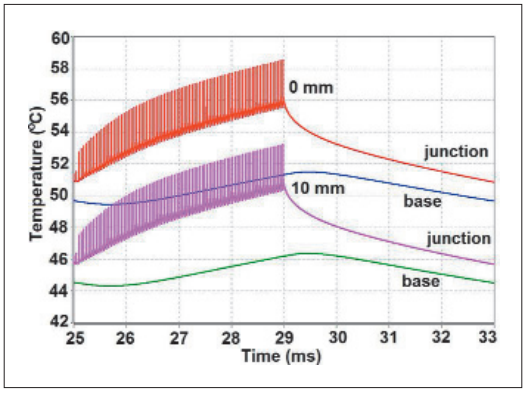

Figure 3. Thermal model validation (smooth line) versus TSP measurement (jagged line) from a 100 W, 5 ms power pulse for a SiC MOSFET package. The image shows that both heating and cooling package performances have good concordance with simulated results.

■ The hardware construction and computer interfacing for the NIST high power rapid thermal cycling/shock test systems were completed. This included necessary electronics instruments, flow controllers, high thermal impedance plumbing interfaces, and computer control of air flow rate, water flow rate, and heater power PID temperature controller. The system produces 300 °C thermal cycles with computer programmable temperature rise and fall times (as fast as 10 min rise and fall times are obtained). The rapid thermal cycling/shock test systems are currently being applied to SiC power modules developed by the DARPA HPE program where the NIST high-speed TSP and thermal imaging systems are being used to monitor thermal performance degradation. Software tools and hardware requirements for kilowatt level power cycling have also been developed.

Collaborations

University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

Virginia Tech: Jason Lai

University of Central Florida: Z. John Shen

American Competitiveness Institute (ACI), Navy ManTech Center: Barry Thaler

General Electric R&D: Ravisekhar Raju.

Powerex: Scott Leslie

Quantum Focus Instruments Corporation:

Cree Inc.

Recent Publications

J. M. Ortiz-Rodríguez, M. Hernández-Mora, T. Duong, S. G. Leslie, and A. R. Hefner, *"Thermal Network Component Models for 10 kV SiC Power Module Packages,"* to be appearing in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

T. H. Duong, J. M. Ortiz-Rodriguez, R. N. Raju, and A. R. Hefner, *"Electro-thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module,"* to be appearing in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

N. Barbosa III and A. J. Slifka, *"Spatially- and Temporally-Resolved Thermal Imaging of Cyclically Heated Interconnects by Use of Scanning Thermal Microscopy (SThM),"* submitted to Microscopy Research and Technique.

A. R. Hefner and S. Beermann-Curtin, *"Status of the DARPA WBST High Power Electronics Program in SiC Device Development and Technology Transition,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2007, March 19-22, 2007, Lake Buena Vista, FL, pp. 185-188.

M. Hernández-Mora, A. Akuffo, C. E. Hood, J. M. Ortiz-Rodríguez, and A. Hefner, *"Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability,"* 2007 IEEE Power Electronics Specialists Conference (PESC), 17-21 June, 2007, Orlando, FL, pp. 61-65.

A.R. Hefner, R. Sei-Hyung, H. Brett, D.W. Berning, C. E. Hood, J. M. Ortiz-Rodriguez, A. Rivera-Lopez, T. Duong, A. Akuffo, M. Hernández-Mora, *"Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Device,"* Proceedings of the 2006 IEEE Industry Applications Society (IAS) Annual Meeting, October 8-12, 2006, Tampa, FL, pp. 330-337.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Paper presented at the 2006 TMS Annual Meeting, April 2006.

Manufacturing Support Program

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300 mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with the International Semiconductor Industry Initiative (ISMI, a subsidiary of SEMATECH) to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain," and to provide standards for secure electronic diagnostic data and for coherent time synchronization on the factory floor.

Factory Time Synchronization Standards Development for E-Manufacturing

Technical Contacts:
J. Amelot
J. Le Guen
Y. Li

Goals

The project's objective is to facilitate the development of standards and guidelines to achieve reliable clock synchronization and time stamping capabilities for supporting present and future e-Manufacturing needs. The project aims to educate the industry about the requirements, related issues, and potential solutions in regards to distributed precision clock synchronization.

Customer Needs

Increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Advancing next-generation semiconductor manufacturing will require data to be collected and analyzed from a rising confluence of data streams, due to narrowing tolerance windows, new material introduction, and novel processing techniques. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

As 300 mm factories mature, the fabrication facilities continue to face difficult challenges in managing the increasing factory complexity, which has resulted in an:

"Explosive growth of data collection/analysis requirements driven by process and modeling needs." 2007 ITRS, Factory Integration, p. 3.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data.

"Device and process complexity make the ability to trace functional problems to specific process areas difficult." 2007 ITRS, Factory Integration, p. 4.

The quality of the data, including contextual data, impacts the ability to make optimal automated processing decisions in real-time. One aspect of data quality is the ability to acquire accurate time stamps for effectively diagnosing problems and determining other types of cause-effect relationships for Advanced Process Control (APC) applications, especially in the realm of Fault Detection Classification (FDC) and Virtual Metrology (VM).

The Equipment Data Acquisition (EDA) interface where data collection rates can increase to 10,000 data points per second, one millisecond time stamp accuracy is required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require clock synchronization of all the related local clocks in the manufacturing site including the clocks within the process and metrology tools.

Technical Strategy

Through active participation in the SEMI Data Quality Task force, this project will continue to support standards development and legacy standards updates to ensure factory equipment and equipment components can reliably and consistently report time and time-stamp data.

The first approach is to continue to be aware of the latest developments in evolving distributed clock synchronization technologies, specifically in the mainstream protocols such as IEEE 1588, *Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, and NTP, *Network Time Protocol*. The semiconductor industry factory

timing requirements have been presented to the IEEE 1588 group in order to provide input on standards requirements as version 2 of the Precision Time Protocol. Based on request from ISMI, NIST plans to document recommended methods for implementing the upcoming clock requirements.

DELIVERABLES:

- Updated ISMI *Time Synchronization Guidelines* document based on changes in NTP version 4 developments and the evolution of SEMI E148. 3Q 2008

To expedite integration of time synchronization protocols into the equipment, standards will be necessary to make the tasks as efficient as possible. The SEMI Data Quality Task Force has recently developed a new standard for defining a clock object to ensure consistent reporting of time data along with contextual information to allow the user to determine the synchronization accuracy of the time. Additionally, legacy standards need to be updated in order to leverage the new time object.

DELIVERABLES:

- Propose changes to SEMI E54 for enabling retrieval of time stamps in a consistent format with SEMI E148. 2Q 2008

Accurate time stamping requires a reliable and accurate clock synchronization methodology. Research on practical application and performance testing of the synchronization protocols would determine the impact of various computing factors *(e.g.*, CPU usage, network traffic, constraints of sensors and embedded systems, etc.) on distributed clock synchronization performance. The Engineering Research Center at the University of Michigan has been collaborating with NIST in conducting studies on the accuracies achievable with software-based time synchronization protocols in industrial networks. To fully understand the impact of data quality on automated decision-making, a distributed sensor and control environment is being developed along with an evolving factory simulation system. The work will have practical benefits in ensuring the potential solutions and new industry standards are feasible and effective in achieving accurate clock synchronization and data time stamping. Additionally, a distributed sensor and control network enables NIST to research system optimizations for effective data collection, sensor data fusion, and real-time control.

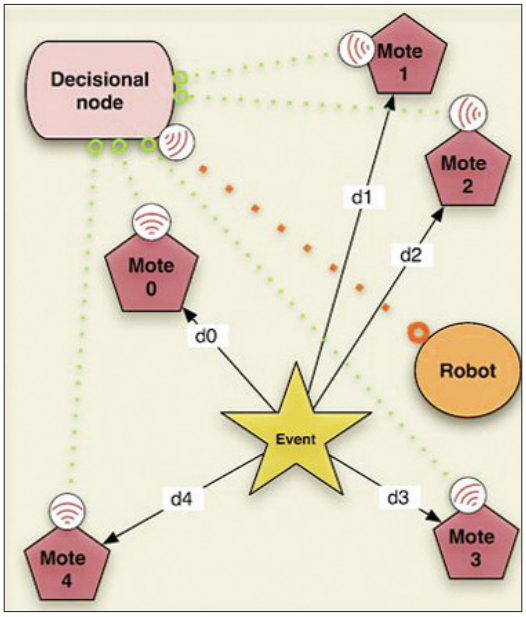

Figure 1. Conceptual design of a distributed sensor network test bed for addressing aspects of data quality and APC issues on the semiconductor factory floor.

Time Synchronization & Time-Stamping Scenario

1. *A clap is generated in the room*
2. *The motes hear the sound at different times.*
3. *Motes time-stamp and transmit data to the decisional node.*
4. *The decisional node computes the source of the sound.*
5. *The robot is driven to the sound source.*

DELIVERABLES:

- Continue to establish a hybrid factory simulation-sensor and control network environment to research the impact of the system on data quality aspects including time synchronization and time-stamping accuracy. 4Q 2008

Accomplishments

A NIST internal report (NISTIR 7184) on "Semiconductor Factory and Equipment Clock Synchronization for e-Manufacturing" was published in December 2004.

The presentation on "*Running Out of Time:* Improvements Required in Current Semiconductor and Equipment Clock Synchronization for Supporting Future Real-Time Data Collection" was given at AEC/APC Symposium in September 2004.

"*In Search of the Key to the Lock:* Clock Synchronization Requirements in Semiconductor

Manufacturing" was presented at the IEEE 1588 Conference in October 2005.

"Using Network Time Protocol (NTP): Introduction and Recommended Practices" was published as an ISMI Technical Report in February 2006.

"Legacy Standards Update: SEMI Standards Analysis to Meet Factory Time Synchronization Requirements" was presented at the SEMI Spring IEE TF meeting in March 2006.

"Time Synchronization in Manufacturing Networks" at the Network Performance Workshop, University of Michigan, April 2006.

Presented the talk on "Advancing Towards Factory-Wide Data Quality for APC Applications, AEC/APC XVIII Proceedings, Westminster, CO, September 29-October 6, 2006.

Published "Factory and Equipment Clock Synchronization and Time-Stamping Guidelines," ISMI Technology Transfer, October 20, 2006.

Presented "Time Synchronization: Leveraging Ethernet Everywhere" keynote at the Network Performance Workshop, University of Michigan, May 1, 2007.

Developed EDA Factory Data Collection Simulation software for testing data quality aspects.

SEMI E148 Specification for the Definition of Time Synchronization Method and Format

Collaborations

Harvey Wohlwend, Gino Crispieri, International SEMATECH Manufacturing Initiative

James Moyne Engineering Research Center, University of Michigan Ann Arbor

Alan Weber, Alan Weber and Associates

Ecole Supérieure d'Informatique et Applications de Lorraine

Publications

V. Anandarajah, N. Kalappa, S. Hussaini, R. Sangole, J. Baboud, Y. Li, and J. Moyne. *"Precise Time Synchronization in Semiconductor Manufacturing,"* Proceedings of the IEEE International Symposium on Precision Clock Synchronization for Measurement Control and Communication, October 1-3, 2007, Vienna, Austria.

N. Kalappa, V. Anandarajah, J. Baboud, Y. Li, and J. Moyne. *"Fab-Wide Network Time Synchronization – Simulation and Analysis,"* AEC/APC Symposium, September 15-20, 2007, Indian Wells, CA.

H. Wohlwend, Y. Li, *"New Industry Requirements for Clock Synchronization and Time Stamping,"* European AEC/APC Symposium, Mar 27-31, 2006, Aix En Provence, France.

N. Kalappa, J. Moyne, J. Parrott, Y. Li, *"Practical Aspects Impacting Time Synchronization Data Quality in Semiconductor Manufacturing,"* Proceedings of the 2006 IEEE-1588 Conference, Conference on IEEE-1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, Oct 02-04, 2006, Gaithersburg, Maryland.

J. Moyne, J. Parrott, N. Kalappa, Y. Li, *"Practical Aspects Impacting Time Synchronization Data Quality in Semiconductor Manufacturing,"* AEC/APC Symposium XVIII, Sep 30, 2006 to Oct 05, 2006, Westminster, Colorado.

E. Simmon, Y. Li, J. V. Messina, *"An External Stopwatch for Measuring the Timing of Events in a Computer or Distributed Computing Environment,"* AEC/APC Symposium XVII, Sep 24-29, 2005, Indian Wells, California.

E. Simmon, Y. Li, J. V. Messina, *"Sands of Time: An External Stopwatch for Measuring the Timing of Events in a Computer or Distributed Computing Environment,"* AEC/APC Symposium, Sep 26-29, 2005, Indian Wells, California.

Y. Li, H. Wohlwend, L. Rist, E. Simmon, *"Intricacies of Time: Demystifying Factory Clock Synchronization and Time Stamping for E-Manufacturing,"* AEC/APC Symposium, Sep 26-29, 2005, Indian Wells, California.

Y. Li, *"Using NTP: Introduction and Recommended Practices,"* ISMI Technology Transfer.

Securing E-Manufacturing

Technical Contacts:
Y. Li
E. Otema
J. Baboud
K. Brady

Goals

The project strives to employ the latest web services security technologies for mitigating increasing security risks of potential Internet-based application systems. As a proof of concept, the project aims to design a security framework enabling efficient authentication and access control to critical resources.

Customer Needs

Optimizing factory and process capabilities and efficiency will require resources to be shared among disparate partners in the engineering chain. The ability to share critical resources among disparate partners has become a priority in the International Technology Roadmap for Semiconductors (ITRS):

"Cyber security continues to remain a high priority from the factory operations perspective" 2007 ITRS , Factory Integration, p. 16.

With the convenience and economic advantages of the distributed global network necessary to realize e-Manufacturing comes the security challenges of the digital world. As data becomes readily accessible from remote locations, the semiconductor industry is facing greater obstacles in protecting its data in order to ensure their intellectual property (IP) will not be compromised. Compromised data can result in lost profits and in a period where counterfeiters of electronic components are increasingly prevalent, allow access to information to which they are not authorized.

Ensuring IP protection is critical to overall financial success in an environment where there is a significant amount of operations-level overlap. 2007 ITRS, Factory Integration, p. 17.

In addition to protecting data, the semiconductor factory must also be vigilant to protect its networked systems from viruses and similar threats, which can lead to additional equipment downtime. Security has been a significant issue in a variety of industries, particularly in healthcare and finance where date privacy is inherent to the industry; the semiconductor industry can potentially leverage the need to ensure privacy and apply similar solutions toward equipment data for protection of IP. Additionally, the web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security.

Technical Strategy

Based on the needs and priorities of industry, we will be expanding upon the security framework developed for e-Diagnostics to protect data exchange within the factory and to secure equipment from both internal and external threats. Companies have expressed the need for methods to manage security risks, but not at the expense of productivity. Therefore simplicity of use and security are the key objectives of this project.

DELIVERABLES:

- Assessment of semiconductor industry security challenges and priorities based on risk and potential costs. 2Q 2008

The web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security. The eXtensible Markup Language (XML) security suite provides a standard paradigm to manage access control in order to restrict who may and may not control the equipment remotely, encryption and signatures in order to protect the data and ensure against malicious attackers, and key management to ensure the encryption used is safe. These features work with web services transport systems such as Simple Object Access Protocol (SOAP) to further ensure the safety of the data passed in transit. Leveraging the available standards in an effective manner can serve as a potential line of defense. However, employing XML-based standards alone is not sufficient in implementing a secure framework. Security must be managed through careful interaction with factory systems, databases and networks, as well as the users accessing the factory systems.

Robust identity management, authentication, and access control of legitimate users must be in place. The system should be readily managed to accommodate dynamic security policies. Simplifying security management is a key practice in avoiding security loopholes. Therefore, in facing the proliferation of security threats and system vulnerabilities, the industry can benefit by leveraging mainstream security tools to provide a ro-

bust line of defense against potentially costly threats to intellectual property and the continuous operation of factory systems.

Lastly, the security of the system will need to be analyzed and verified. Due to the rapidly evolving nature of security attacks, it is imperative to ensure systems are not only secure against current threats, but also mitigate potential risks in the future. The project will examine the latest types of attacks on identity management and access control, and design methods to evaluate the ability of a system to mitigate such risks. The result of the project is intended to provide guidance to current industry activities and a prototype to demonstrate a security framework for managing security at various levels of factory systems from the equipment to enterprise-level systems.

DELIVERABLES:

- Design and initial development of a software-based authentication and access control framework for protecting critical factory resources. 4Q 2008

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES:

- Work with industry to create suitable data exchange standards designed to assist industry in complying with all the forthcoming environmental legislation being passed around the world. 4Q 2008

Accomplishments

E-Diagnostics Security Framework Softwareminister, Colorado.

Engineering Chain Management in the Semiconductor Industry

Technical Contacts:
J. Messina
K. Brady

Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements have led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and data exchange throughout the entire manufacturing chain (see Figure 1) will become a greater issue for realizing the semiconductor industry's requirements to reduce time, inventory, and therefore costs.

"Manufacturing knowledge and control information need to be shared as required among disparate factories" 2007 Update International Technology Roadmap for Semiconductors Factory Integration (ITRS) 2007 Update, Factory Integration, p.2.

A growing area of concern for the semiconductor industry is the growing trend towards legislation that seeks to minimize the environmental impact of manufacturing. This can range from legislation that bans the use of hazardous substances, to mandating tracking of resources (energy and water), to mandating the use of energy efficient designs. An example of this new trend is the European Union's Restriction of Hazardous Substances (RoHS) in electronics directive that seeks to reduce or eliminate six substances known to be hazardous to humans and the environment. RoHS alone will result in a massive shift in the availability of parts as some components are removed from the marketplace while others are redesigned completely to remove the banned substances. For most of these pieces of environmental legislation, companies will only be able to prove compliance through the exchange of extensive amounts of product and manufacturing data. This can only be achieved through the development of new standards that span the entire supply chain.

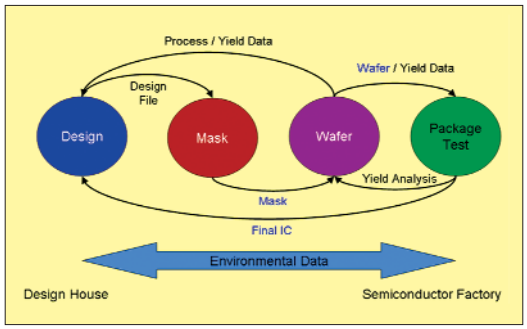

Figure 1. Engineering Chain: Semiconductor Data Exchange Needs Engineering Chain: Semiconductor Data Exchange Needs

Determining the physical/chemical, environmental, and toxicological properties of chemicals and materials as well as any reaction by-products is essential to protecting human health and the environment as well as minimizing business impacts after processes are developed and introduced into high volume manufacturing.2007 ITRS ESH, p. 1.

Finally, the semiconductor industry is also seeking to control costs and improve semiconductor yields through the development of advanced Factory Information and Control Systems (FICS). Next generation FICS are expected to be able to collect information from equipment that will enable intelligent automated decision-making concerning factory resources. (This will require data quality assurance). Materials will be processed and dispatched to equipment in a way to minimize production-equipment idle time thus maximizing factory output. In addition, FICS will allow factories to be more reconfigurable as needed even to the point of being able to modifying wafer processes on a wafer-by-wafer basis. This is even more important with factories expected to use even few total wafers with the expected transition to 450mm. Developing these FICS will require a

greater level of interoperability and data exchange within the semiconductor factory.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES:

- Chair the Product Lifecycle Information Management (PLIM) TWG of the ITRS 2008 Roadmapping Update. 4Q 2008

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI), and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project provides guidance in leveraging existing best practices from other industries and promoting collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES:

- Work with SEMI to identify standards needs for developing areas such as environmental compliance, anti-counterfeiting activities, and data quality. 4Q 2008

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development for the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES:

- Work with industry to create suitable data exchange standards designed to assist industry in complying with all the forthcoming environmental legislation being passed around the world. 4Q 2008

Accomplishments

■ In conjunction with IPC Corp., NIST developed the IPC 1752 material declaration standard that supports the exchange of RoHS environmental legislation through the engineering chain.

■ Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial has been taught as a class at both NIST and various SEMI standards workshops.

■ Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.

■ NIST co-led the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Efforts were made to determine the scope and identify the challenges of creating an effective Engineering Chain.

■ Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a fu-

ture role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Collaborations

Alan Weber, Alan Weber & Associates.

ITRS Factory Integration Technical Working Group.

SEMI.

SEMATECH.

IPC.

Publications

J. V. Messina , E. Simmon, E., K. Brady, *"Information Management for Environmental Concerns and Regulatory Requirements"* FEO Magazine, Feb 2008.

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H. Wohlwend, G. Crispieri, Y. Li, *"Advancing Towards Factory-Wide Data Quality for APC Applications,"* AEC/APC Symposium XVIII, Sep 30, 2006 to Oct 05, 2006, Westminster, Colorado.

A. Griesser, *"Ensuring High Quality Data Transfer Standards,"* AEC/APC Symposium XVI, Sep 18-24, 2004, Westminister, Colorado.

NIST/SEMATECH e-Handbook of Statistical Methods

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Goals

The goal of the *NIST/SEMATECH e-Handbook* of Statistical Methods project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the *e-Handbook* readily accessible to its target audiences in industry, including the semiconductor industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH (Fig. 1).

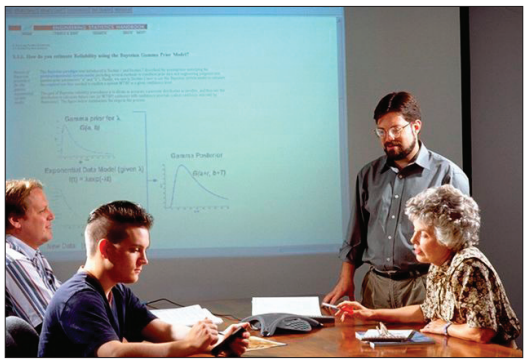

Figure 1. NIST Engineering Statistics Internet Handbook team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

Deliverables:

- Update and maintain the e-Handbook on-line, and continue to distribute the e-Handbook on CD for off-line use. 4Q 2008

Accomplishments

Since release of the final version, work has focused on publicizing the e-Handbook, responding to user feedback, and developing a compact disk version for off-line use (Fig. 2). The web version of the e-Handbook averages approximately 1 million hits per month and over 8,900 e-Handbook compact disks have been distributed to industrial, government, and academic users all over the world over the last two years. Publicity on the e-Handbook has appeared in *Science, Quality Digest, MicroMagazine.com, States News Service, National Science Digital Library Report for Math, Engineering, and Technology, and American Statistician.*

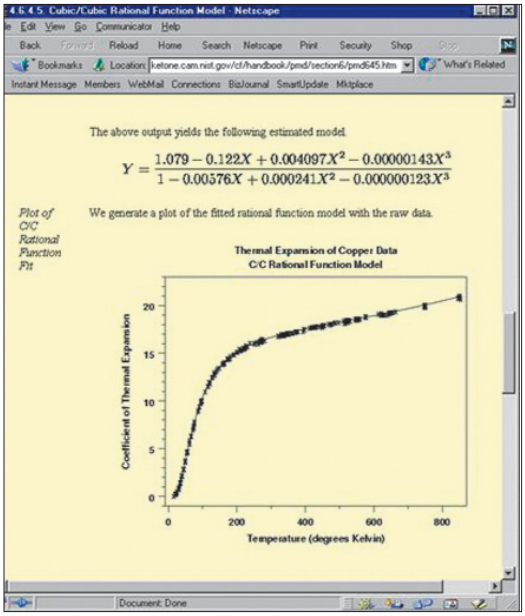

Figure 1. NIST Engineering Statistics Internet Handbook team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

The online engineering statistics handbook is very useful and I make reference to it often in my position as an R&D engineer at a medical device company.

Josh Molho, Ph.D.
Pelikan Technologies

"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc

Collaborations

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

Motorola, Pat Spagon; project planning, organization, and writing

Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.

Abbreviations and Acronyms

A.C.	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CNT	carbon nanotubes
CPU	central processing unit
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
D.C.	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy

Abbreviations and Acronyms (cont'd)

EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IETS	Inelastic Electron Tunneling Spectroscopy
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	local oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPU	microprocessor unit
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy

OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	random-access memory
RGA	residual gas analyzer
RLGC	distributed resistance, inductance, conductance, and capacitance
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-a-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
STM	scanning tunneling microscope
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectometry

Technical Contacts

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