Three-Dimensionally Structured Thin Film Heterojunction Photovoltaics on Interdigitated Back-Contacts

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Fabrication and properties of three-dimensionally structured back-contact heterojunction solar cells are described. A variety of devices are explored, all of which were fabricated by electrochemical deposition of a semiconducting material on one of two interdigitated electrodes in a comb structure followed by deposition of a second semiconducting material over the entire surface, including over both the bare and coated electrodes in the comb. The performance of fabricated devices is described and interpreted using a simplified model of the device geometry, light absorption and carrier transport. The results demonstrate that the processes and structures are amenable to a broad array of materials and deposition techniques, providing well-defined geometries amenable to fabrication and study of 3-D structured photovoltaic devices.

Introduction

Photovoltaic (PV) devices convert sunlight into electrical current through the conjunction of n-type and p-type materials to separate electron-hole pairs created during absorption of light. "First generation" devices are based on crystalline silicon, an indirect bandgap material. "Second generation" devices are based on thin films of direct bandgap materials. "Third generation" devices are anticipated to utilize three-dimensional micro- or nano-scale structures to lead to higher efficiency and/or lower cost.

Materials and structures proposed for both second and third generation devices are discussed in a number of review articles (1-3). Second generation devices based on thin films of cadmium telluride (CdTe) with cadmium sulfide (CdS) as well as copper indium gallium diselenide (CIGS) with CdS are already being sold commercially. Third generation devices utilizing nanoscale features such as semiconductor nanowires (4,5), nanorods in polymers (6) and pillars in inorganic materials, including some with the CdS and CdTe (7,8) system found commercially in thin film devices, are being examined at

the research level. With only one exception (9), all disclosed geometries for both second and third generation devices utilize a contact geometry whereby holes and electrons are collected on opposite surfaces of the device, i.e., with collection of one charge carrier on the film surface facing the sun. The structures required for current collection on the irradiated side, typically a transparent conductor such as indium-tin-oxide and metal lines, block a fraction of the incoming light, decreasing device performance even as they add to processing complexity and cost.

Back contact geometries, in which both electrons and holes are collected on the back surface, do not have metal wires or transparent conductors blocking incoming light. Because of the associated potential for improved conversion efficiency, silicon-based devices with a variety of back contact geometries have been studied for more than three decades (10-16). Such devices typically have an the electrode pitch of the same order as the thickness of the semiconductor (14,17,18).

A process whereby back contact photovoltaic devices were created by electrodepositing CdTe on an insulating substrate that had been previously patterned with two interdigitated electrodes in the "comb" geometry used by the microelectronics industry (Fig. 1) was recently detailed (9). To summarize, first n-type CdTe was deposited on one electrode in the interdigitated structure while p-type material was deposited on the other electrode by the application of different deposition potentials to the electrodes. Prior to impingement of the deposits on the interdigitated wires of the two electrodes the deposition potentials were adjusted so that p-type CdTe began depositing on both electrodes, and deposition was continued through impingement of the two deposits. CdTe homojunction devices with back contacts, the contacts being the same two interdigitated electrodes used for the deposition, were thus fabricated in a single electrolyte. The approach was noted to be amenable to study and optimization of a wide range of materials and three-dimensionally patterned structures specifically including heterojunction devices.
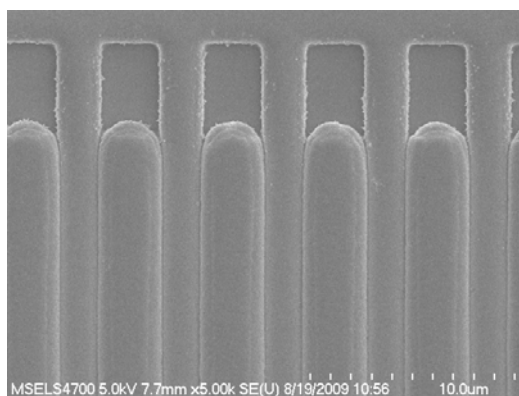

Figure 1: The interdigitated device geometry is captured in this planview scanning electron microscope image of a homojunction device: CdTe deposited on one electrode, with contact pad visible at the top of the image and five connected wires, making contact to the CdTe deposited on five interdigitated wires coming from the second electrode, contact pad not visible below the bottom of the image. The interdigitated wires are used

for electrodeposition as well as current extraction, the two contact pads allowing convenient electrical contact for processing and study to the two sets of wires that underlie the active, interdigitated portion of the device.

This study describes implementation of a process for fabrication of heterojunction photovoltaic devices with the same backside contacts based on the interdigitated electrode geometry. First, a semiconducting material is electrodeposited on one of the electrodes. A second semiconducting material is subsequently deposited to cover the entire surface. Structures with this second semiconductor were deposited by means including chemical bath deposition (CBD), sputter deposition and sol-gel processing. In all cases, formation of a deposit that bridges both electrodes creates optically active device with controlled 3-D patterning and dimensions and back contacts. Like planar thin film devices based on the same materials and deposition processes, subsequent annealing or other processing is sometimes required to achieve reasonable performance.

Electrodeposition

Patterned Substrates

The two interdigitated electrodes on each substrate each include on the order of one thousand parallel wires (lines), as well as a rectangular contact pad connecting them, all lithographically patterned on thermally oxidized silicon. The electrodes on the specimens described here are gold and/or platinum, with individual wires on the order of 1 μm wide and from 50 nm to 200 nm tall, including a 5 nm titanium adhesion layer. The active area of each device, i.e., the region containing the interdigitated wires, covers an area four or five millimeters on a side, so that the lines are all four or five millimeters long, respectively. The pitch of adjacent lines ranges from 2 μm (i.e., 4 μm spacing between lines on the same electrode) to 4 μm (i.e., 8 μm spacing between lines on the same electrode). During electrodeposition the substrates are held in a custom-made rotating holder enabling independent control of the potentials on the two electrodes.

CdTe Electrodeposition

Cadmium telluride (CdTe) was electrodeposited using a codeposition technique based on the enthalpies of reaction of the compounds (19,20) that has been used to deposit a number of stoichiometric compound semiconductors (21,22). For CdTe in particular, the deposition potential impacts both the deposition rate and the electrical properties of the deposited material (23-25).

As in the study on backside contacted homojunction devices (9), the electrolyte contained Cd^{+2} and Te^{+4} ions. The 0.1 mol/L Cd^{+2} was obtained through addition of $3(CdSO_4) \cdot 8H_2O$ (99.999% by mass) to 18 MΩ·cm water. The Te^{+4} concentration in the electrolyte is estimated from the solution pH and temperature to range from ≈ 0.1 mmol/L and up based on saturation with TeO_2 powder (99.999% by mass); a solution pH of 2 was obtained through addition of sulfuric acid (Environmental Grade Plus 93 % to

98 % assay - Alfa Aesar[1]) and deposition temperatures ranged between 60 ºC and 85 ºC. Depositions were conducted in a cell holding 100 mL of solution and having ports for a custom made rotating substrate holder providing independent control of the potentials on two electrodes, a platinum counter electrode, a reference electrode and an ultra-high-purity argon gas sparge line that ran continuously during and between depositions to remove dissolved oxygen. Specimens were rotated at fixed rates to control hydrodynamics. Additional details can be found in Ref. 9.

Reference electrodes included mercury/mercurous-sulfate in saturated potassium sulfate (SSE) and cadmium (99.999 mass %) 2.0 mm diameter wire (99.998 mass % on a metals basis) in TeO_2-free, Cd electrolyte (Cd/CdS). Measurements indicated a stable 1.070 ± 0.001 V difference between the Cd/CdS and SSE reference electrodes (the latter being more negative). All electrodeposition potentials (V) in this work are indicated relative to the Cd/CdS reference electrode.

Heterojunction Devices

CdTe/ITO Heterojunction Devices

Figure 2 shows examples of heterojunction devices fabricated by electrodepositing CdTe on one electrode of an interdigitated electrode pair then sputter-depositing indium-tin-oxide (ITO) over the entire surface. The ITO, a tin-doped indium oxide that is a solid solution of indium (III) oxide (In_2O_3) and tin (IV) oxide (SnO_2) having 90% In_2O_3 and 10% SnO_2 by mass, is typically used as a transparent conducting oxide. The ITO was deposited in an RF sputtering system with base pressure of 6.5×10^{-5} Pa (5×10^{-7} Torr). Devices, each with CdTe already on one of their two Pt electrodes, were ramped to the indicated deposition temperature over 10 min and then maintained at temperature for 10 min prior to ITO deposition. Deposition was conducted under argon and oxygen gas flows of 50 standard cubic centimeters per minute (sccm) and 10 sccm, respectively, with an associated deposition pressure of 0.65 Pa (5×10^{-3} Torr). The RF deposition power of 300 W, with associated DC self-bias of 347 V, resulted in a deposition rate of ≈ 4 nm/min. The Pt electrodes, the electrodeposited CdTe on one electrode and the sputter deposited indium-tin-oxide (ITO) over the entire surface are evident in Fig. 2a,b. The CdTe retains a fine grained microstructure, distinct from the columnar ITO layer, ever after the 325 º C ITO deposition. As shown in Fig. 2c,d, further annealing for 10 min at 400 ºC of a similar device that had been dipped in a $CdCl_2$ solution leads to a markedly increased CdTe grainsize. Previous studies have described the impact of annealing on the microstructure and optical properties of CdTe (9, 26,27), particularly when the material is annealed in the presence of $CdCl_2$.

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[1] Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.
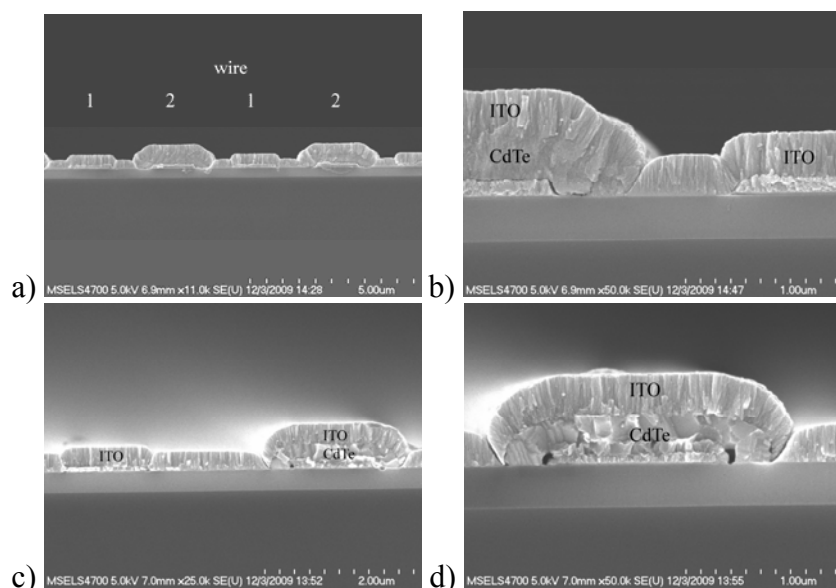
Figure 2: Cross-section views of CdTe/ITO devices fabricated on platinum electrodes. A 2 µm pitch device with electrodeposited CdTe on one electrode (25 s at -0.02 V then 975 s at +0.02 V, 70 ºC and 60 rpm) and ITO sputter deposited at 325 ºC over the entire surface: (a) two wires with CdTe/ITO and two with ITO, (b) higher magnification view of parts of one wire with CdTe/ITO and one wire with ITO. A 4 µm device with electrodeposited CdTe on one electrode (1000 s at +0.02 V, 70 ºC and 60 rpm) and ITO deposited over the entire surface at 300 ºC that was annealed in CdCl$_2$ vapor for 10 min at 400 º C: (c) one electrode with CdTe/ITO and one with ITO, (d) a higher magnification view of one wire with CdTe/ITO. The CdTe grainsize is substantially larger after the anneal in CdCl$_2$; voids on either side of the wire possibly arise from densification of the CdTe.

Figure 3 shows the optical response characterized by external quantum efficiency (EQE) of the specimen shown in Fig. 2c,d while it was still in its as-deposited state (details of the EQE measurements can be found in Ref. 9). The optical response is consistent with the CdTe optical bandgap at approximately 829 nm. Significantly lower response, and thus reduced density of defect states, is exhibited at longer wavelengths as compared to interdigitated back-contact CdTe homojunction devices that did not experience such elevated temperature processing (9). Decreased EQE at shorter wavelengths is consistent with absorbtion of the light in the ITO, its bandgap (28,29) indicated, before it reaches the CdTe. The annealed specimen in Fig. 2c,d exhibited no optical response. The failure is presumed to result from the cracks evident where the ITO goes from the field onto the bare and CdTe-coated Pt electrodes; the seams underlying the failure locations are a byproduct of sputter-deposition on nonplanar surfaces.
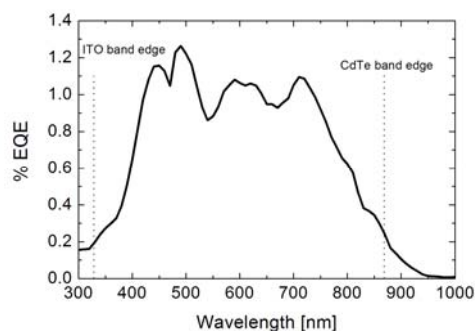
Figure 3: The optical response, as assessed by the external quantum efficiency, of the as-deposited CdTe/ITO device that is pictured in its annealed state in Fig. 2c,d; wavelengths where absorption and photocurrent is anticipated for the different materials, based on bulk properties, are indicated. The gradual increase at wavelengths smaller than the 829 nm bandgap of bulk CdTe likely reflects wavelength dependent absorption in the thin CdTe[8]. The oscillations for shorter wavelengths suggest the results of modulated absorption in the CdTe associated with optical interference within the smooth surfaced, planar ITO layer.

<u>CdTe/CdS Heterojunction Devices</u>

   Figure 4 shows examples of heterojunction devices fabricated by CdTe electrodeposition on one electrode followed by CBD of CdS by a process described previously (30) and then annealed for 20 min at 350 °C. Examples are shown of devices with Au electrodes (Fig. 4a) and with Pt electrodes (Fig. 4b). The CdTe deposits (on every other wire) are visible in the cleaved cross-section views as is the overlayer of CdS; the CdS deposits include a continuous film as well as larger particles nucleated homogenously in the electrolyte and subsequently incorporated in the deposit. The microstructures of the annealed CdTe deposits differ substantially from each other. Specifically, the deposit on the Au electrodes has a visual appearance little different from as-deposited CdTe deposits (see Ref. 9) while the deposit on the Pt electrode exhibits substantial grain growth that evidently originated at the Pt electrode.
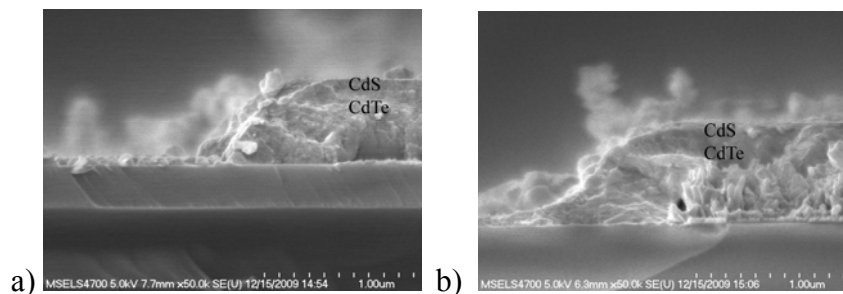

Figure 4: Cross-section views of cleaved 4 μm pitch CdTe/CdS heterojunction devices. (a) The left side of an electrode with CdTe/CdS. The device has Au electrodes, CdTe electrodeposited on one electrode (1800 s at +0.02 V, in electrolyte also containing 0.5 μmol/L In$_2$SO$_4$ as an indium dopant, 60 ºC and 60 rpm) followed by CdS chemical bath

deposition over the entire surface then annealing at 350 °C for 20 min. (b) The left side of an electrode with CdTe/CdS. Grain growth in the annealed CdTe is evident, the grains growing up from the Pt electrode; a void apparently associated with the densification is visible at the edge of the wire. The device has Pt electrodes, CdTe electrodeposited on one electrode (3600 s at +0.02 V, 85 ºC and 60 rpm) followed by CdS chemical bath deposition then annealing at 350 °C for 20 min. The continuous overlayer of CdS is evident in both specimens, as are larger particles that homogeneously nucleated in the electrolyte and subsequently incorporated during the deposition.

The optical performance of the as-deposited and annealed devices on the different electrode metals is shown in Fig. 5. The specimens exhibit different behaviors in the as-deposited state despite having similar thicknesses of CdTe and CdS: the specimen with the Au electrode in the CdTe has a higher response at wavelengths where only CdTe absorbs while the specimen with the Pt electrode has a higher response where the CdS (also) absorbs. Annealing for 20 min at 350 °C leads to significant changes in the responses from both specimens; the maximum EQE increases by an order of magnitude and the spectral ranges with the highest values switch after annealing. Specifically, the EQE of the specimen with Pt electrodes increases by an order of magnitude at wavelengths absorbed by the CdTe, with comparatively little change at wavelengths where CdS also absorbs. The EQE of the specimen with Au electrodes increases by an order of magnitude at wavelengths absorbed by the CdS (and CdTe); the response at wavelengths where only CdTe absorbs actually decreases.
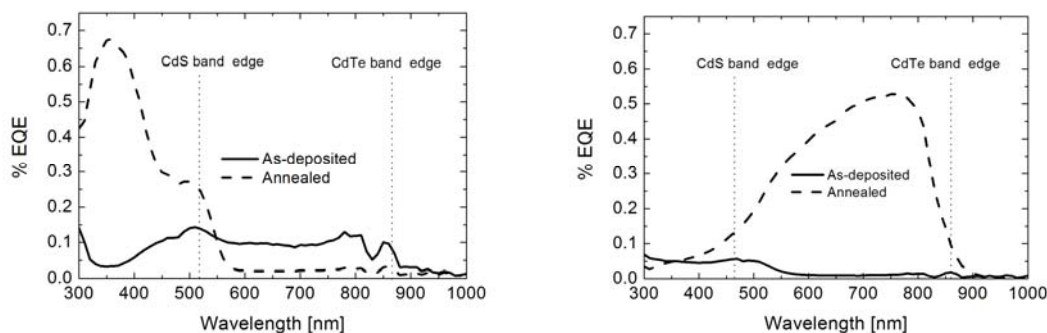
a)   b)

Figure 5: EQE results for CdTe/CdS heterojunction devices shown in Fig. 4. (a) Device fabricated on Au electrodes with data for as-deposited condition and annealed at 350 °C for 20 min (Fig. 4a). (b) Devices fabricated on Pt electrodes for as-deposited condition and annealed at 350 °C for 20 min (Fig. 4b). Wavelengths where absorption/photocurrent is anticipated for the different materials, based on bulk properties, are indicated.

CdTe/TiO$_2$ Heterojunction Devices

Figure 6 shows an example of a heterojunction device fabricated by CdTe electrodeposition on one of the Pt electrodes followed by sol-gel deposition of n-type TiO$_x$ (1 < x < 2) over the entire device; the CdTe deposit, only a few 10's of nanometers thick, is nearly indistinguishable from the equally thin TiO$_x$ surrounding the approximately 300 nm tall Pt electrodes. Processing of this specimen included sol-gel

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application, specimen spinning at 2000 rpm to distribute the solution and annealing in air at 400 ºC for 15 min. The sol-gel process used has been described previously (31). The performance of the device is shown in Fig. 7.
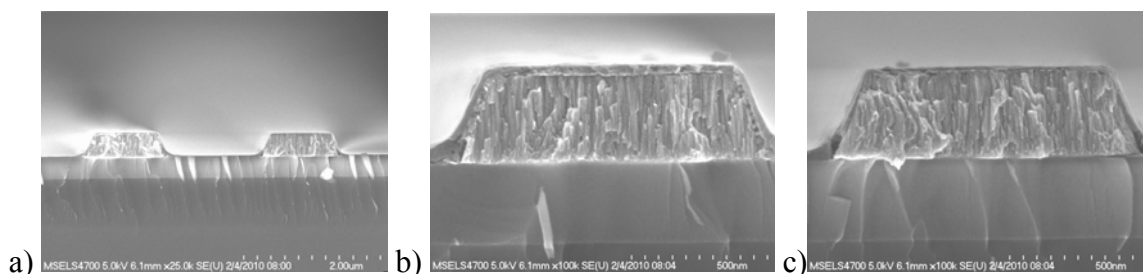

Figure 6: Cross-section views of a CdTe/TiO$_x$ heterojunction device fabricated on approximately 300 nm tall platinum electrodes: (a) one wire with with CdTe/TiO$_x$ and one wire with TiO$_x$, (b) one wire with CdTe/TiO$_x$ and (c) one wire with TiO$_x$. Both the CdTe and TiOx, each only a few 10's of nanometers thick, appear as a thin layer surrounding the columnar grained Pt electrodes. Device fabricated on Pt electrodes including anneal at 400 °C for 15 min.
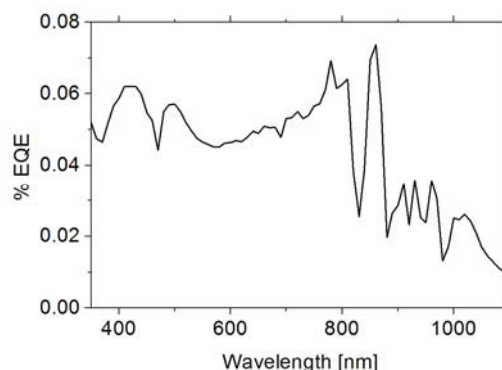

Figure 7: EQE results for the CdTe/ TiO$_x$ heterojunction device shown in Fig. 6. The band edge of TiO$_x$ is below the range of wavelengths shown; the response is consistent with the extremely thin CdTe.

Modeling

The optical responses of these 3D devices, as any photovoltaic devices, are dictated by the interplay between optical characteristics, which determine reflection of light from the surface and absorption of light within the film, and electrical characteristics, which determine separation of carriers at the junction and recombination of carriers in the bulk and at the interfaces. The impacts of these factors are dictated by device geometry and are accentuated in the 3D geometries presented here. Independent control over device pitch, layer thicknesses, and contact heights opens the possibility of optimizing the relative contributions of optical absorption, bulk mobility, surface recombination, and contact

quality. Previous simulations of interdigitated and related PV structures have focused on much large dimensions in Si (32) or have required front contacts for current collection (17,33).

Figure 8 shows predicted performance of CdTe homojunction (p-type and n-type CdTe) devices with varying dimensions. The model code implemented with the FiPy partial differential equation solver (34) simultaneously solves Poisson's equation and drift-diffusion equations for the holes and electrons. Except as given here, materials parameters are taken from Ref. 35. Both p- and n-type dopant densities are 10^{-13} cm^{-3}. The Shockly-Read-Hall recombination lifetime is 10^{-12} s.

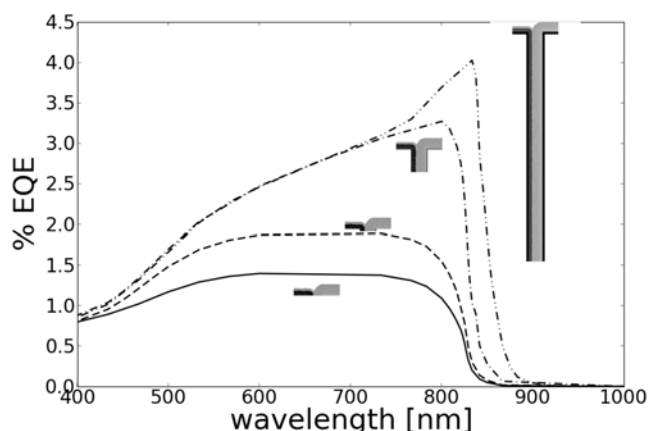Figure 8: Model predictions for EQE of CdTe homojunction devices show the impact of varying the height of idealized rectangular electrodes: 0.01 µm, 0.1 µm, 1 µm, and 10 µm. Electrode pitch is fixed at 2 µm and line width is 1.3 µm, with 0.2 µm n-type CdTe and 0.1 µm p-type CdTe conformally placed around one electrode and 0.5 µm p-type CdTe conformally placed around the second electrode.

The impact of the wavelength-dependent length for light absorption and recombination within the bulk of the devices leads to predictions of clear dimensional dependent performance. Substantial improvement in efficiency with electrode height is apparent, although it is also clear that excessive height is of little benefit. Inclusion of significant recombination at interfaces (not done here) would lead to different optimum geometries and performance. In addition, these simulations are for perfectly ohmic contacts; Schottky barriers are very likely a major issue for the heterojunction devices described in this work with their identical metals for the electrodes contacting both n-type and p-type materials.

Discussion

The periodic structure of the EQE for the CdTe/ITO device (Fig. 3) is attributed to interference of the light between the top and bottom surfaces of the ITO. The device response for wavelengths longer than $\approx$ 400 nm is derived entirely from absorption of

light by the CdTe. As per the corresponding sample images in Fig. 2c,d, the CdTe covers only approximately one-quarter of the surface and is only ≈ 200 nm thick, an order of magnitude thinner than typical planar CdTe devices; the EQE of a device with ITO on one electrode and thicker CdTe over the entire surface might reasonably be expected to exhibit at least a factor of four improvement in performance over this spectral range. Were failure at the seams in the ITO avoided, the 400 °C anneal would also be expected to improve performance.

With regard to the CdTe/CdS specimens it should be noted that electrodeposited CdTe is anticipated to be n-type as-deposited for the 20 mV electrodeposition potential used for these devices, converting to p-type upon annealing (24,25). The In^{-3} dopant in the electrolyte used for deposition of the CdTe on the Au-electrode specimen has been said to yield n-type annealed material, effectively preventing this type conversion (36,37). This type difference might underlie the very different spectral responses of the two CdTe/CdS devices that is evident particularly after annealing. The increased grain size of approximately half the CdTe in the annealed Pt-electrode device (Fig. 4b) offers another explanation for the increased EQE of the Pt device in the spectral range where only CdTe absorbs (21), while excessive Au diffusion into the CdTe in the other device might underlie its poor performance in this spectral range. While the origins of the different behaviors remain to be determined, it is clear from comparison of the devices in Figs. 2 and 4 that the CdTe grain size in both CdTe/CdS devices remains well below what is obtained when annealed at the higher, more typical, temperature.

The approximately 500 nm thick CdTe in the CdTe/CdS devices also covers approximately one-quarter of the surface area, being electrodeposited on only one electrode in these 4 μm pitch devices. In addition, device operation requires electrical conduction through several micrometers of only the ≈ 100 nm thick CdS deposit between the bare and CdTe-coated wires. Devices with CdS on one electrode and thicker CdTe over the entire surface might reasonably be expected to exhibit at least a factor of four improvement in performance over the CdTe spectral range. While not pursued here, it is worth noting that such a device might be fabricated by electrodepositing CdS on one electrode using approaches that have previously been used to electrodeposit CdS on planar substrates (38-40) and then depositing CdTe over the entire surface.

The response of the $CdTe/TiO_x$ specimen at wavelengths below the CdTe band edge is lower than those of the other devices, consistent with the very thin CdTe.

Conclusions

This paper describes heterojunction, photovoltaic devices fabricated by electrodeposition of one semiconductor on one electrode of two interdigitated electrodes followed by deposition of a second semiconductor by any of a variety of techniques to cover the entire device surface. The interdigitated electrodes are used both for deposition of the semiconductor and as backside contacts for carrier collection during operation of

the fabricated devices. The geometry and general process provide a simple, highly versatile means of creating three-dimensionally patterned photovoltaic devices.

The geometry and general process have several positive features: both contacts are created in a single lithography process; a wide variety of materials and deposition techniques are possible; there are no front contacts or transparent conductor that block incoming light; a nonplanar light-trapping surface geometry can be created by the deposition without additional processing; alignment of the materials to the appropriate electrodes is automatic and complete; 3-D geometries can be controlled; and modification of one or both electrodes can be accomplished through low cost electrochemical processing. A limitation of the geometry and process is the presence of both electrodes during any high temperature processing. Improving performance through the use of different contact metallizations for the two electrodes remains to be addressed for the devices described herein.

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