Efficiency enhancement of copper contaminated radial p–n junction solar cells

Akram Boukai[1], Paul Haney[2], Aaron Katzenmeyer[3], Gregg M. Gallatin[2], A. Alec Talin[2], Peidong Yang[4]

[1] University of Michigan, Ann Arbor, MI; [2]Center for Nanoscale Science and Technology, NIST, Gaithersburg, MD; [3]Sandia National Laboratories, Livermore, CA; [4]University of California, Berkeley, CA;

A significant fraction of the cost of a planar p-n junction silicon solar cell stems from the silicon purification process.[1] Eliminating the purification step would decrease the cost, yet also decrease the solar cell efficiency significantly. Here, we have developed an alternative geometry− a radial p-n junction− different from that of a typical planar p-n junction[2, 3]. Radial p-n junctions have been predicted theoretically to have larger efficiencies than their planar counterparts due to a decrease in carrier collection length relative to carrier diffusion length.[4] Radial p-n junctions studied here consist of micron-scale to nano-scale diameter holes etched into a copper contaminated silicon wafer using standard semiconductor fabrication steps. Radial p-n junctions contaminated with copper impurities show roughly a two times increase in efficiency than similarly contaminated planar p-n junction solar cells; however the enhancement is a strong function of the radial junction pitch, with maximum enhancement occurring for a pitch that is twice the carrier diffusion length.

Solar cells are attractive electric power sources since they are a form of renewable energy. The most common material used in solar cells is silicon. Silicon accounts for more than 90 % of the solar cell market.[5] Also, silicon is non-toxic and earth abundant. Crystalline silicon solar cells have achieved efficiencies approaching 25 % in the laboratory and 20 % commercially.[6] Currently, however, the US receives less than 1 % of its electrical power from solar cells.[5] The reason is that crystalline silicon solar cell manufacture and installation remains prohibitively expensive. One of the reasons for the high cost of crystalline silicon is the expense required to purify metallurgical-grade silicon (99 % pure) to solar-grade silicon (99.99999 % pure). The purification process accounts for a one hundred-fold increase in the material cost.[1] If solar cells are to become commercially competitive, the ultimate goal is to achieve a cost to power ratio under one dollar per watt.

One strategy that would help achieve this goal would be to manufacture radial p-n junction solar cells from metallurgical-grade silicon (MGS) or upgraded-MGS. MGS is the raw, unpurified silicon reduced from quartz in an arc-furnace. Its cost basis is roughly one dollar per kg, making it almost one-hundred times less expensive than solar-grade silicon.[1] Metallurgical-grade silicon contains many metal impurities such as Fe, Al, Cu, Ti, etc.[1] Some impurities are not uniformly distributed but tend to form metal-silicide particles, especially transition metal impurities[7]. Many of the impurities in metallurgical-grade silicon are deep level traps.[8] Consequently, metallurgical grade silicon solar cells suffer high recombination rates, which leads to dramatically reduced efficiency. Past studies have shown the detrimental effects of individual metal impurities on the efficiency of silicon solar cells.[9] All the impurities studied degraded the efficiency by decreasing the minority-carrier diffusion length. Typical diffusion length values are smaller than 10 μm for large impurity concentrations > $1x10^{16}$ cm^{-3}.[10]

Recent theoretical studies indicate that changing a planar p-n junction geometry to a radial p-n junction geometry may allow for high efficiencies for solar cells with small diffusion lengths.[4] In a typical planar p-n junction solar cell, light absorption is in the same direction as carrier collection. Photo-generated electron-hole pairs outside of the p-n junction are collected only if they are within a diffusion length away from the junction. This is because the diffusion length sets the average distance an electron-hole pair may travel before recombination. Recombination results in a loss of the electron-hole pair and thus no current production. Therefore, large diffusion lengths necessitate the use of high purity silicon materials so that trap densities are low. Minority-carrier diffusion lengths of several hundreds of microns in solar-grade silicon are typical.[11]

The key feature of radial p-n junctions is that carrier collection is to a significant extent orthogonal to light collection. This means that shorter carrier collection distances (< 10 μm) are possible. Therefore, as light is absorbed throughout the entire cell thickness, the carriers have a much shorter collection pathway to traverse before recombination can occur.[4] Radial p-n junctions can be fabricated using any rod-like structure. The diffusion length, $L = \sqrt{D\tau}$, where τ is the recombination lifetime and D is the diffusion constant, limits the radius of the "rods". Therefore, for small diffusion lengths, < 10 μm, micro- to nanostructures are desirable. The recombination lifetime is inversely proportional to the trap density. In high-purity silicon wafers with a trap density $<10^{14}$ cm^{-3}, τ is 1 μs or longer, which corresponds to a diffusion length from hundreds of micrometers to several millimeters long. However, in silicon with trap densities on the order of 10^{18} cm^{-3}, we expect to have diffusion lengths of 100 nm to 1 μm and indeed as discussed below, fitting our I-V data to a model of the device yields diffusion lengths on this order.

In this work, we have used copper contaminated silicon to investigate the potential advantages of radial p-n junctions over their planar counterparts. Copper is chosen because it easily diffuses through silicon and is a constituent in MGS.[12, 13] Copper can diffuse through a 500 μm thick silicon wafer in 14 hours at room temperature since its diffusion coefficient is 2.8×10^{-7} cm^2/s.[12] Copper is known to degrade the efficiency of silicon solar cells at concentrations above 10^{16} cm^{-3}.[10, 14, 15]

Boron doped (p-type) silicon wafers with resistivity of 5-10 Ω cm were cleaned in a piranha solution for 10 minutes. The back surface of the wafer was first coated with 1 μm of Al by sputter deposition. The Al dopes the back surface p-type through a subsequent high temperature anneal at 850 °C in N_2 for 90 min. A thin layer (~75 nm) of copper was subsequently sputtered onto the top polished surface. Afterwards, the copper diffused through the silicon wafer through a high-temperature anneal (950 °C) in N_2 for 5 hr. The Al was deposited first to minimize out-diffusion of copper.[12] After annealing, the wafer was rapidly cooled and then placed into a solution of copper etchant consisting of $FeCl_3$ and water. This step removed any residual copper on the surface and the polished surface of the wafer was recovered.

Secondary Ion Mass Spectroscopy (SIMS) studies confirmed that the silicon wafer was contaminated with copper impurities (Figure 1). The copper concentration is highest at the surface and steadily plateaus throughout the bulk to levels consistent with the solid solubility of copper in silicon. The copper signal detected by SIMS shows that the copper is not uniformly

distributed in the silicon but most probably has formed copper silicide precipitates.[16] This is consistent with previous observations of copper silicide formation.[12] Copper silicide is known to significantly decrease minority carrier diffusion lengths to values less than 20 μm.[10, 14] At this stage, the copper contaminated wafer is ready for radial p-n junction fabrication.

The radial p-n junctions are formed via a top-down approach using either optical or nanoimprint (NIL) lithography and standard CMOS compatible processes (see Figure 2 and supplementary information). Individual devices were secured onto a gold coated chip carrier with silver paste. Sputtered silver finger contacts that were 1μm thick, 30 μm wide, and spaced 800 μm apart, were used for the top contacts.[17] Wire bonding onto the top finger contacts completed the circuit. The devices were then loaded onto a stage that has been calibrated to receive 100 mW/cm^2 photon flux (1 sun) through an atmospheric mass (AM) 1.5 filter. I-V measurements were conducted on two types of samples: electronic grade ("clean") planar and radial p-n junction devices and copper contaminated ("dirty") planar and radial p-n junctions (Figure 3). The planar devices were used as controls to show the difference if any from the radial devices and were always fabricated from the identical wafer used for the radial p-n junctions.

For clean devices, the largest efficiency (8 %) is observed for the planar geometry. In contrast, for the dirty devices, those with the radial geometry have larger efficiencies over their planar counterparts. Furthermore, the higher efficiency (≈1.8%) is obtained with a pitch (4 μm) device and arises due to a larger short circuit current. Interestingly, the NIL devices have the smallest efficiency since depletion effects become more important as explained by a model below. Reflectance measurements were performed to rule out any significant contributions from an increase in absorption for the array of holes. Reflectance data show a negligible contribution (reflectance is ≈10 % smaller) for the radial geometry devices.

Previous models of radial p-n-junctions only considered isolated junctions,[4] an analysis which is applicable to multi junction arrays when the nearest neighbor spacing is much larger than twice the diffusion length L_D. To study the effect of device geometry for junction spacing smaller than this, we use a 2-dimensional drift-diffusion / Poisson-equation model with Shockley-Read-Hall recombination (see supplementary material for model details). The geometry in our model is shown in the inset of Figure 4. For large inter-rod spacing, simple geometrical considerations imply that the current collected by the junction in a unit cell of width W is proportional to $W + 2h$, implying a pitch-dependence of the short circuit current density of $1+\frac{2h}{W}$ (dashed green line in Fig. 4). As the pitch is reduced below $2L_D$, the IQE begins to saturate. This is because the collection area of one interface overlaps a region where charge was already being collected by the other interface; the extra interface therefore adds no further benefit.

Further decrease in the pitch so that depletion regions of adjacent interfaces overlap results in a sharp drop in IQE. When depletion regions overlap, carrier densities do not relax to the asymptotic values of single junctions: the majority density maximum value is reduced, and the minority density minimum value is increased. The increase in minority carrier density results in higher recombination, which is the cause of the reduced IQE. As the pitch is further decreased, there is no longer space to accommodate a crossover from n-type to p-type, and the

vertical sections of the rods no longer operate as p-n junctions. At this point, only the horizontal junction contributes (participates in) charge collections, and the structure effectively operates as a planar junction.

In conclusion, we have fabricated and characterized copper contaminated radial p-n junction solar cells. Our experiments have shown that radial p-n junction geometry can resultin improved efficiencies compared to the planar p-n junction devices for silicon samples contaminated with copper. Based on our experimental results and a 2-dimensional model, we have shown that performance of radial p-n junction array solar cells is a strong function of nearest neighbor distance, reaching a maximum at approximately twice the carrier diffusion length, and rapidly degrading as the distance becomes shorter than twice the depletion width.

References

1. Mauk, M. G. *Jom-Journal of the Minerals Metals & Materials Society* **2003,** 55, (5), 38-42.
2. Boettcher, S. W.; Spurgeon, J. M.; Putnam, M. C.; Warren, E. L.; Turner-Evans, D. B.; Kelzenberg, M. D.; Maiolo, J. R.; Atwater, H. A.; Lewis, N. S. *Science* 327, (5962), 185-187.
3. Kelzenberg, M. D.; Boettcher, S. W.; Petykiewicz, J. A.; Turner-Evans, D. B.; Putnam, M. C.; Warren, E. L.; Spurgeon, J. M.; Briggs, R. M.; Lewis, N. S.; Atwater, H. A. *Nature Materials* 9, (4), 368-368.
4. Kayes, B. M.; Atwater, H. A.; Lewis, N. S. Journal of Applied Physics 2005, 97, (11), 11.
5. Ginley, D.; Green, M. A.; Collins, R. Mrs Bulletin 2008, 33, (4), 355-364.
6. Green, M. A.; Emery, K.; Hishikawa, Y.; Warta, W. Progress in Photovoltaics 18, (2), 144-150.
7. Buonassisi, T.; Istratov, A. A.; Pickett, M. D.; Heuer, M.; Kalejs, J. P.; Hahn, G.; Marcus, M. A.; Lai, B.; Cai, Z.; Heald, S. M.; Ciszek, T. F.; Clark, R. F.; Cunningham, D. W.; Gabor, A. M.; Jonczyk, R.; Narayanan, S.; Sauar, E.; Weber, E. R. Progress in Photovoltaics: Research and Applications 2006, 14, (6), 513-531.
8. Sze, S. M., Physics of Semiconductor Devices. John Wiley and Sons: New York, 1981.
9. Davis, J. R.; Rohatgi, A.; Hopkins, R. H.; Blais, P. D.; Raichoudhury, P.; McCormick, J. R.; Mollenkopf, H. C. Ieee Transactions on Electron Devices 1980, 27, (4), 677-687.
10. Istratov, A. A.; Buonassisi, T.; Pickett, M. D.; Heuer, M.; Weber, E. R. Materials Science and Engineering B-Solid State Materials for Advanced Technology 2006, 134, (2-3), 282-286.
11. Wuerfel, P., Physics of Solar Cells. Wiley-VCH: Weinheim, 2005.
12. Istratov, A. A.; Weber, E. R. Journal of the Electrochemical Society 2002, 149, (1), G21-G30.
13. Bathey, B. R.; Cretella, M. C. Journal of Materials Science 1982, 17, (11), 3077-3096.
14. Sachdeva, R.; Istratov, A. A.; Weber, E. R. Applied Physics Letters 2001, 79, (18), 2937-2939.
15. Putnam, M. C.; Turner-Evans, D. B.; Kelzenberg, M. D.; Boettcher, S. W.; Lewis, N. S.; Atwater, H. A. Applied Physics Letters 2009, 95, (16).
16. Istratov, A. A.; Weber, E. R. Applied Physics a-Materials Science & Processing 1998, 66, (2), 123-136.

17. Green, M. A.; Blakers, A. W.; Shi, J.; Keller, E. M.; Wenham, S. R. Ieee Transactions on Electron Devices 1984, 31, (5), 679-683.

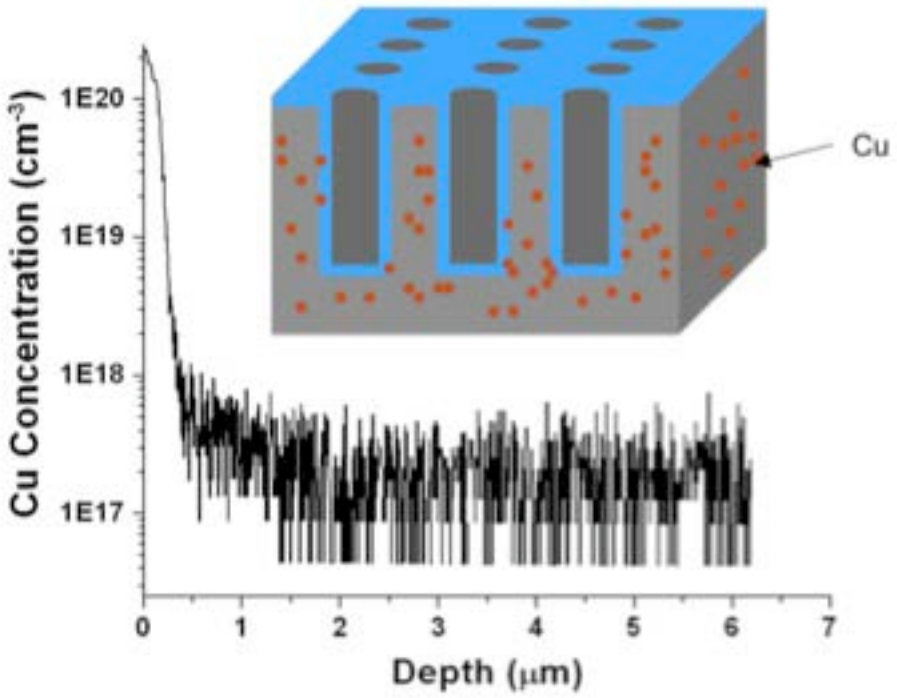

Figure 1. SIMS data collected on a silicon sample contaminated with copper at 950 °C. The copper concentration is highest near the surface but eventually plateaus to a constant level throughout the bulk.

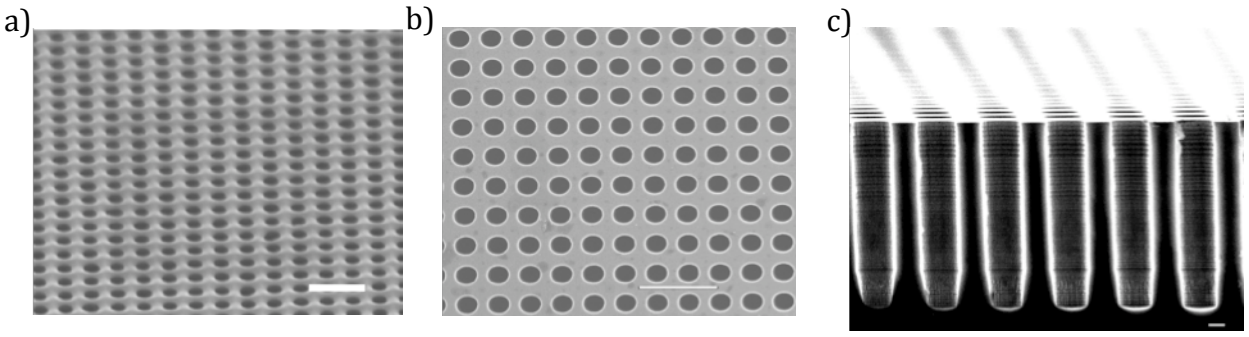

Figure 2. a) A SEM image of an array of holes generated by NIL. The hole diameter is 370 nm and the pitch is 500 nm. (scale bar is 1 μm). b) and c) SEM image of an array of holes generated by optical lithography. The hole diameter is 2 μm and the pitch is 4 μm (scale bar is 10 μm. c) A cross sectional SEM of a representative device. The trenches are 8 μm deep and are etched by DRIE (scale bar is 1 μm).

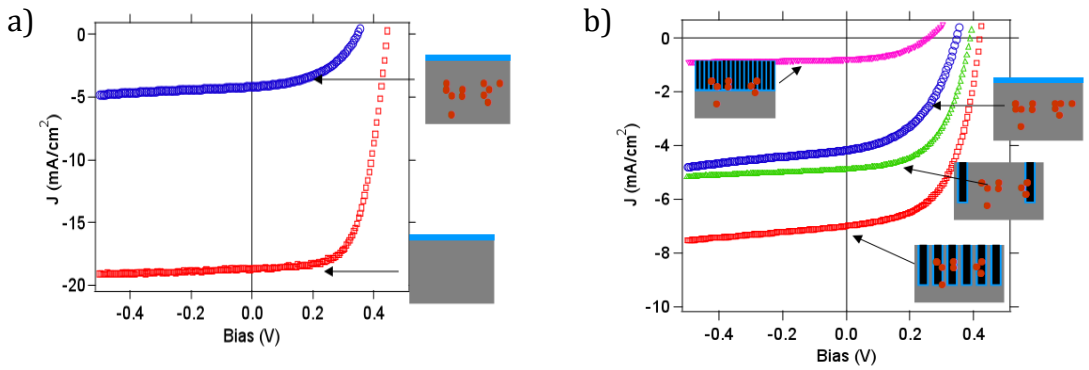

Figure 3. a) I-V data at 100 mW/cm^2 (1 sun and AM 1.5) for a "clean" planar and "dirty" p-n junction solar cell device. The efficiency decreases due to the presence of copper impurities. b) I-V data at 1 sun and AM 1.5 for planar and PL radial devices which were copper contaminated. The radial device with 4 μm pitch has the largest short circuit current and thus the largest efficiency.

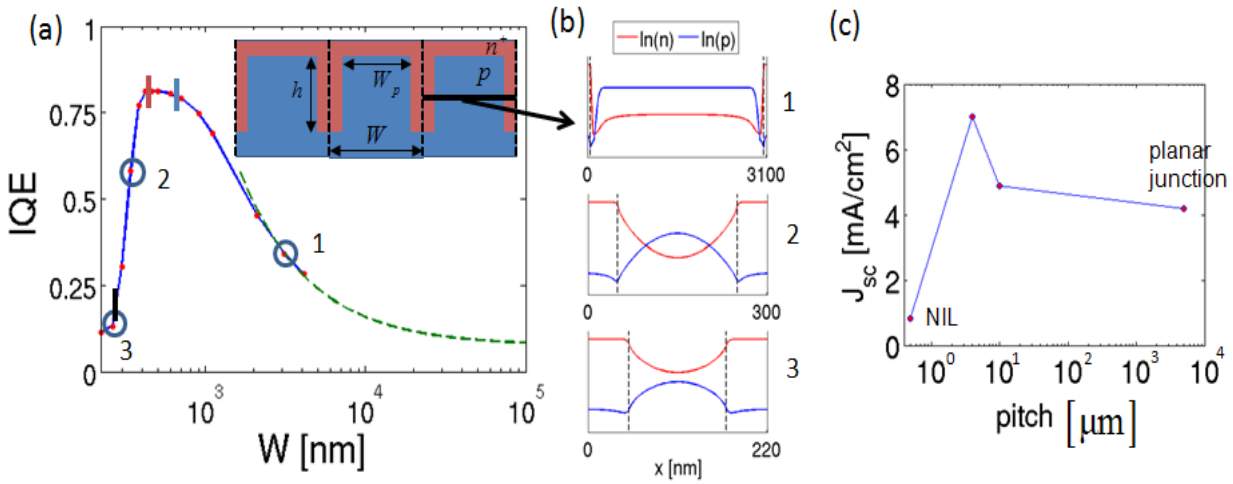

Figure. 4 a) Model results for Internal quantum efficiency versus inter-rod spacing W_p. The dashed green line is the asymptotic form of IQE, as described in the text. Inset shows device geometry, $h = 5500$, $W = W_p + 100$. Blue (red) line on IQE curve shows W_p value where diffusion length (depletion width) of two interfaces overlap, black line shows where rods no longer form p-n junction. b) Cross sections through a unit cell of log(carrier density) for 3 values of W_p: 1. shows widely separated rods, 2. shows regime of depletion width overlap, 3. shows regime with no p-n junction. c) The experimental short circuit current versus pitch shows qualitative features consistent with the modeling result