Six-Pack IGBT Dynamic Electro-Thermal Model: Parameter Extraction and Validation[1]

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Abstract:-**An electro-thermal simulation model is developed for a six-pack IGBT power module. A measurement system suitable for extracting transient thermal data for short term, high-power heating conditions is used in this work for thermal model validation. A set of parameter extraction software tools is used to extract the electrical parameters as well as temperature dependant parameters associated with the IGBT die within the module.**

Keywords: DBC, electro-thermal model, IGBT module, model validation, thermal network.

I. INTRODUCTION

An electro-thermal simulation methodology using the Saber simulator has previously been introduced for a half bridge high power IGBT module [1]. However, the previously developed thermal network only considered one IGBT and one diode per direct-bond copper (DBC) insulating layer structure atop one base plate. The three-phase bridge pack studied in this work has multiple chips per DBC and multiple DBCs on one baseplate. In this work a lateral coupling network is added to the existing model methodology to consider heat flow between chips on the DBC and between DBCs through the baseplate.

Validation of the model is achieved through a high speed transient thermal response system developed in [2]. Previously, only long-term effects at low power of the model were validated. The new system for validation can consider short-term high power conditions. Parameters are extracted from a Six-Pack IGBT module in order to model the electrical characteristics as well as temperature dependent parameters within the device. This is achieved by extracting the temperature dependent parameters at various temperatures to develop a temperature dependent coefficient to be used in the model.

II. ELECTRICAL MODEL

The electro thermal models for power semiconductors devices are connected to both the electrical and thermal networks. The IGBT electro thermal model has three electrical terminals and one thermal terminal. The IGBT electrical terminals are connected to the electrical network component models, and the thermal terminal is connected to the thermal network component models.

To couple the electrical and thermal networks, the IGBT electro-thermal model describes the instantaneous electrical behavior in terms of the instantaneous temperature of the device silicon chip surface T_j (temperature at the device thermal terminal). The temperature dependent electrical model is based upon temperature dependent IGBT model parameters and the temperature dependent physical properties of silicon. The IGBT electro thermal model also calculates the instantaneous power dissipation from the internal components of current because a portion of the electrical power delivered to the device terminals is dissipated as heat and the remainder charges the internal capacitances. The dissipated power calculated by the electrical model supplies heat to the surface of the silicon chip thermal model through the thermal terminal.

The electrical type terminals have units of voltage (V) across the terminals and units of current flowing through the terminals, whereas the thermal-k type terminals have units of temperature (K) across the terminals and units of power (W) flowing through the terminals.

A set of parameters needs to be extracted from the device in order to model its electrical behavior within the circuit simulation. These parameters are defined in Table 1.

The area of the chip was found by measuring the chip directly with a micrometer. The top of the device was opened making the chip visible for measuring.

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[2] Saber is a trademark of Synopsys, Inc. Certain commercial products or materials have been identified in order to specify or describe the subject matter of this paper adequately. This does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that these products are necessarily the best for the purpose.

A	Area of IGBT chip (cm^2)
τ	Minority Carrier Lifetime (s)
I_{sne}	Emmitter electron Saturation Current (A)
V_T	MOSFET threshold (V)
k_{psat}	MOSFET saturation transconductance parameter (A/V^2)
k_{plin}	MOSFET linear transconductance parameter (A/V^2)
C_{gs}	Gate - source Capacitance
W_B	Metallurgical base width
N_B	Base doping concentration
C_{oxd}	Gate drain overlap oxide capacitance (F)

Table 1 Extracted Parameters/definitions

To extract the minority carrier lifetime parameter, the tail current for a constant voltage condition is first measured and transferred to the appropriate software. The exponential current decay rate versus current of the data is fitted to the model equation for constant voltage current decay:

$$-\frac{d\ln I_T}{dt} = \frac{1}{\tau}\left(1+\frac{I_T}{I_{k,\tau}}\right) \tag{1}$$

The anode turnoff current I_T waveform is generated using a clamped large inductive load. The inductor is used because it results in a large current tail. Initially there is a rapid drop in current from the on-state condition in the initial stage of turn-off due to the channel current being cutoff. The remainder of the current tails off slowly, where the time constant of this decay is given by (1).

The relative size of the Anode current tail is used to extract the emitter electron saturation current I_{sne}. The extraction software determines the relative size of the tail by the following equations:

$$\beta_{tr,V} = \frac{I_T(0^+)}{I_T(0^-)-I_T(0^+)}\Big|_{VA=cons\tan t} \tag{2}$$

$$\beta_{tr} = \beta_{tr-\max}\left(1+\frac{I_T(0^+)}{I_k}\right)^{-1} \tag{3}$$

where the expressions for I_K and $\beta_{tr\text{-}max}$ are given by [5]. I_{sne} is then given by the following:

$$I_{sne} = \left(\frac{1}{\beta_{tr-\max} I_k}\right)\frac{4(qn_i AD_p)^2}{(1+1/b)W^2} \tag{4}$$

where b is the ambipolar mobility ratio, and W the base width.

The saturation current $I_{mos\text{-}sat}$ versus gate voltage is used to extract the internal MOSFET saturation transconductance parameter and the threshold voltage. To perform the extraction, the IGBT saturation current is measured versus gate voltage and divided by the current gain of the internal bipolar transistor. The square root of the saturation current is linearly related to the gate voltage given by the following:

$$\sqrt{I_{mos-sat}} = \sqrt{\frac{K_{psat}}{2}}(V_{gs}-V_T) \tag{5}$$

The linear on state voltage versus gate voltage for a constant anode current I_T is used to extract the linear transconductance parameter. The θ term is known as the transverse field transconductance factor and is obtained from the saturation current versus gate voltage for high current. The data is fitted to the following equation:

$$V_{on} = V_r + \frac{I_T}{(1+\beta_{ss})K_{plin}}\left(\frac{1}{V_{gs}-V_T}\right) \tag{6}$$

where:

$$V_r = V_{eb} + R_s I_T + \frac{I_T\theta}{(1+\beta_{ss})K_{plin}} \tag{7}$$

and V_{eb} is the emitter to base junction voltage and R_s is the series resistance.

The IGBT gate-to-source capacitance is found by measuring the turn on gate current waveform and integrating to obtain the charge. Then the gate voltage is plotted versus the gate charge. The slope of this curve during the initial turn on delay time then determines the gate-to-source capacitance. The slope during the second part determines C_{oxd}.

The temperature dependent properties of silicon can be found in [6]. Table 2 shows the temperature dependent IGBT parameters.

$$\tau_{HL} = \tau_{HLO}\left(\frac{T_j}{T_o}\right)^{\tau_{HL1}}$$

$$I_{sne}(T_j) = \frac{I_{sneo}\left(\frac{T_j}{T_o}\right)^{I_{sne1}}}{\exp\left(14000(1/T_j - 1/T_o)\right)}$$

$$V_T(T_j) = V_{TO} + V_{T1}(T_j - T_o)$$

$$K_p(T_j) = K_{po}(T_o/T_j)^{K_{p1}}$$

Table 2 Temperature Dependent Parameters

The expressions for the temperature dependent IGBT model parameters given in Table 2 are developed using the extracted values of the model parameters versus temperature (Fig. 1). An accurate extraction sequence is required to resolve the variations of the model parameters with temperature and is described in [3]. The physical mechanisms resulting in the temperature dependence are described in [6]. Table 3 shows the extracted temperature dependent and non-temperature dependent IGBT parameters for the Six-Pack.

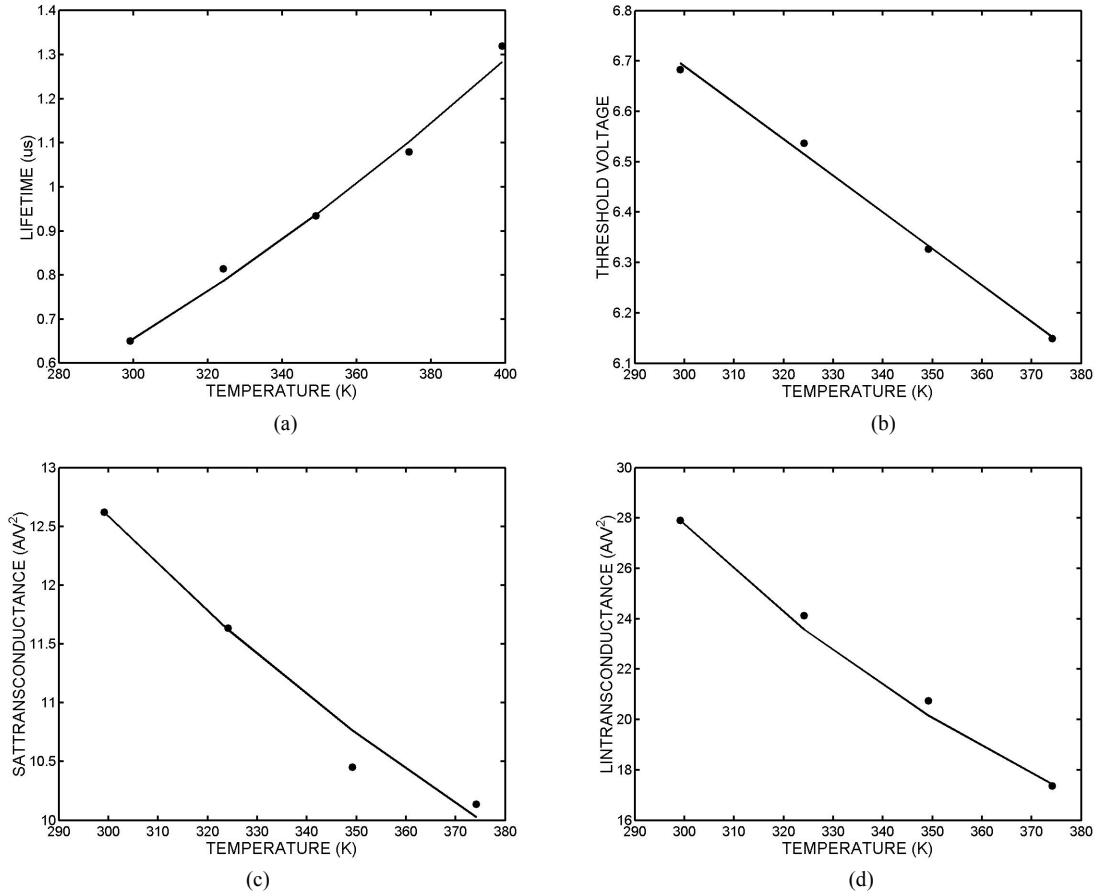

Fig. 1. IGBT temperature dependent model parameters: (a) Lifetime vs. Temperature; (b) Threshold Voltage vs. Temperature; (c) Saturation Transconductance vs. Temperature; and (d) Linear Transconductance vs. Temperature.

$A = 1\ cm^2$	$I_{sne1} = 1.189\ A$
$W_b = 0.02\ cm^2$	$V_{T1} = -7.2$ mV/K
$N_b = 1.5\times10^{14}$	$K_{plin1} = 2.1032$
$\tau_{HL1} = 2.3536$ us	$K_{psat1} = 1.0286$
$C_{gs} = 3.98\times10^{-9} F$	$C_{oxd} = 1.51\times10^{-8} F$

Table 3 Extracted Parameters.

III. THERMAL MODEL DEVELOPMENT

Methods used to develop temperature dependent models for power semiconductor devices are described in the literature, see for example [6]. In this section, the techniques used to develop and to implement the thermal network component models in Saber for the six-pack IGBT power module silicon chips, electrical insulating layer structure, and base plate are described.

The heat transfer process is modeled as a quasi-one-dimensional process with lateral coupling consideration. The rectangular coordinates heat equation describes this process and is shown below:

$$K\frac{\partial^2 T}{\partial z^2} = \rho c\frac{\partial T}{\partial t} \tag{8}$$

with boundary conditions,

$$AK\left.\frac{\partial T}{\partial x}\right|_{X=0} = -P_{in}(t) \text{ and } T(t, x = L_o) = T_{in}(t) \tag{9}$$

Using the geometry of the component, the nonlinear thermal properties of the material and other non-linear heat transport mechanisms such as convection, the thermal network component models are derived from the heat diffusion equation. The three-dimensional heat flow is accounted for using the appropriate symmetry in the discretization in each region of the component using the effective heat flow area approach [6]. This is used to derive expressions for the two-dimensional network of thermal resistances, thermal capacitance, and the heat energies. The grid spacing is made to increase logarithmically with distance from the heat source

to minimize the number of thermal elements required to accurately represent the heat flow for the full range of application conditions.

Figure 2 shows the internal structure of the module.

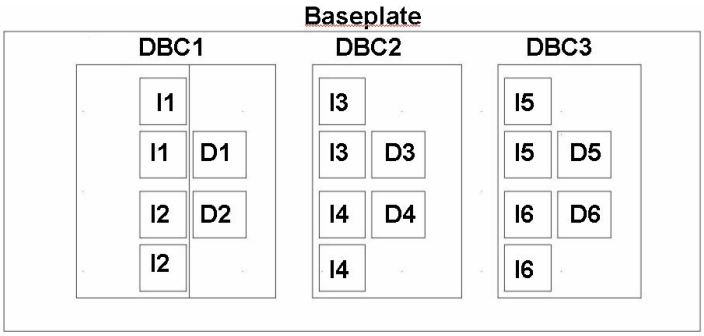

Fig.2 Internal structure of the SEMIKRON power module

There are three DBC structures mounted on one baseplate. Each DBC structure contains two IGBT's and two diodes. Each IGBT is a paralleled combination of two silicon chips. Only one silicon chip is used for each diode.

The thermal model is divided into 12 thermal networks with a thermal network designated for one device. Within each network, three sections are considered. One section is designated for the silicon chip and the others for the DBC and base-plate layer respectively. Lateral coupling between the networks is also included.

A. Silicon Chip Thermal Model

The silicon chip thermal model is a standard library component in the SABER software and it is based upon the rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The details of the model are given in [6].

B. DBC Layer Model

Figure 3 shows the individual layers within the DBC structure. The total thickness of the DBC is divided into five parts. The main heat flow conduction path is made up of five thermal nodes in the vertical direction from the DBC header to the base plate. The thermal resistance and capacitance is calculated between each node. An additional node is used to model the package periphery and accounts for the remainder of the heat capacitance outside the main heat flow conduction path.

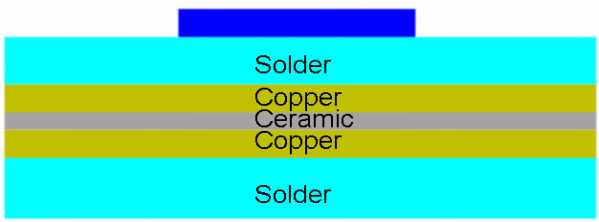

Fig.3 Direct Bonded Copper (DBC) layer structure

A horizontal thermal resistor network is used to model the coupling between each device on the DBC layer. The coupling network consists of thermal resistances because it has been assumed that the majority of the heat capacitance has been accounted for in the main heat flow conduction path and periphery node.

The lateral heat spreading effect, described in [6], describes the main heat flow conduction path making up the vertical portion of the thermal network. A heat flow area that increases with depth into the package is obtained by combining the components of heat flow area due to the cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip.

Because the heat does not spread laterally beyond the edges of the DBC layer, the radius that the heat spreads beyond the edge of chip is limited in the model for each node at depth z_i by the distance from each edge of the chip to the edges of the package on the midpoint between chips. Figure 4 shows a detailed schematic of the boundary conditions on one DBC. The area equation at each node within the DBC for the IGBT is given by (10).

$$
\begin{aligned}
A_{cyli} &= \frac{\pi}{4} L_{ch}(r_{ymci} + r_{ypci}) + 2\frac{\pi}{4} W_{ch}(r_{xmci} + r_{xpci}) + \frac{\pi}{4} L_{ch}(2r_{bti}) \\
A_{sphi} &= \frac{\pi}{4}(r_{ymci} + r_{ypci})(r_{xmci} + r_{xpci}) + \frac{\pi}{4}(2r_{bti})(r_{xmci} + r_{xpci}) \\
A_{rect} &= W_{ch} L_{ch} \\
A_i &= A_{cyli} + A_{sphi} + A_{rect}
\end{aligned}
\tag{10}
$$

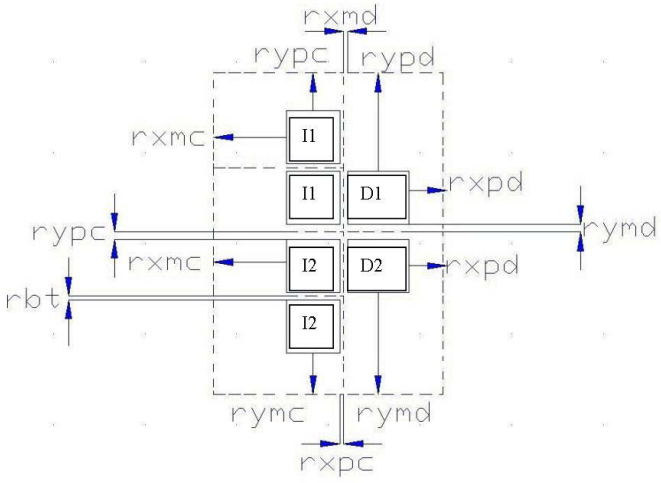

Fig.4 Boundary Conditions for radial heat spread

The dotted lines indicate the radial boundary conditions between chips. The radius that the heat spreads at each node is in the same direction and limited by the corresponding boundary.

$$r_{xpci} = \begin{Bmatrix} z_i \ for \ z_i \le xchedpc \\ xchedpc \ for \ z_i > xchedpc \end{Bmatrix} \quad (11)$$

The effective areas for each of the nodes are calculated in the parameter section of the Saber model and take in consideration the boundaries of the package. The area changes with depth, and the thermal conductivity changes with the materials involved between each pair of nodes. These values are used to calculate the thermal resistance between nodes using:

$$R_{th} = \frac{d}{kA} \quad (12)$$

where R_{th} is the thermal resistance, k is the thermal conductivity, A is the average area between nodes, and d is the distance between nodes. The thermal capacitance is given by:

$$C_{th} = v\rho c \quad (13)$$

where v is the volume between nodes, ρ is the density of the material between nodes, and c is the specific heat of the material between nodes.

Because each DBC layer contains four devices, horizontal coupling must be considered between each vertical thermal network. A coupling resistor is placed between the case nodes of the top IGBT chip and diode. Another coupling resistor is placed between the case nodes of the top IGBT and bottom diode. Finally a resistor is placed between the case nodes of the bottom IGBT chip and diode. Figure 5 shows one segment of the coupling network. The nodes are marked as the temperature at the case of either the top IGBT or bottom diode. For example Tcasect designates the temperature at the case of the top IGBT chip. The coupling resistors are designated as the thermal resistance between the nodes. For example Rcdt is the thermal resistance between the top IGBT and top diode. Each DBC contains one coupling network.

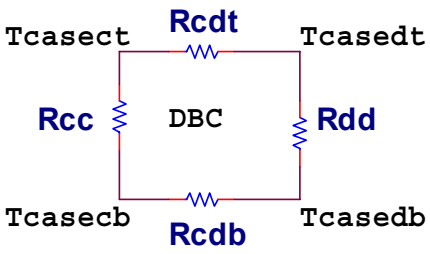

Fig. 5 Coupling network of DBC

C. Base Plate Model

The base plate is divided into three parts, where the main heat flow conduction path is made up of three thermal nodes in the vertical direction from the top of the base plate to the bottom of the base plate. The thermal resistances and capacitances are calculated in the same manner as in the DBC model. The rectangular portion of the heat flow area is the heat flow area at the case of the DBC layer. This value is calculated in the DBC model and exported to the base plate model. The boundary conditions remain the same except for between DBC layers. A boundary is placed between the DBC layers to represent heat flow through the base plate. This boundary is dependent upon the radial heat flow distances at the case nodes of each DBC layer. This location is calculated in the DBC model and exported to the base plate model. A node is also placed at this location and is used for horizontal coupling between DBC layers through the base plate.

A coupling network similar to the coupling network in the DBC model is calculated. The only difference is coupling must be considered between DBC layers. A capacitance is considered between DBC layers and represents the heat capacitance not accounted for in the vertical thermal network. All remaining volume is accounted for in the periphery node. Figure 6 shows the coupling network of the base plate. A temperature is calculated at the node between DBC layers. For example Tbt12 designates the temperature between DBC1 and DBC2.

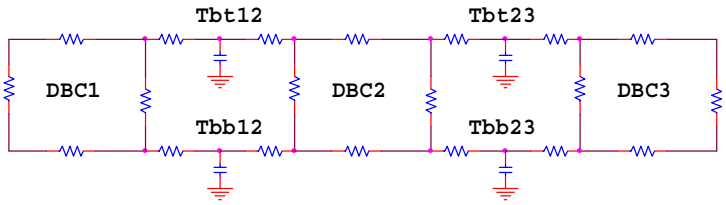

Fig.6 Coupling network of baseplate

IV. Model Validation and Simulation

The test circuit used for the measurements is shown in Figure 7. The TSP used to measure the IGBT chip transient temperature response in this work is the gate-cathode threshold voltage. The test circuit is set up to deal with a half bridge configuration. Either IGBT1 or IGBT2 can be used; the unused devices of the six-pack are disabled by connecting their gate and cathode terminals together as shown. Neither diode is forward biased during the measurements [2].

The cathode of the test IGBT is connected to a pulsed constant current source that is referenced to ground, and the anode of the IGBT is connected to a heavily-bypassed voltage supply, also referenced to ground. The gate of the IGBT is grounded through a 470 ohm resistor that serves as a damping resistor to prevent oscillation. This circuit arrangement causes the IGBT to operate in the active or linear region during the heating phase of the measurement. There is a small auxiliary current source comprised of a 62 V voltage supply and 7.5 k resistor as shown in Figure 7 which is used to limit the amplitude of the measured switching voltage that appears on the cathode, and to provide the capability of using the TSP measurement during the cooling phase [2].

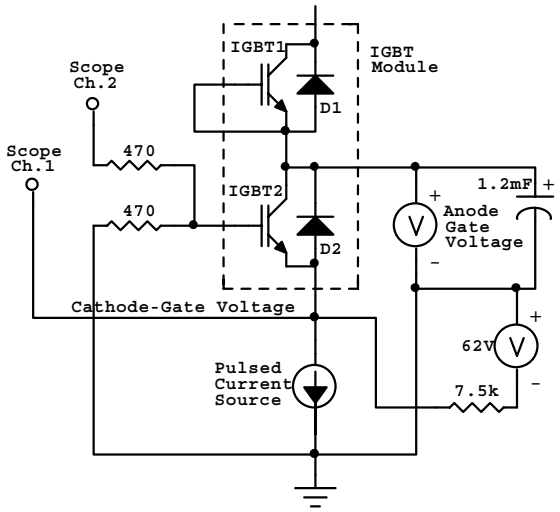

Fig. 7. High Speed IGBT Thermal transient test circuit.

The cathode voltage is applied to channel 1 of a digitizing oscilloscope, and the gate voltage is applied to channel 2 of the scope. The data acquisition is used to provide a differential gate-to-cathode measurement because a substantial voltage transient appears at the gate during switching due to the gate resistor used to prevent oscillation.

The simulations were run in Saber using a constant power pulse source connected to the IGBT thermal module model. Only one IGBT is connected to the power source. A constant temperature source is connected to the base plate of the module representing the constant heat sink temperature used in the experiment. The power level and pulse times are the same as those used in the experiment. The simulated temperatures shown in Figure 8 are the chip junction temperatures. Three power levels were considered and were as follows: 380W, 950W, and 2700W. The highest power pulse was heated for a shorter period of time to save the device from overheating. The remaining pulses were adjusted accordingly. The results look quit good.

A study was done on a half bridge device in [2] that showed that current sharing can be an issue when making thermal measurements on IGBTs made from multiple chips. In that work the chips were then separated from each other and the test was run again on a single chip at the third of a power level, producing much better results. In the study of the six-pack, the current sharing issue did not seem to be as significant and the two IGBT chips did not have to be separated.

V. CONCLUSION

A dynamic electro thermal model is developed and validated for a six pack IGBT module. The same techniques that were previously used for modeling a half bridge IGBT module were improved and used in this work. Parameters were extracted to develop the temperature dependent electrical model. An additional coupling network was added to the model to improve its performance.

Current sharing did not appear to be a problem for the currents used to validate the model, and the agreement between measured and simulated temperature is good.

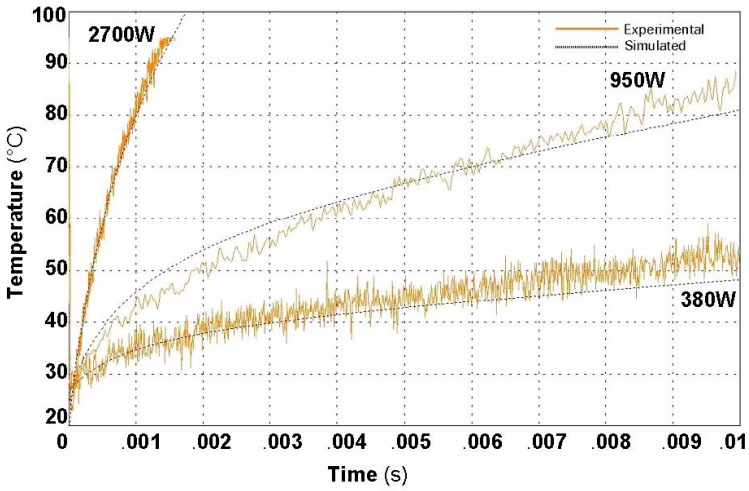

Fig. 8. Transient heating of single IGBT under various power conditions

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