A 4 : 1 Transmission-Line Impedance Transformer for Broadband Superconducting Circuits

Leonardo Ranzani, *Member, IEEE*, Lafe Spietz, Zoya Popovic, *Fellow, IEEE*, and Jose Aumentado

***Abstract*—We present a 4 : 1 superconducting transmission-line impedance transformer for cryogenic applications. The device transforms 25 Ω in the coplanar waveguide to 6.25 Ω in the microstrip and is designed to operate at 20 mK. Calibrated measurements in a dilution refrigerator demonstrate a −3 dB bandwidth from 1.6 to 13 GHz. In a modified Ruthroff design, a small capacitor is integrated at the input as a direct-current block, making it suitable for biasing and matching to low-impedance active circuits, such as superconducting quantum interference device (SQUID) amplifiers.**

***Index Terms*—Impedance matching, superconducting microwave devices, transformers.**

I. Introduction

IMPEDANCE matching to microwave superconducting circuits and components is often difficult to achieve because of extremely low input or output impedances [1]–[3]. The input impedance of superconducting antennas and the output/input impedances of superconducting quantum interference device (SQUID) amplifiers in particular are typically on the order of a few ohms [1], [2], [4]. DC-SQUID amplifiers, consisting of two dc-biased Josephson junctions arranged in parallel to form a loop, can reach noise temperatures below 1 K, limited by the normal (i.e., *nonsuperconducting*) currents in the junctions [5]. However, present designs are typically limited to 5% relative bandwidth with the center frequency in the 1- to 8-GHz range. In order to achieve the impedance matching of dc-SQUID amplifiers to 50 Ω at cryogenic temperatures, quarter-wave resonators [2] or flux transformers [3] have been traditionally employed, but such techniques are often limited by low self-resonance frequencies or narrow bandwidths. Other matching methods that might be used involve either complicated multipole filter topologies [6] (particularly with very high source/device impedance ratios) or are incompatible with the low magnetic fields required for many superconducting devices due to the presence of a ferrite element [7].

Transmission-line transformers (TLTs) [8]–[12] have been extensively used at UHF and higher frequencies due to their compact size and extremely wideband performance. TLTs can achieve high impedance transformation ratios over wide bandwidths by suitably connecting electrically short sections of uniform transmission lines. The Guanella and Ruthroff transformers, in particular, can be used to achieve rational number-valued impedance transformation ratios over several octaves [8]–[10], [13].

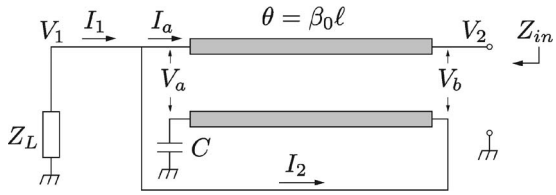

Fig. 1. Schematic of the 1 : 4 impedance transformer developed in this paper.

At UHF and low microwave frequencies, TLTs are typically fabricated with coaxial lines of various characteristic impedance, which are readily available and are commonly wound around a ferrite core to suppress unbalanced currents [9], [14]. The proper operation of the transformer critically depends on the two lines having the same electrical length θ. With increased frequency, the interconnections at the two ends of the transformer become difficult to implement without parasitic reactances, which effectively changes the electrical lengths. Therefore, at higher frequencies, fabrication technologies with good control of parasitics are needed [10], [15]. Recently, a new wafer-scale microcoaxial technology has been demonstrated with 4 : 1 transformation operating in the 2- to 22-GHz range [11].

In this paper, we demonstrate an on-chip TLT in superconducting technology for the first time. The circuit diagram of the TLT is shown in Fig. 1. We introduced capacitor C, usually not present in previous designs, in order to make the device suitable for amplifier biasing. The Ruthroff topology was chosen for its small size and easy microfabrication into superconducting circuits. Impedance matching to 6.25 Ω from 1.6 to 13 GHz has been achieved. The device, fabricated in niobium, has a coplanar waveguide (CPW) 25-Ω input and a microstrip low-impedance 6.25-Ω output, thus providing an easy transition from the off-chip high-impedance CPW lines to the on-chip low-impedance environment. In Section II, we describe the theory and the design of the impedance transformer. In Section III, we discuss the device fabrication and packaging. Section IV describes the device characterization and experimental results. Finally, conclusions are drawn in Section V.

Manuscript received March 22, 2012; revised May 16, 2012; accepted May 21, 2012. Date of current version August 28, 2012. This paper was recommended by Associate Editor B. Plourde.

L. Ranzani and Z. Popovic are with the Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309 USA (e-mail: leonardo.ranzani@colorado.edu).

L. Spietz and J. Aumentado are with the National Institute of Standards and Technology, Boulder, CO 80303 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TASC.2012.2202116

II. Transformer Design

The transformer shown from Fig. 1 can be analyzed in terms of even- and odd-mode excitations [9], [10]. The impedance transformation ratio can be then expressed as a function of the even- and odd-mode characteristic impedances Z_{0e} and Z_{0o}, respectively, and the propagation constants β_e and β_o, respectively. In the limiting case where $Z_{0e} \gg Z_{0o}$, the even mode can be neglected, and the relation between the output and load impedances ($Z_{\rm in}$ and Z_L, respectively) can be calculated following the procedure shown in [10]. The basic network equations for the device in Fig. 1 are

$$\begin{aligned} I_1 &= I_a + I_2 \\ V_a &= V_b \cos\theta + 2jI_2 Z_{0o} \sin\theta \\ I_a &= I_2 \cos\theta + j\frac{V_b}{2Z_{0o}} \sin\theta \\ V_1 &= V_a + \frac{I_a}{j\omega C} \\ V_2 - V_b - V_1 &= 0 \end{aligned} \tag{1}$$

where $\theta = \beta_o l$ is the electrical length of the coupled lines, while V_a and V_b are the voltages across the input and the output of the coupled lines, respectively. As a consequence, the relationship between the input and output impedances ($Z_L = -V_1/I_1$ and $Z_{\rm in} = -V_2/I_2$) can be derived as

$$\begin{aligned} Z_{\rm in} &= 4Z_{0o} \\ &\times \frac{Z_L(\cos\theta+1)+jZ_{0o}\,\sin\theta - \frac{j\cos\theta}{2\omega C}\left(j\frac{Z_L}{2Z_{0o}}\,\tan\theta+1\right)}{2Z_{0o}\,\cos\theta+jZ_L\,\sin\theta+\frac{\sin\theta}{\omega C}}. \end{aligned} \tag{2}$$

With no capacitor, this reduces to the standard Ruthroff expression [9]. The real part of the impedance transformation ratio $Z_{\rm out}/Z_L$ is plotted in Fig. 2 as a function of the electrical length of lines θ for different odd-mode characteristic impedances. An approximate $4:1$ impedance ratio is obtained for $\theta \ll 1.5$ rad. The impedance ratio has a peak at about 1.5 rad. The amplitude of the peak can be controlled by changing the value of the odd-mode impedance. The transformation ratio goes to zero at $\theta = \pi$. Fig. 2 also shows that the impedance transformation ratio at low frequencies is reduced from its ideal value. From (2), the low frequency limit of $R_{\rm in} = Re(Z_{\rm in})$ can be calculated as

$$R_{\rm in} = \frac{4R_L}{1+3\frac{l}{8v_oCZ_{0o}+l}} \tag{3}$$

where v_o is the propagation speed of the odd mode, and $\theta = \omega l/v_o$.

Capacitor C, introduced to allow a dc connection between the input and the output of the device, controls the lower frequency limit of the transformer. Because of the finite value of the even-mode impedance Z_{0e}, the input impedance of the transformer is zero when

$$Z_{0e}\tan(\beta_o l) = \frac{1}{\omega C}. \tag{4}$$

Equation (4) is used to determine the minimum value of C given a desired transformer bandwidth.

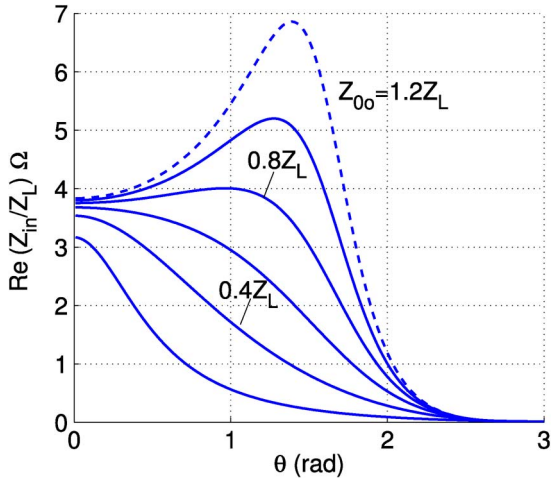

Fig. 2. Theoretical impedance ratio of the transformer from Fig. 1 as a function of the electrical length θ of the coupled lines. Capacitor $C = 10$ pF is assumed. The odd-mode impedance is varied from $0.2Z_L$ to $1.2Z_L$ in 0.2 increments.

III. Device Fabrication and Packaging

The goal of this paper was to design and build a broadband impedance transformer operating from 1.6 GHz over more than 10 GHz of bandwidth, providing a $4:1$ impedance transformation from 25 to 6.25 Ω, for the purpose of providing broadband matching for an ultralow-noise SQUID amplifier. The desired impedance match should minimize the noise temperature of the final amplifier, including the transformer and possibly other matching elements (this is different in general from maximum gain matching). Input and output impedances of microwave SQUID amplifiers are typically ~ 5 and ~ 10 Ω, respectively [1], [2], [4].

This transformer is fabricated in a Josephson junction process, with the layer structure shown in Fig. 3(a). The process is described in detail in [16]. Two layers of Nb and two SiO_2 insulated layers are deposited via sputtering on a 381-μm-thick Si substrate ($\epsilon_r = 11.9$). The top and bottom Nb layers are 400 and 200 nm thick, respectively. The traces are defined via etching. The SiO_2 layers are 350 and 450 nm thick. The superconducting transition temperature of the Nb films is about $T_c = 9$ K and was verified on a different set of wafers produced with the same process.

A sketch of a back-to-back transformer is shown in Fig. 3(b), where both the input and the output are 25-Ω lines. The higher impedance input is fed by a CPW line, while the output is realized in a low-impedance 6.25-Ω microstrip. The sample box provides the ground plane to the coupled lines and the conductor backing to the CPW. The side ground plane of the CPW, placed on the bottom layer of the stackup in Fig. 3, serves as the bottom ground plane for the microstrip. The low 6.25-Ω impedance microstrip line is 80 μm wide. The coupled lines are two broadside-coupled transmission lines placed on the top and bottom Nb layers. The two transmission lines are bent in a ring to enable a short parallel output connection between them.

The ratio between the odd- and even-mode impedances can be estimated by the ratio of the even- and odd-mode capacitances. As a first approximation, this scales as the ratio of substrate thickness, as shown in Fig. 3(a). The Si substrate is

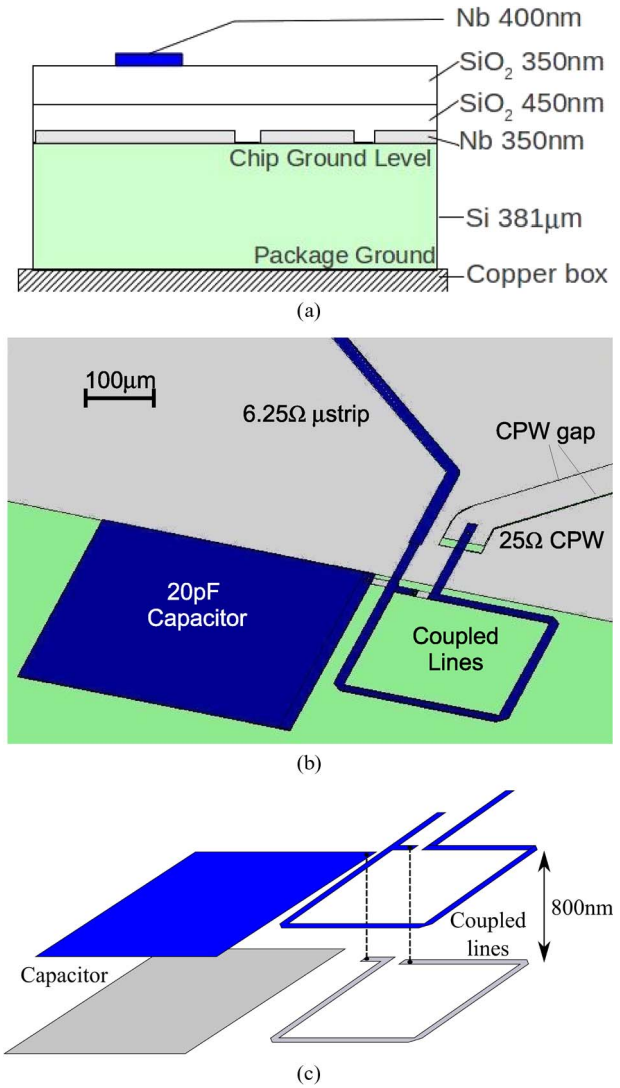

Fig. 3. (a) Layer structure of the deposition process (not to scale) and (b) schematic view of the device. (c) Exploded view of the coupled lines and capacitor. (Gray) Bottom ground plane. (Blue) Top metal. The CPW is 70 μm wide with a 1.5-μm gap. The microstrip line width is 25 μm. The coupled lines are 16 μm wide. A bottom ground plane is provided by the metallic package where the chip is mounted.

381 μm thick, whereas the SiO_2 layer is 0.8 μm thick; therefore, $Z_{0e}/Z_{0o} = 381/0.80 = 476$. The parallel-plate blocking capacitor (C in Fig. 1) is fabricated by the use of the two available Nb layers. A high capacitance is desired for a wider bandwidth; however, the occupied chip area is also a constraint. A value of 10 pF (corresponding to a 450-μm side square capacitor) was chosen. The odd-mode impedance was fixed to $Z_{0o} = 8\ \Omega$. This value, corresponding to the dashed curve in Fig. 2, results in a minimal return loss in the 1.6- to 13-GHz range. Full-wave simulations performed in the High-Frequency Structure Simulator (HFSS)[1] show that, because of dispersion, the microstrip line impedance varies between 6.8 and 6.25 Ω from 1 to 10 GHz. This is partially compensated by means of an

[1]Certain commercial software, equipment, instruments, and materials are identified in this paper to foster understanding. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the software, the material, or the equipment are necessarily the best available for the purpose.

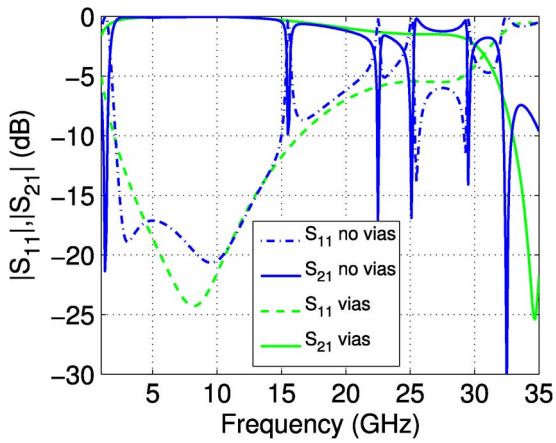

Fig. 4. Full-wave simulation of the influence of through vias connecting the device ground planes on the transformer performance. By avoiding parasitic modes, plated vias through the chip could extend the device bandwidth up to its theoretical limit (continuous line). (Dashed line) In a real device, the bandwidth is reduced. A particular chip size (4 mm $\times$ 5 mm) was chosen in the simulation, and the Nb layers had zero thickness. The simulation was performed on a single 25- to 6.25-Ω transformer.

increased transformation ratio over the same frequency range. The desired transformer operating bandwidth determines the length of the coupled lines. A high value for length l limits the device upper frequency limit, given by condition $\beta_o l = \pi$. The lower frequency limit is determined by (4) and increases at low values of l. A value of $l = 1$ mm was chosen for this design to set a lower frequency limit of 1.6 GHz. The linewidth is optimized to improve the response flatness over the bandwidth, by controlling the odd-mode impedance, as shown in Fig. 2.

We simulated and optimized the 25- to 6.25-Ω transformer using HFSS, with a perfect conductor boundary condition under the substrate, to simulate the package on which it is mounted. The chip ground layer is not directly connected to the package with through vias. The Nb layers were treated as perfect electric conductors for the purpose of the simulation. During the full-wave simulations, the physical dimensions of the device were tuned to minimize the device return loss. The simulation results are shown in Fig. 4. With $l = 1$ mm, the high frequency limit of the device is theoretically equal to 35 GHz (at which point the transmission drops to zero). Full-wave simulations show that parasitic modes in the conductor-backed CPW structure limit the available bandwidth [17]. Such modes can be suppressed by removing the bottom ground plane and adding air bridges or by connecting the two ground planes with through vias. Full-wave simulations performed with through vias next to the main CPW trace, in fact, show a frequency limit of 35 GHz, as shown in Fig. 4. When the through vias are removed, the device upper frequency limit is reduced to 16 GHz for the particular case in Fig. 4. The actual frequency limit depends on the size of the superconducting chip. Since through vias to the bottom of the silicon chip are not possible with the trilayer superconducting deposition process, parasitic CPW modes set the frequency limit in the final fabricated prototype discussed below.

As a test device, a back-to-back transformer was fabricated. The package is shown in Fig. 5. The superconducting chip (with a size of 3.5 mm $\times$ 5 mm) was attached to the bottom of the box

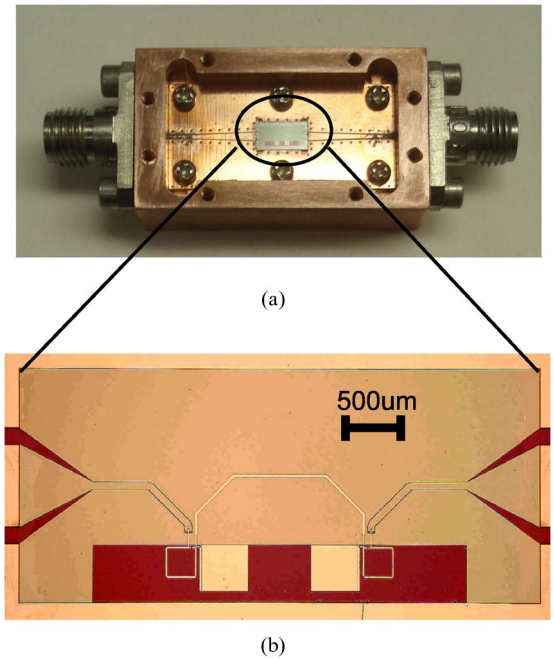

Fig. 5. (a) Picture of the fabricated back-to-back transformer and (b) detail of the superconducting chip. The fabricated device achieves broadband impedance transformation from 25 to 6.25 Ω and back to 25 Ω.

with an Apiezon N[1] high-vacuum grease and wire bonded to a 15-mil-thick Rogers[1] TMM10i microwave board ($\epsilon_r = 9.8$).

The 50- to 25-Ω CPW exponential tapers were fabricated off-chip to connect the input port of the transformer to the 50-Ω coaxial environment. These tapers provide better than 10 dB of return loss at 1 GHz and above. Through vias all around the boards and next to the tapered CPW lines provide good grounding and suppress spurious modes due to the metallic enclosure where the device is placed. The chip bottom ground plane is provided by the metallic package where the superconducting chip is placed. There is no Nb layer at the bottom of the silicon substrate, and therefore, no through-via connection to the top ground plane was possible. The possibility of suspending the superconducting chip and adding air bridges to increase the device bandwidth was not considered, due to its complexity. Resonances related to additional modes in the substrate depend on the chip size and limit the upper frequency of the device to 13 GHz, which satisfied our design goal.

IV. Experimental Results

We characterized the device by the use of an Agilent E5071C Vector Network Analyzer[1] with cables connecting to the device inside a dilution refrigerator operating at a base temperature of approximately 11 mK with no load. During the experiment, an effective temperature between 20 and 30 mK was measured. Through–reflect–line calibration standards, designed and fabricated on the same substrate and in the same type of package as the device under test, were placed at the base of the refrigerator and used to de-embed the effect of the tapers [18]–[20]. Two line standards of different lengths were employed to cover a frequency range from 1 to 16 GHz. The reference planes of the calibration are situated at the 25-Ω CPWs. Mechanical RF

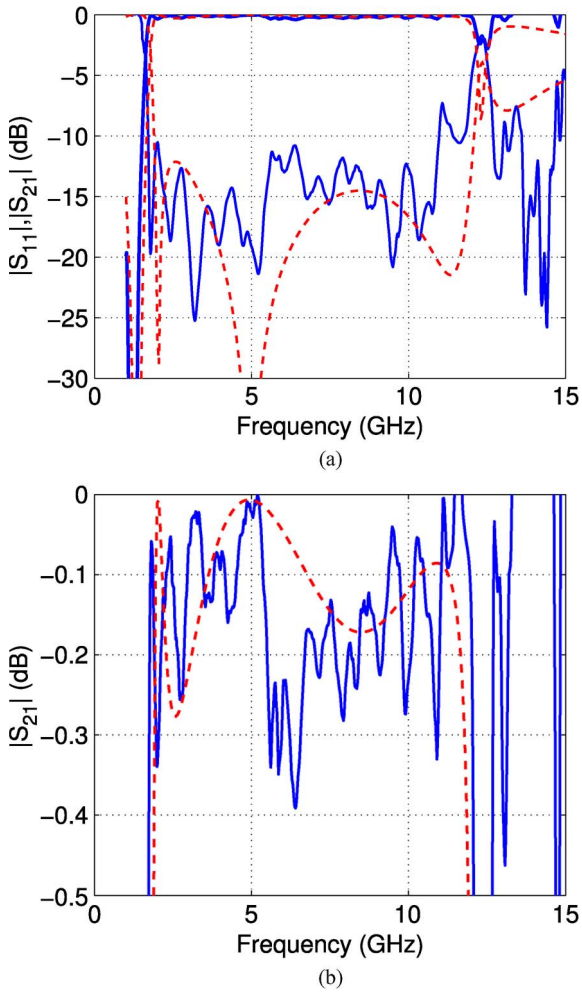

Fig. 6. (a) (Continuous line) Experimental and (dashed line) simulated transmission and reflection coefficients of the back-to-back transformer prototype fabricated in this paper. The data were taken at a base temperature of 20 mK. (b) Transmission is shown in detail on a 0.5-dB scale.

switches operating from dc to 18 GHz were used to switch between the device and calibration standards without the need to warm up the system. The measurement bandwidth was limited by the low-noise amplifiers at the 4-K stage, which worked up to 16 GHz. We obtained a good agreement with the HFSS simulations, as shown in Fig. 6(a). A detailed view of the device insertion loss is reported in Fig. 6(b), where the 0.1-dB 1-GHz standing wave corresponds to the length of the cables between the RF switches and the device, which was not fully removed during the calibration procedure. The low frequency limit of the device at 1.6 GHz agrees well with that predicted by theoretical calculations and simulations. The high frequency limit is due to additional modes in the conductor-backed CPW and could be accounted for by our full-wave simulations, as shown in Fig. 6 and as previously discussed. This limit is dependent on the size of the superconducting chip and, to a lesser degree, on the thickness of the dielectric and Nb layers (300 nm), which was therefore taken into account in the simulations.

The different port impedances on the transformer make it difficult to test it alone. Therefore, we designed a simple capacitively coupled shunt Nb LC resonator with 6-Ω input impedance to test the structure, by inserting it between two

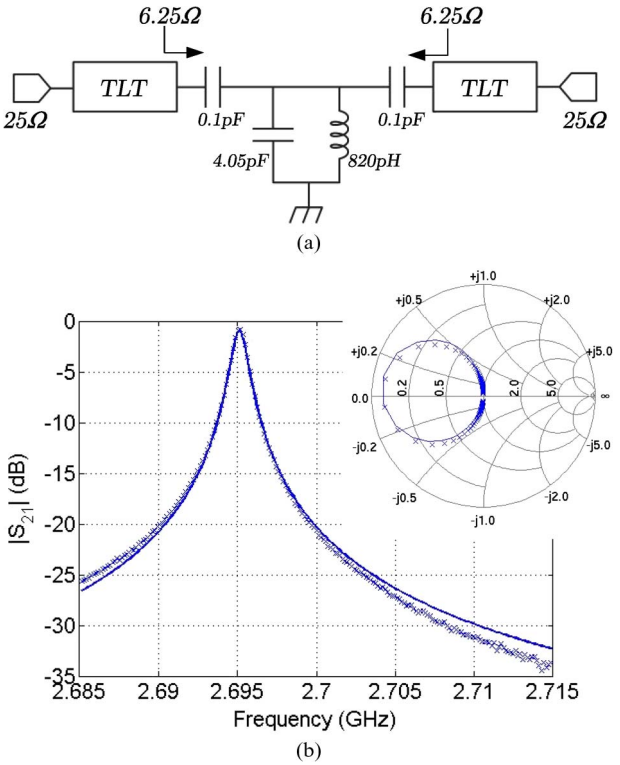

Fig. 7. (a) Schematic of test circuit. (b) (Crosses) Experimental transmission data are compared with (continuous line) theoretical calculations. (Inset) Smith chart plot. The data were taken at a temperature of approximately 20 mK and calibrated at the microstrip line reference plane. The best fitting was obtained for component values within 5% from the original design.

transformers (see Fig. 7). The same package, microwave board, and superconducting-chip footprint were used. The resonator was made of a parallel-plate capacitor (4.05 pF), a coil inductor (820 pH), and two small input decoupling capacitors (0.1 pF). The resonator had a central frequency of 2.7 GHz and a Q factor of 3300. The measured transmission coefficient is shown in Fig. 7 and compared with the circuit simulation best fit. The simulation line corresponds to the lumped element circuit shown in Fig. 7(a). The resonator is strongly overcoupled and well matched. About 83%–90% of the power is dissipated in the load, less than 2% is reflected, and the rest is dissipated in the resonator components. The best fit between simulation and measurements is obtained for a microstrip characteristic impedance of 6.6 Ω with 5% uncertainty.

V. Conclusion

In this paper, we have studied and characterized a superconducting 4 : 1 TLT with a 6.25-Ω output impedance. The transformer design is based on the Ruthroff topology, which was modified by introducing a small blocking capacitor in order to break the ground path at the dc. We have shown that the capacitor increases the low-frequency cutoff of the device and modifies the transformation ratio. The transformer implementation, with an input CPW and an output microstrip line, is suitable to interface high-impedance off-chip devices to low-impedance standard superconducting circuits. This device can be therefore used to achieve broadband matching and biasing of various superconducting devices such as SQUID amplifiers. To achieve the latter goal, the superconducting transformer could be used in conjunction with a lumped-element filter to match both real and imaginary parts of the SQUID impedance over frequency. It is also possible to design a TLT with a larger transformation ratio eliminating the tapered line. This would however require more coupled-line sections. In addition, the transformation ratio must be a square of a rational number [11]; thus, a 1 : 8 ratio is impossible for a pure TLT. However, an extension of the design to a 1 : 9 Ruthroff transformer is possible using four lines, transforming 50 to 5.6 Ω, and is currently under consideration.

References

[1] Y. Tsutsumi, H. Kanaya, and K. Yoshida, "Design and performance of an electrically small slot loop antenna with a miniaturized superconducting matching circuit," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 1020–1023, Jun. 2005.

[2] M. Mück and R. McDermott, "Topical Review: Radio-frequency amplifiers based on dc SQUIDs," *Supercond. Sci. Technol.*, vol. 23, no. 9, p. 093001, 2010.

[3] J. Clarke, W. E. Tennant, and D. Woody, "Impedance matching a Josephson galvanometer by means of a superconducting transformer," *J. Appl. Phys.*, vol. 42, no. 10, pp. 3859–3865, Sep. 1971.

[4] L. Spietz, K. Irwin, and J. Aumentado, "Input impedance and gain of a gigahertz amplifier using a dc superconducting quantum interference device in a quarter wave resonator," *Appl. Phys. Lett.*, vol. 93, no. 8, pp. 082506-1–082506-3, Aug. 2008.

[5] J. Clarke and A. I. Braginski, *The SQUID Handbook*. Winheim, Germany: Wiley, 2003.

[6] S. Oda, S. Sakaguchi, H. Kanaya, R. Pokharel, and K. Yoshida, "Electrically small superconducting antennas with bandpass filters," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 878–881, Jun. 2007.

[7] R. Drapeau, "A wide bandwidth, high-ratio, planar transmission-line transformer for use at cryogenic temperatures," *IEEE Trans. Magn.*, vol. 3, no. 1, pp. 64–71, Mar. 1967.

[8] G. Guanella, "New method of impedance matching in radio-frequency circuits," *Brown Boveri Rev.*, vol. 31, pp. 327–329, Sep. 1944.

[9] C. Ruthroff, "Some broad-band transformers," *Proc. IRE*, vol. 47, no. 8, pp. 1337–1342, Aug. 1959.

[10] J. E. Post, "Analysis and design of planar, spiral-shaped, transmission-line transformers," *IEEE Trans. Adv. Packag.*, vol. 30, no. 1, pp. 104–114, Feb. 2007.

[11] N. Ehsan, K. Vanhille, S. Rondineau, and Z. Popovic, "Micro-coaxial impedance transformers," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 11, pp. 2908–2914, Nov. 2010.

[12] R. F. Sobrany and I. D. Robertson, "Ruthroff transmission line transformers using multilayer technology," in *Proc. 33rd Eur. Microw. Conf.*, Oct. 2003, pp. 559–562.

[13] J. Sevick, *Transmission Line Transformers*, 4th ed. Raleigh, NC: Scitech Publ., 2001.

[14] D. Myer, "Synthesis of equal delay transmission line transformer networks," *Microw. J.*, vol. 35, no. 3, pp. 106–114, Mar. 1992.

[15] M. Engels, R. Jansen, W. Daumann, R. Bertenburg, and F. Tegude, "Design methodology, measurement and application of MMIC transmission line transformers," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, May 1995, vol. 3, pp. 1635–1638.

[16] J. Sauvageau, C. Burroughs, P. Booi, M. Cromar, R. Benz, and J. Koch, "Superconducting integrated circuit fabrication with low temperature ECR-based PECVD SiO_2 dielectric films," *IEEE Trans. Appl. Supercond.*, vol. 5, no. 2, pp. 2303–2309, Jun. 1995.

[17] R. Jackson, "Mode conversion at discontinuities in finite-width conductor-backed coplanar waveguide," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 10, pp. 1582–1589, Oct. 1989.

[18] "Applying the 8510 TRL calibration for non-coaxial measurements," Agilent Technol., San Clara, CA, Agilent Appl. Note 8510-8A.

[19] G. Engen and C. Hoer, "Thru–reflect–line: An improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-27, no. 12, pp. 987–993, Dec. 1979.

[20] M. Elsbury, P. Dresselhaus, N. Bergren, C. Burroughs, S. Benz, and Z. Popovic, "Broadband lumped-element integrated n-way power dividers for voltage standards," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 2055–2063, Aug. 2009.

Leonardo Ranzani (M'09) received the Ph.D. degree in information technology from Politecnico di Milano, Milan, Italy, in 2008.

From 2004 to 2009, he was with the Consortium for Research in Optical Processing and Switching (Corecom), Milan. He is currently a Research Associate with the University of Colorado, Boulder, and a Visiting Researcher with the National Institute of Standards and Technology, Boulder. His research interests include microwave devices, direct-current superconducting quantum interference device (SQUID) low-noise cryogenic amplifiers, optics, and dispersion compensation.

Lafe Spietz was born in Juneau, AL, in 1976. He received the A.B. degree in mathematics and physics from the University of California, Berkeley, in 1998 and the Ph.D. degree in applied physics from Yale University, New Haven, CT, in 2006.

He was a Laboratory Assistant first with the University of California and then with Yale University. Since 2006, he has been a Postdoctoral Associate with National Institute of Standards and Technology, Boulder, CO.

Dr. Spietz is a member of the American Physical Society and the Korean Physical Society.

Zoya Popovic (S'86–M'90–SM'99–F'02) received the Dipl.Ing. degree from the University of Belgrade, Belgrade, Serbia, in 1985 and the Ph.D. degree from California Institute of Technology, Pasadena, in 1990.

Since 1990, she has been with the University of Colorado, Boulder, where she is currently a Distinguished Professor and holds the Hudson Moore Jr. Chair in the Department of Electrical, Computer, and Energy Engineering. In 2001, she was a Visiting Professor with the Technical University of Munich, Munich, Germany. Since 1991, she has been able to make 44 Ph.D. students graduate. Her research interests include high-efficiency, low-noise, and broadband microwave and millimeter-wave circuits; quasi-optical millimeter-wave techniques for imaging; active antenna arrays; and wireless powering for batteryless sensors.

Prof. Popovic was elected as a Foreign Member of the Serbian Academy of Sciences and Arts in 2006. She was the recipient of the 1993 and 2006 Microwave Prizes presented by the IEEE Microwave Theory and Techniques Society for the best journal papers and the 1996 International Union of Radio Science (URSI) Issac Koga Gold Medal. She was the recipient of a 2000 Humboldt Research Award for Senior U.S. Scientists from the German Alexander von Humboldt Stiftung and the 2001 Hewlett-Packard/American Society for Engineering Education Terman Medal for combined teaching and research excellence.

Jose Aumentado, biography not available at the time of publication.