Cryogen-Free Operation of 10 V Programmable Josephson Voltage Standards

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***Abstract*—Given the recent shortages of liquid helium, cryogen-free operation of superconducting devices, such as programmable Josephson voltage standard (PJVS) systems, has become preferable worldwide, and a necessity in some locations. However, reliable operation on a cryocooler is heavily dependent on the ability to create a constant temperature that is low enough to allow the PJVS junctions to operate uniformly. In this work, we systematically investigated as a function of temperature the performance of NIST 10 V PJVS chips employing Nb/Nb_xSi_{1-x}/Nb superconducting junctions. Additionally, we addressed the major factors limiting the performance of a cryocooled PJVS: adequate attenuation of the coldhead temperature oscillations and the minimization thermal gradients between the chip and the cryocooler. Through the development of a robust and reproducible method for soldering chips to a Cu carrier (package), we increased the thermal conductances within the packaging to their practical maximum values. This, in addition to the incorporation of a passive two-stage thermal filter, allows us to confidently predict that the required cooling power for the successful cryogen-free operation of the NIST 10 V PJVS is ∼0.5 W at 4 K.**

***Index Terms*—Josephson arrays, primary standards, superconducting device packaging, thermal conductance, voltage.**

I. Introduction

PROGRAMMABLE Josephson voltage standards (PJVS) utilizing many thousands of Josephson junctions are used worldwide as the accepted standard for the Volt [1]–[3]. The precision voltage of a PJVS is determined solely by fundamental constants and the frequency of the incident microwave signal, and is constant for a range of bias parameters. PJVS operation on a cryocooler [4]–[6] presents three key differences when compared to operation in liquid cryogens. First, the temperature of the coldhead is time-dependent and oscillates at the cryocooler operating frequency (∼1.2 Hz), so some manner of temperature stabilization must be implemented. Second, the cryocooler extracts heat from the system at the surface of the coldhead and, because of the existence of multiple mechanical joints between the circuit and the cryocooler, the temperature of the circuit is always higher than that of the coldhead. Finally, unlike liquid helium, which remains at an essentially constant temperature, the average temperature of the coldhead is a function of the amount of power that is introduced into it, as shown in the load curve of Fig. 1. In this work we describe a temperature stabilization system and optimized thermal interfaces so that a 10 V PJVS can operate on the smallest practical cryocooler.

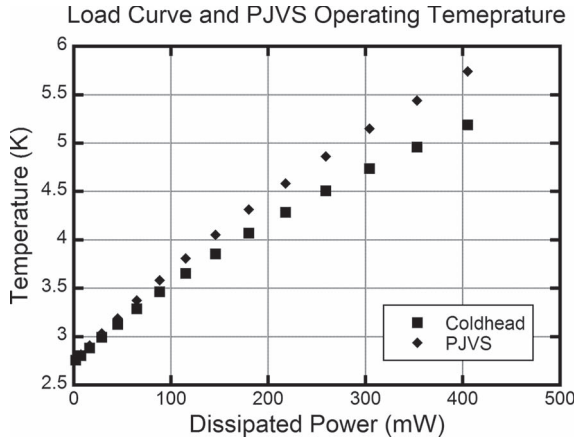

Fig. 1. Load curve of the Sumitomo RDK-101D/CNA-11C[1] cryocooler and the corresponding chip operating temperature. Includes all parasitic heat loads because of dc and microwave leads.

II. PJVS Step Width

While there are multiple quantized states that arise from the ac Josephson effect, the PJVS circuit and its various subarrays of series connected junctions are commonly operated on the voltage corresponding to the first Shapiro step $(n = 1)$ of each junction, as shown in Fig. 2. The array voltage is given by

$$V_{array} = \frac{Nf}{K_{J-90}} \tag{1}$$

where N is the total number of Josephson junctions in that array or set of arrays, f is the frequency of the microwave signal, and K_{J-90} is the 1990-defined value of the Josephson constant. The *step width* of the $n = 1$ step is defined as the current range for which the measured voltage remains constant within a 5 μV threshold. Step width is crucial, as it defines the range of bias parameters over which the voltage is accurately described by

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[1]Commercial software and instruments are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified are necessarily the best available for the purpose.

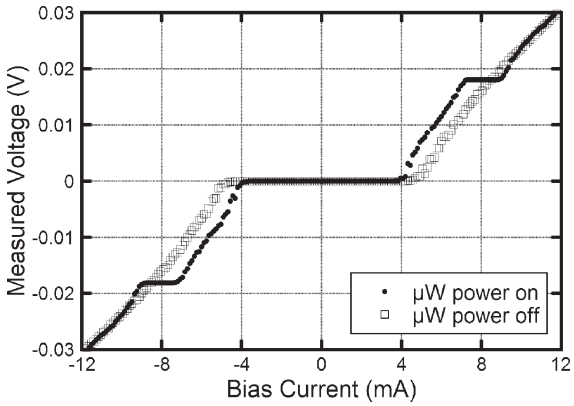

Fig. 2. I–V curve of one of the smaller subarrays of a NIST 10 V PJVS containing only 486 Josephson junctions. The $n = 1$ step is clearly visible when the microwave bias is applied.

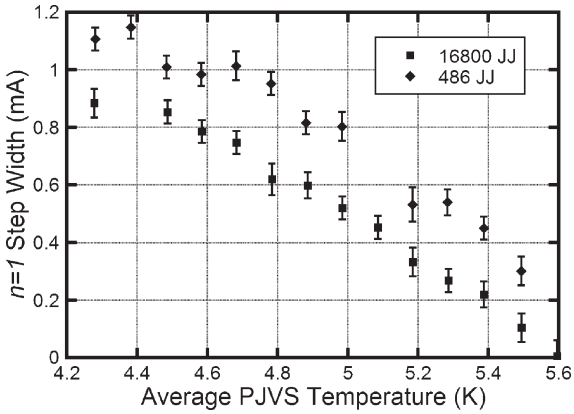

Fig. 3. Maximum step width as a function of temperature of two subarrays of a NIST 10 V PJVS containing 16 800 and 486 Josephson junctions. Each data point is obtained by setting the cryocooler control loop to a given temperature, and then tuning the microwave power to maximize the step width at that temperature. The smaller step width of the larger array demonstrates the effects of junction and microwave power nonuniformity.

(1). Step widths greater than 1 mA are preferred in order to guarantee reliable system operation [7].

Operationally, step width is a function of many factors: the frequency, power level, and uniformity of the microwave signal, junction electrical characteristics, and the junction temperature. Optimal frequencies are largely determined by the design of on-chip microwave components and array transmission lines [8], [9]; thus, at constant temperature, there is an optimal microwave power that provides the maximum step width. When operating on a small cryocooler however, the chip temperature is a strong function of the microwave power dissipated on chip, and it is often impossible to apply the optimum microwave power without increasing the chip temperature and thus decreasing step width below the 1 mA threshold. The effect of increasing temperature on step width is shown in Fig. 3, which demonstrates, as expected, that the maximum step width decreases rapidly with increasing chip temperature. Measurements below 4.28 K were not possible because the microwave power required to obtain a sharply defined step always heated the chip to at least 4.28 K on the present cryocooler. This illustrates the major challenge of successful operation of a cryogen-free PJVS: optimizing the cryogenic system in an effort to minimize the chip temperature within the capacity constraints of the cryocooler.

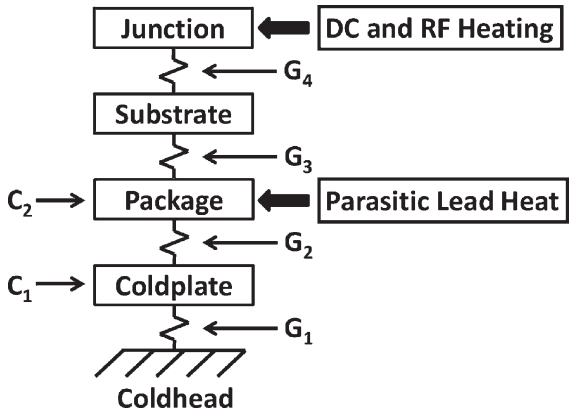

Fig. 4. Block diagram for thermal model defining all thermal conductances.

III. Cryocooler Temperature Stabilization

To minimize the temperature oscillations it is customary to use a low-pass thermal filter consisting of a thermal mass (referred to as the "coldplate") connected to the coldhead via a shim with a high thermal impedance. Fig. 4 shows a simple thermal model of the present cryocooler system, the chip, and the chip packaging. The heat capacities C_1 and C_2, together with the thermal conductances G_1 and G_2, form a two-pole filter described by

$$\frac{\Delta T_P}{\Delta T_{CH}} = \frac{1}{1 + \omega \frac{C_1}{C_2} + \omega C_2 \left(\frac{1}{G_1} + \frac{1}{G_2} \right) + \omega^2 \frac{C_1 C_2}{G_1 G_2}} \tag{2}$$

where ΔT_P is the amplitude of the temperature oscillations of the package, ΔT_{CH} is the amplitude of the oscillations of the coldhead, ω is the cryocooler operating frequency, C_1 and C_2 are the heat capacities of the coldplate and package, and G_1 and G_2 are the thermal conductances of the connecting shim and coldplate-package interface. From (2) it is clear that increasing C_1 or C_2 increases the filter effectiveness so materials with large heat capacity at 4 K such as Er_3Ni [10], or a reservoir of supercritical He [11] have been used by other groups. A simpler and less expensive approach has been employed here using Pb molded around a Cu structure to provide the bulk of the heat capacity C_1. G_1 can be adjusted to provide the desired tradeoff between filter attenuation and steady-state temperature rise. Also, (2) assumes near ideal thermal diffusivity for the coldplate assembly, and without this the effectiveness of the filter is somewhat less than is predicted by (2).

From prior work it has been found that the disparity in thermal contraction rates between Pb and Cu can degrade the clamped thermal interface to the Pb mass after tens of thermal cycles. Combined with the low thermal diffusivity of Pb [12], this reduces the filter effectiveness. To address this, the present coldplate (Fig. 5) was fabricated by casting Pb around a Cu tube so that the differential thermal contraction rates would place the Cu-Pb interface in compression. Additionally, the outer surface of the Cu tube was tinned with Sn-Pb solder before the Pb was cast to provide a metallurgical bond. Table I shows the masses of the materials used, as well as relevant attenuation data at 4 K. Step width is a function of both the time-averaged temperature and the amplitude of the temperature oscillations, so G_1 has

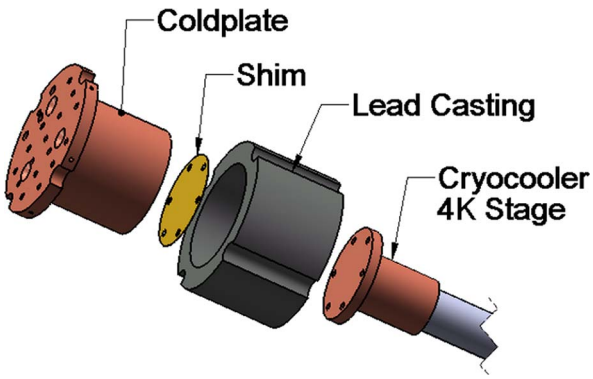

Fig. 5. Exploded view of the coldplate design showing the coldplate and its Pb annulus. The Pb mass (and thus C1) is limited by the volume of the 60 K radiation shield.

TABLE I
COLDPLATE MASS AND FILTER ATTENUATION DATA AT 4 K

Pb Mass (kg)	0.982	C_1 (J/K)	0.719
Total Cu Mass (kg)	1.14	C_2 (J/K)	0.0720
G_1 (W/K)	1.44		
G_2 (W/K)	3.00		
ΔT_{CH} (K)	0.272		
ΔT_P (K)	0.136		
$\Delta T_P/\Delta T_{CH}$	0.499		

been adjusted to give the largest step width, not the smallest temperature oscillations.

IV. THERMAL INTERFACES AND THEIR CONDUCTANCES

A. Overview

In a cryogen-free PJVS the heat generated on-chip passes through a series of thermal interfaces between the chip and coldhead, whereas for operation in liquid helium the chip is always in contact with the cryogen, and the temperature rise in pool boiling helium is ~0.1–0.2 K [13]. In practice, many of the thermal conductances, G_{1-4}, (Fig. 4) are much smaller than the chip-cryogen pool boiling heat transfer coefficient, so a temperature gradient develops between the junctions and the coldhead according to

$$T_J = T_{CH} + Q\left(\frac{1}{G_1} + \frac{1}{G_2} + \frac{1}{G_3} + \frac{1}{G_4}\right) \qquad (3)$$

where T_J is the junction temperature, and Q is the power generated by the chip. As seen in Fig. 3, the Nb/Nb_xSi_{1-x}/Nb junctions used in the NIST PJVS chips require an operating temperature in the range of 4.2–4.6 K which, when coupled with the cryocooler load curve in Fig. 1, indicates that successful operation will be heavily dependent on the optimization of all thermal conductances G_{1-4}, so that the chip may run at the lowest possible temperature. However, in [14] it was found that the use of high-resistivity Si for the substrate of the fabricated chips, as well as increasing the trench depth of the junctions to be greater than the ~150 nm oxide thickness, effectively increases G_4 to ~100 W/K. In this paper, we focus on the optimization of G_{1-3}.

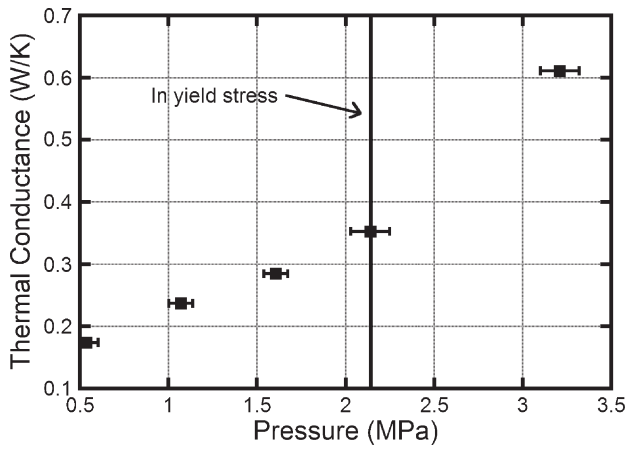

Fig. 6. Plot of the linear behavior of the thermal conductance of a 12 × 17 mm Cu In Si In foil thermal interface (0.127 mm foil) as a function of applied pressure.

B. G_1 (Thermal Filter Shim)

As noted above, G_1 is adjusted to provide a tolerable thermal oscillation consistent with the minimum steady-state temperature rise. In the present coldplate design, a brass shim 0.127 mm thick provides G_1 of 1.44 W/K (at 4 K). While this choice of G_1 minimizes the operating temperature, the remaining temperature oscillations of the chip result in an oscillation in the critical current I_c of the junctions. This oscillation does not change the precision voltage V_{array}, but reduces the step width. Decreasing G_1 would reduce these fluctuations; however, it would also increase the average chip temperature, so the net effect would be to further reduce the step width. In this case, G_1 must be chosen to be as high as possible in order to maximize step width.

C. G_2 (Pressed Indium Foil)

The use of pure In foil (typically 0.127 mm thick) as a thermal interface between various mechanical fixtures is widely accepted in cryogenics as one of the highest-conductance demountable interfaces [15]. This was the original impetus for employing a pressed Cu-In-Si joint between the chip and package in [14], as it provides a demountable interface with reasonable thermal conductance. In that system, the In interface was loaded to its yield stress (~2.14 MPa) under the assumption that the interface thermal conductance would be fairly constant as pressure was increased beyond that point. However, we have since discovered, as shown in Fig. 6, that the conductance of the pressed In foil joint continues to increase significantly at pressures above the In yield stress. Also evidenced by these data is the fact that at the yield stress, the conductance of a Cu-In-Si interface is actually quite low, especially when compared to that of the 0.127 mm brass stabilizer shim.

In the present system, In foil is used in the Cu-In-Cu joint between the chip package and the coldplate (G_2). Further investigation of the conductance of pressed In foil thermal interfaces has revealed that the interface's conductance is determined by three variables: the degree of oxidation of the foil surface

when pressure is applied, the original foil thickness, and the applied pressure. Indium oxidizes rather rapidly when exposed to room-temperature air, so the oxide layer must be removed before assembling the joint. Our final joint design for Cu-In-Cu interfaces employs an In foil 0.076 mm thick, cleaned with a goat-hair brush immediately before pressure is applied, and loaded to several times the yield stress of In. This yields a reproducible thermal conductance for a Cu-In-Cu interface of at least 5 W/K.

D. G_3 (Indium Solder)

While the previous section presents an effective method of thermally connecting the chip package to the coldplate, the amount of pressure required for a 5 W/K interface is far greater than the Si substrate can withstand. Thus we are forced to incorporate a soldered joint at the substrate-package interface (G_3). Literature values for the conductance of Cu-Cu solder joints at cryogenic temperatures are extremely high [16], [17]. This makes a soldered interface a promising approach. However, in our application the solder bond must have the following characteristics: G_3 must be greater than $\sim$10 W/K, the bond must have sufficient ductility to prevent damage to the 12 mm $\times$ 17 mm chip from the differential thermal contraction of Cu and Si, the soldering process must not damage the chip, and the solder bond must withstand numerous thermal cycles without any significant decrease in G_3.

NIST PJVS chips are fabricated on thermally-oxidized silicon substrates, which are very difficult to solder reliably. It is thus necessary to metallize the back of the PJVS chip, either by removing the oxide (often done by etching with a Fl chemistry plasma) and metallizing the Si directly, or by metallizing the oxide. Removal of the oxide can damage the PJVS circuitry, so we chose to thermally evaporate multilayer Cr-Cu-Au 150 nm thick, directly onto the SiO_2. This resulted in a surface that could be easily soldered and caused no degradation of the PJVS circuitry.

A variety of low-temperature solders have been employed for joining cryogenic electronics [18], [19]. We investigated four eutectic solders (wt% compositions are: 51In, 32.5Bi, 16.5Sn; 66.3In, 33.7Bi; 52In, 48Sn; and 100In) by soldering metallized chips to Cu plates, thermally cycling repeatedly to 70 K, evaluating mechanical strength at room temperature, and measuring the thermal conductance of the interface at 4 K. The Bi-based solders exhibited mechanical failures after repeated thermal cycling. The Sn-In solder exhibited sufficient mechanical robustness when cycled. However, while no mechanical failure occurred, the thermal conductance of the solder bond degraded from over 10 W/K to $\sim$1.5 W/K after one thermal cycle. We tentatively attribute this to the previously observed [20] irreversible shrinkage of the solder layer when thermally cycled. Pure In provides a bond with stable mechanical properties, and $G_3 > 10$ W/K for over 10 thermal cycles. Although In has a higher melting temperature than that of the other solders, we were able to avoid any degradation of the PJVS circuitry or formation of excess intermetallic compounds with the chip backside metallization by utilizing a programmable soldering fixture that maintains a controlled pressure on the interface while quickly heating the In solder above its melting point, and rapidly cooling it back to room temperature.

TABLE II
NIST 10 V PJVS THERMAL BUDGET

Source of Heat Load	Heat Generated at 10 V (mW)
DC electrical power	100
Microwave power	250
Total	350

Heat load generated by a NIST 10 V PJVS while in operation at 10 V.

V. REQUIRED COOLING POWER FOR A NIST 10 V PJVS

We previously [14] published a thermal budget for the NIST 10 V PJVS that suggested that operation on the cryocooler characterized in Fig. 1 might be possible. However, the more precise characterization presented here, of both step width vs. temperature, and the on-chip power dissipation, demonstrate that achieving a 1 mA step width for the existing chip design on this cryocooler is not possible. Even after increasing all the system thermal conductances to their practical maxima, the chip cannot produce 10 V with a 1 mA step width at any temperature. In Table II we present a revised thermal budget based on measurements of on-chip power dissipation. The 350 mW on-chip dissipation, plus a conservative allowance for parasitic load due to leads, indicate that a cryocooler capacity of $\sim$0.5 W at 4 K will be necessary to operate the present generation NIST PJVS at 10 V with 1 mA step widths.

VI. CONCLUSION

We have developed techniques for maximizing the conductances of the packaging interfaces for a cryogen-free NIST 10 V PJVS, which in turn allows the chip to operate at the lowest possible temperatures for a given cryocooler capacity. When thermally cycled more than ten times, these interfaces have proven to be mechanically robust and to provide consistent thermal conductance. Using this packaging approach, we predict that operation of a 10 V NIST PJVS is possible on a $\sim$0.5 W cryocooler.

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REFERENCES

[1] S. P. Benz and C. A. Hamilton, "Application of the Josephson effect to voltage metrology," *Proc. IEEE*, vol. 92, pp. 1617–1629, Oct. 2004.
[2] M. Schubert *et al.*, "First direct comparison of a cryocooler-based Josephson voltage standard system at 10 V," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, pp. 816–820, Apr. 2009.
[3] M. Maruyama, T. Yamada, H. Sasaki, H. Yamamori, C. Urano, and N. Kaneko, "Generation of ac waveforms using a NbN-based programmable Josephson voltage standard system with a 10-K cryocooler," in *Proc. Conf. Precision Electromagn. Meas. (CPEM)*, Jun. 13–18, 2010, pp. 8–9.
[4] H. Yamamori, M. Ishizaki, H. Sasaki, and A. Shoji, "Operating margins of a 10 V programmable Josephson Voltage standard circuit using

NbN/TiN$_x$/NbN/TiN$_x$/NbN double-junction stacks," *IEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 858–863, Jun. 2007.

[5] R. Behr, M. Schubert, and T. May, "Accuracy of a cryocooler-based programmable Josephson Voltage standard," *IEEE Trans. Instrum. Meas.*, vol. 53, no. 3, pp. 822–825, Jun. 2004.

[6] A. Shoji, H. Yamamori, M. Ishizaki, S. P. Benz, and P. D. Dresselhaus, "Operation of a NbN-based programmable Josephson voltage standard chip with a compact refrigeration system," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 919–921, Jun. 2003.

[7] C. J. Burroughs, P. D. Dresselhaus, A. Rufenacht, D. Olaya, M. M. Elsbury, Y.-H. Tang, and S. P. Benz, "NIST 10 V programmable josephson voltage standard system, instrumentation and measurement," *IEEE Trans. Appl. Supercond.*, vol. 60, no. 7, pp. 2482–2488, Jul. 2011.

[8] M. M. Elsbury, P. D. Dresselhaus, S. P. Benz, and Z. Popovic, "Integrated broadband lumped-element symmetrical-hybrid N-way power dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 2055–2063, Aug. 2009.

[9] P. D. Dresselhaus, M. M. Elsbury, and S. P. Benz, "Tapered transmission lines with dissipative junctions," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 993–998, Jun. 2009.

[10] K. Allweins, L. M. Qiu, and G. Thummes, "Damping of intrinsic temperature oscillations in a 4 K pulse tube cryocooler by means of rare earth plates," in *AIP Conf. Proc.*, 2008, vol. 985, p. 109.

[11] R. Li, A. Onishi, T. Satoh, and Y. Kanazawa, "Temperature stabilization on a cold stage of a 4 K GM cryocooler," presented at the 9th Int. Cryocooler Conf., Jun. 25–27, 1996.

[12] Y. S. Touloukian, *Thermophysical Properties of Matter*. New York: Plenum, 1970.

[13] B. A. Hands, *Cryogenic Engineering*. New York: Academic Press, 1986.

[14] R. E. Schwall, D. P. Zilz, J. Power, C. J. Burroughs, P. D. Dresselhaus, and S. P. Benz, "Practical operation of cryogen-free programmable Josephson voltage standards," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 891–895, Jun. 2011.

[15] M. Deutsch, "Thermal conductance in screw-fastened joints at helium temperatures," *Cryogenics*, vol. 19, pp. 273–274, 1979.

[16] M. Suomi, A. C. Anderson, and B. Holmström, "Heat transfer below 0.2 °K," *Physica*, vol. 38, pp. 67–80, 1968.

[17] R. J. Webber, C. J. Burroughs, and M. Radparvar, "Performance of a cryocooled Nb DC programmable voltage standard at 4 K," *IEEE Trans. Appl. Supercond.*, vol. 17, pp. 3857–3861, 2007.

[18] J. T. Yeh, "Mechanical properties of In-based eutectic alloy solders used in Josephson packaging," *Cryogenics*, vol. 24, pp. 261–265, 1984.

[19] M. Plötner, B. Donat, and A. Benke, "Deformation properties of indium-based solders at 294 and 77 K," *Cryogenics*, vol. 31, pp. 159–162, 1991.

[20] J. T. Yeh, "Characterization of In-based eutectic alloys used in Josephson packaging," *Metallurgical Mater. Trans. A*, vol. 13, pp. 1547–1562, 1982.