

Nondestructive Measurement of the Residual Stresses in Copper Through-Silicon Vias Using Synchrotron-Based Microbeam X-Ray Diffraction

Chukwudi Okoro, Lyle E. Levine, Ruqing Xu, Klaus Hummler, and Yaw S. Obeng

Abstract—In this paper, we report a new method for achieving depth resolved determination of the full stress tensor in buried Cu through-silicon vias (TSVs), using a synchrotron-based X-ray microdiffraction technique. Two adjacent Cu TSVs were analyzed; one capped with SiO₂ (0.17 μ m) and the other without. The uncapped Cu TSV was found to have higher stresses with an average hydrostatic stress value of 145 ± 37 MPa, as compared with the capped Cu TSV, which had a value of 89 ± 28 MPa. Finite element-based parametric analyses of the effect of cap thickness on TSV stress were also performed. The differences in the stresses in the adjacent Cu TSVs were attributed to their microstructural differences and not to the presence of a cap layer. Based on the experimentally determined stresses, the stresses in the surrounding Si for both Cu TSVs were calculated and the FinFET keep-out-zone (KOZ) from the Cu TSV was estimated. The FinFET KOZ is influenced by the microstructural variations in their neighboring Cu TSVs, thus, it should be accounted for in KOZ design rules.

Index Terms—Interconnect, keep-out-zone (KOZ), stress measurement, synchrotron, three-dimensional integrated circuits (3DIC), through-silicon via (TSV), X-ray diffraction.

I. INTRODUCTION

ONE of the main root causes for failure occurrence in microelectronic devices is the buildup of stresses. Stresses result in damage such as delamination, cracking, and voiding, which may lead to a short or open circuits. These stresses originate from the mismatch in the material properties of the different material constituents of the microelectronic chip, most especially their coefficient of thermal expansion (CTE).

Even though stress-related failures have been and continue to be a major challenge in the semiconductor industry, the

emergence of 3-D stacking of chips using through-silicon vias (TSV), has significantly increased stress-related reliability challenges. Since connection between the stacked dies are achieved vertically through active silicon dies using TSV interconnects, the large mismatch in the CTE of the silicon matrix and the copper TSV interconnects results in the buildup of stresses [1]. Reports have shown that stress related to the integration of Cu TSVs leads to failures or damage such as silicon cracking [2], back-end-of-line (BEOL) bending and damage [3], sidewall delamination [4], and the degradation of front-end-of-line (FEOL) device performance [5].

The key to addressing stress-related reliability challenges presented by the integration of Cu TSVs is anchored on the development of a metrology technique for accurate quantification of the stress in these structures. The micro-Raman spectroscopy technique has been widely used for assessing local stresses in microelectronic chips. Unfortunately, while the micro-Raman technique can determine the stress in the surrounding Si by measuring the frequency shift of the Raman peak, it cannot measure the stress in Cu TSVs because Cu does not have a Raman peak [6]. Additionally, this technique measures only the effective stresses in materials, i.e., the interaction between the different stress components. Furthermore, it does not give depth profile information of the stress in a structure as the calculated effective stress is integrated over the beam penetration depth. Similarly, the other techniques used for measuring stresses in microelectronics such as the wafer curvature method, and laboratory X-ray diffraction cannot be used for determining stress in individual Cu TSVs.

In recent times, synchrotron-based microbeam diffraction has been demonstrated to be an effective metrology tool for the measurement of the stress/strain in Cu TSVs. Some researchers have used this technique to quantify the stress in Cu TSVs [8], [9]. However, their measurement technique required destructive sample preparation, as the sample was cut through and measurements were performed close to the TSVs. This method of measurement has the disadvantage of possibly underestimating the stress in the Cu TSV and the surrounding Si, as a result of stress relief during sample preparation. Additionally, they were not able to achieve a depth resolved measurement of the full stress tensors in Cu TSVs.

In contrast, in this paper, we report the use of synchrotron-based X-ray microdiffraction to perform a nondestructive, depth resolved determination of the stress tensors in buried Cu TSVs. We also attempted to determine the impact of a BEOL layer on the stress in Cu TSVs, by performing a

Manuscript received February 12, 2014; accepted April 30, 2014. Date of publication May 20, 2014; date of current version June 17, 2014. The XOR/UNI facilities on Sector 34 at the Advanced Photon Source (APS) is supported by the U.S Department of Energy's (DOE) Office of Science, under Contract No. DE-AC02-06CH11357. The review of this paper was arranged by Editor R. Venkatasubramanian.

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Digital Object Identifier 10.1109/TED.2014.2321736

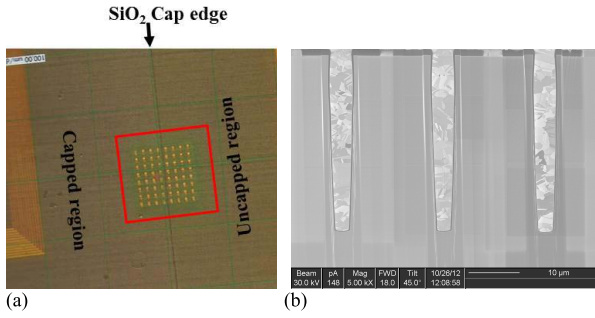


Fig. 1. Images of the sample used in this paper. (a) Optical image of the top view of the sample. Highlighted area shows the 8 by 8 Cu TSV array, half of which were capped with SiO_2 . (b) FIB-SEM image of three adjacent Cu TSVs without any SiO_2 capping.

comparative study. Using the experimentally determined Cu TSV stress, we analytically calculated the expected stress in the surrounding Si, as well as the keep-out-zone (KOZ) of the FinFETs. Additionally, thermomechanical modeling was performed to gain more insight on the impact of a cap layer on the stress distribution in Cu TSVs. A preliminary work was reported in [10].

II. EXPERIMENT

A. Sample

This paper was performed on blind Cu TSV arrays, with pitch, diameter, and depth dimensions of 12, 5, and 50 μm , respectively. The thicknesses of the isolation liner (SiO_2) and the barrier layer (TaN) were about 0.5 and 0.025 μm , respectively. The TSV wafers were manufactured by SEMATECH.¹ After wafer dicing, half of an individual die was capped with 0.17 μm of plasma-enhanced chemical vapor deposition SiO_2 . Afterward, the sample was annealed at 420 $^\circ\text{C}$ for 30 min in a nitrogen ambient environment. These additional processing steps were to simulate the presence of a BEOL layer, and to study the effect of such a post-TSV layer on the stress state in the Cu TSV. Synchrotron-based X-ray microdiffraction was performed on two adjacent Cu TSVs; one capped with SiO_2 , the other without. Fig. 1(a) shows the plan view optical image of the sample used in this paper, the boxed region shows the 8 by 8 array of TSVs, where half of the array is capped with SiO_2 . Fig. 1(b) shows a FIB-SEM cross-sectional image of three adjacent Cu TSVs, without any SiO_2 capping.

B. X-Ray Microdiffraction Experiment

This synchrotron-based study used the microdiffraction instrument on sector 34-ID E at the advanced photon source, Argonne National Laboratory. Three amorphous Si area detectors were used for this experiment to measure the full strain/stress tensors in buried Cu TSVs, as shown in Fig. 2.

¹Certain commercial equipment, instruments, or materials are identified in this paper to specify experimental or theoretical procedures. Such identification does not imply recommendation by NIST nor the authors, nor does it imply that the equipment or materials are necessarily the best available for the intended purpose.

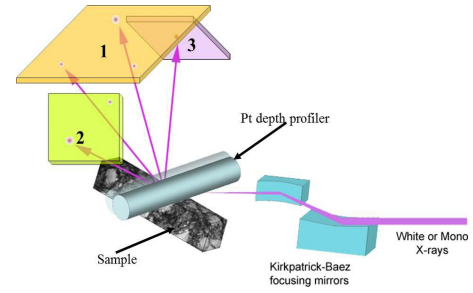


Fig. 2. Schematic diagram of the X-ray microbeam diffraction instrument that was used for this experiment. Three area detectors were used for this paper. Note the identification numbers of the different area detectors. Detectors 2 and 3 are inclined at 45° with respect to detector 1 to maximize the range of measured angles.

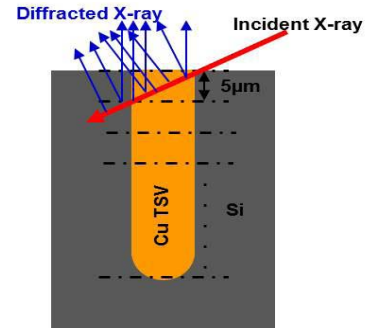


Fig. 3. Schematic diagram showing how the measurements were performed. Measurements were performed at a depth interval of 5 μm .

The incident 0.5 by 0.5 μm polychromatic X-ray beam is inclined at 45° to the sample surface and intersects multiple Cu TSVs, producing Laue patterns on three area detectors that are placed to cover the widest possible angular range. Translating a depth-profiling platinum wire across the sample surface allows the depth of each diffracting volume to be determined [11], [12], thus identifying those diffraction peaks that originate from the desired TSV. After each polychromatic, depth-resolved measurement, the sample is translated parallel to the sample surface so the X-ray beam intersects the selected TSV at a different depth. Eleven of these measurements were performed along the Cu TSV depth, with a step interval of 5 μm , as schematically shown in Fig. 3.

For each sample step, the polychromatic Laue patterns from the correct TSV were indexed. Three widely separated reflections (one on each detector) from a single grain were identified, as well as their corresponding energies and pixel coordinates. These matching reflections were then examined using energy-scanned monochromatic X-rays which allow absolute lattice spacing to be determined. As an illustration, Fig. 4 shows the energy-integrated diffraction peaks of the matching reflections from the three different detectors. These data are from the uncapped sample at $\approx 12.5\text{-}\mu\text{m}$ depth. The marked peak intensities, **A**, are the matching peaks on the three detectors, which were used for the calculation of the strain tensors. In most of the cases, the Cu grains exhibit multiple peaks for each reflection, indicating that the grain is broken up into subvolumes with relative rotations, typically around $1^\circ\text{--}2^\circ$. Matching volumes were easily identified

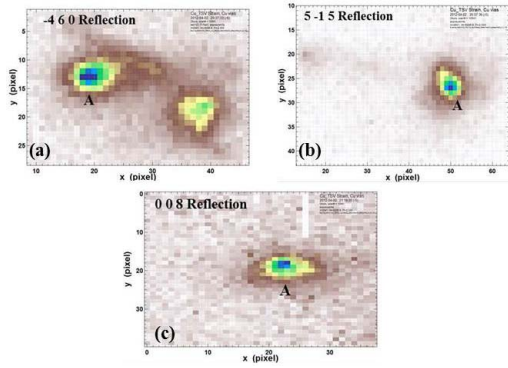


Fig. 4. Peaks of the matching Laue pattern reflections of the three different area detectors obtained after an energy scan using monochromatic X-ray beam, for the uncapped Cu TSV at a depth of $\approx 12.5 \mu\text{m}$. (a) Detector 1. (b) Detector 2. (c) Detector 3. The peaks marked **A** are the matching peaks from the different area detector reflections.

by examining the subtended angles between the reflections. Nonmatching volumes produced large artificial shear stresses in the GPa range.

From this experiment, we obtain the depth of the diffracting volume, the indices of the reflections, the coordinates of the peaks on the detectors, and the corresponding d spacings. These data are sufficient to compute the complete geometry of the unit cell and Euler angles describing the orientation with respect to the lab coordinate system. The full strain tensor is then calculated assuming the unstrained lattice constant of pure Cu at room temperature. The reported uncertainties in the tensor components were obtained by propagating all of the measurement uncertainties using Monte Carlo uncertainty analysis. We note that all of the off-diagonal components of the stress tensors were much smaller than the diagonal components, demonstrating that correctly matching sample volumes were used. Any such errors would produce large, unphysical values. Additional details about the procedure used for the measurement of the full strain/stress tensor are reported elsewhere [13].

The stress tensor results are initially computed in the coordinate system of the given crystal, then converted to the laboratory coordinate system using the Euler angles (φ , θ , ψ), and finally transformed to a coordinate system tied to the sample geometry. This was achieved by performing a 45° rotation about the x -axis (out of the page in Fig. 3), since the sample was inclined at 45° to the incident X-ray beam direction.

It is worth noting that the depth along the Cu TSV of each measurement is only known within a $5 \mu\text{m}$ window, as the selected grain could be anywhere along the path of the incident X-ray beam. Thus, the mean depth is used for all measurement results. For instance, the measurement done between 0 and $5 \mu\text{m}$ is assumed to be measured at a depth of $2.5 \mu\text{m}$.

C. Finite Element Modeling

To understand the stress distribution in a Cu TSV, as well as the impact of capping, a finite element method (FEM)-based 3-D thermomechanical model was built using the COMSOL software platform.¹ Due to geometric symmetry, only half of the structure was modeled, as shown in Fig. 5. For

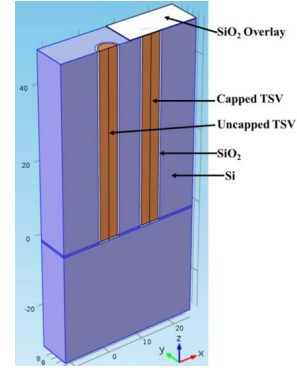


Fig. 5. 3-D model of the structure that was built to study the effect of temperature on the buildup of stresses.

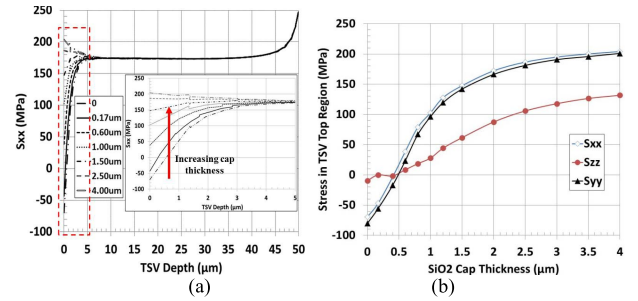


Fig. 6. Effect of SiO_2 cap thickness on the stress in Cu TSV. (a) S_{xx} stress profile along the Cu TSV depth. Stress profile was taken from the center of the Cu TSV. Inset: blowup of the boxed region of the main graph. (b) Normal stresses in the top-most region of the Cu TSV.

simplicity, all of the materials were modeled as isotropic materials, and the material properties were obtained from [6] and [7]. While Si and SiO_2 were modeled as elastic materials, Cu was modeled using elastic-plastic behavior with strain-hardening, having an initial yield stress of 172 MPa and a tangential modulus of 512 MPa [6]. A stress-free temperature of 143°C was used for Cu, based on the results from [5] and [7]. To fully understand the impact of capping on the stress in a Cu TSV, a parametric study of the thickness of the SiO_2 cap layer was performed by varying its value from 0.17 to $4.0 \mu\text{m}$. FEM results are presented in Fig. 6.

It is worth noting that the presented FEM studies and the X-ray microdiffraction experimental data share the same coordinate system (Fig. 5).

III. RESULTS AND DISCUSSION

A. Finite Element Modeling

To understand the impact of capping on the stress in Cu TSVs, a parametric study was performed in which the TSV stress was calculated as a function of the SiO_2 cap thickness, as shown in Fig. 6. This graph was taken from the center of the Cu TSV. Fig. 6(a) shows that independent of the SiO_2 cap thickness that the stress in the Cu TSV remained unchanged for depths $\geq 5 \mu\text{m}$. This means that the impact of capping on Cu TSV stress is limited to the top $5\text{-}\mu\text{m}$ region of the Cu TSV. The insert graph, which is a blow-up of the top $5\text{-}\mu\text{m}$ region, shows that the stress at the top region of the Cu TSV increases with cap thickness. As the cap thickness

TABLE I
DEPTH DEPENDENT GRAIN ORIENTATION FOR THE CAPPED
AND UNCAPPED Cu TSVs, NORMAL TO THE SAMPLE
SURFACE DIRECTION [0 1 - 1]

Depth (μm)	Capped Cu TSV	Uncapped Cu TSV
2.5	-	-
7.5	(1 0 2)	($\bar{1}$ 0 $\bar{3}$)
12.5	(2 $\bar{1}$ $\bar{2}$)	($\bar{1}$ 2 1)
17.5	-	($\bar{1}$ 2 2)
22.5	($\bar{3}$ 1 0)	-
27.5	($\bar{1}$ 0 1)	(1 $\bar{3}$ 1)
32.5	-	(1 $\bar{1}$ $\bar{3}$)
37.5	(2 $\bar{1}$ $\bar{2}$)	-
42.5	-	-
47.5	-	(1 0 1)
52.5	-	(1 0 1)

increases, the stresses at the top region became increasingly tensile. A plot of the normal stresses in the top-most region of the Cu TSV, shown in Fig. 6(b), clearly shows a continuous increase in the stresses with cap thickness. For instance, when the cap thickness increases from zero to $4.0 \mu\text{m}$, the change in the in-plane stresses (S_{xx} and S_{yy}) were found to be as large as 270 MPa, while the out-of-plane stress (S_{zz}) was about 180 MPa.

This result indicates that the thickness of the cap layer can critically influence the stress magnitude within the top region of the Cu TSV. This has reliability implications, as the induced stresses in the surrounding silicon are detrimental to the performance of integrated FEOL devices such as MOSFETs, FinFETs, and so on. The variation in these devices is expected to scale with the thickness of the BEOL layer.

B. Microdiffraction Measurement Grain Orientation

Based on the determined Euler angles, the depth dependent grain orientation of the capped and the uncapped Cu TSVs were determined and presented in Table I. The orientation of the grains are calculated in the direction normal to the sample surface, i.e., [0 1 - 1] direction.

The grain orientations were observed to vary across the length of the Cu TSV. Additionally, the grain orientation of the capped and the uncapped Cu TSVs are shown to be dissimilar from each other. For the uncapped Cu TSV, the grain orientations at 47.5 and 52.5 μm are the same (1 0 1). Additionally, the reflection of their diffracted X-ray were similar having a reflection of 2 4 4 for the detector 1. This means that the measurement was performed on the same grain at 47.5 and 52.5- μm depth, which implies that this grain is at least 10- μm large.

C. Normal Stresses

Figs. 7 and 8 show the depth dependence of the normal stress components (S_{xx} , S_{yy} , and S_{zz}) for the capped and the uncapped Cu TSVs, respectively. All uncertainties are one sigma. They result from uncertainties associated with the accurate determination of the position of the diffracted X-ray

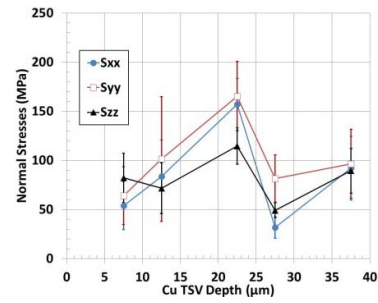


Fig. 7. Experimentally determined normal stresses for the capped Cu TSV with respect to depth. The uncertainties result from uncertainties in the diffracted X-ray peak positions on the area detectors and uncertainties in the lattice spacing determination.

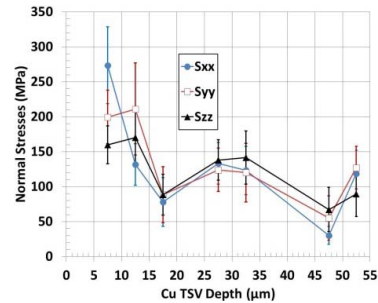


Fig. 8. Experimentally determined normal stresses for the uncapped Cu TSV with respect to depth. The uncertainties result from uncertainties in the diffracted X-ray peak positions on the area detectors and uncertainties in the lattice spacing determination.

peak on the area detectors, as well as uncertainties associated with the accurate determination of the lattice spacing. These two graphs (Figs. 7 and 8) show that the entire Cu TSVs, both the capped and the uncapped, are under tensile hydrostatic stress, since the values of the different normal stresses are positive and approximately equal. The magnitude of the normal stresses varied along the length of the Cu TSVs, which is attributed to a combination of experimental uncertainties and local variations in the microstructure as evidenced by Table I. Furthermore, for both Cu TSV types, we were unable to determine the stress within the top 5 μm of the TSV due to the large plastic deformation within this region.

For the capped Cu TSV (Fig. 7) a hydrostatic stress value of ≈ 67 MPa is observed at a depth of about 7.5 μm and ≈ 93 MPa at a depth of 37.5 μm . The different normal stresses were observed to overlap as a function of the Cu TSV depth, except at about the center of the Cu TSV (22.5 μm), where the maximum stress in the capped Cu TSV was observed. At this depth, the maximum stress of 165 MPa was observed in the y-direction, while the calculated hydrostatic stress at this depth was ≈ 146 MPa.

Fig. 8 shows the normal stresses in the uncapped Cu TSV. The stresses were observed to be higher compared with the capped Cu TSV (Fig. 7). At a depth of about 7.5 μm , the average hydrostatic stress was ≈ 211 MPa. At the center of the Cu TSV (27.5 μm), the average hydrostatic stress was ≈ 132 MPa. A minimum average hydrostatic stress of

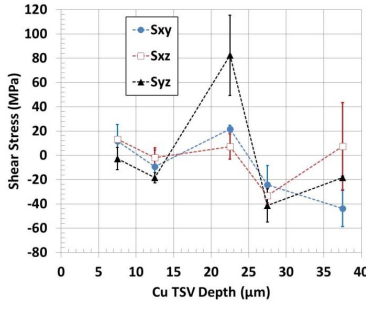


Fig. 9. Experiment shear stress components (S_{xy} , S_{xz} , and S_{yz}) for the capped Cu TSV with respect to depth. The uncertainties result from uncertainties in the diffracted X-ray peak positions on the area detectors and uncertainties in the lattice spacing determination.

≈ 51 MPa was observed at a depth of ≈ 47.5 μm . This means that the stresses in the uncapped Cu TSV are much higher than those in the capped TSV, with average hydrostatic stress across the lengths of the capped and the uncapped Cu TSVs of $(89 \pm 28$ MPa) and $(145 \pm 37$ MPa), respectively.

From the FEM results presented in Fig. 6, it was shown that the impact of SiO_2 cap thickness is limited to a depth of ≤ 5 μm . This means that the measured differences in stress values between the capped and the uncapped Cu TSVs are not related to their capping state, but are attributed to their microstructural differences. This claim is supported by the FIB-SEM shown in Fig. 1(b), in which it was observed that the grain sizes, as well as the distribution of twin boundaries in the three adjacent Cu TSVs are dissimilar. Additionally, the grain orientation analysis of the two Cu TSVs (Table I), also show a variation in their grain orientation, which is expected to significantly influence their stress state. While the FEM results (Fig. 6) indicate that compressive stresses were anticipated at the top region of the TSV, we were unable to confirm this by the microdiffraction measurements, as no measurements were obtained within the initial 5 μm of the two Cu TSVs, due to large plastic deformation within this region.

D. Shear Stresses

The shear stress data for the capped Cu TSV are shown in Fig. 9, and no clear trend with depth is observed. The shear stress components in the uncapped Cu TSV were observed to be overlapping with the exception of the shear stresses at 22.5- μm depth, where the S_{yz} component is an outlier. The absolute mean shear stresses across the entire length of the capped Cu TSV is about ≈ 22 MPa, with a minimum value of ≈ 10 MPa observed within the top 12.5- μm region. Deeper within the capped Cu TSV, their absolute shear stress values were larger, with the maximum shear stress of ≈ 80 MPa occurring at the center of the capped Cu TSV (22.5- μm depth). The observed apparent randomness in the shear stress data are likely related to its microstructure. Additionally, the observed shear stress values may be influenced by the undetermined exact measurement location across the diameter of the Cu TSV.

On the other hand, the shear stresses in the uncapped Cu TSV show a clear trend, as shown in Fig. 10. From about 17.5–47.5- μm depth, the different shear stress components

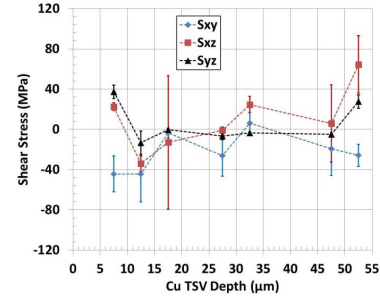


Fig. 10. Experimental shear stress components (S_{xy} , S_{xz} , and S_{yz}) for the uncapped Cu TSV with respect to depth. The uncertainties result from uncertainties in the diffracted X-ray peak positions on the area detectors and uncertainties in the lattice spacing determination.

were observed to be overlapping, having approximately constant absolute mean values of about ≈ 10 MPa. However, the ends of the uncapped Cu TSV showed large variation between them, with nonoverlapping one-sigma uncertainties and much higher shear stresses with mean absolute value of about ≈ 35 MPa. This trend in the profile of the shear stresses in the uncapped Cu TSV correlates with reported FEM-based studies [4].

E. Estimation of the Impact of Cu TSV Stress on FinFET Performance

Stress in the Si matrix is known to be induced by the presence of the Cu TSV. Based on the microdiffraction measurements, we have determined the stress in the Cu TSV (σ_{TSV}). Due to the cylindrical nature of the TSV, a solid cylinder formulation based on the Lamé approximation can be used for the calculation of the stress in the Si. Based on this formulation

$$\sigma_{S_{ir}} \approx -\sigma_{S_{i\theta}} \approx \sigma_{\text{TSV}} \cdot \left(\frac{\emptyset}{2r}\right)^2. \quad (1)$$

This means that the radial Si stress is equal in magnitude to the circumferential Si stress, although in opposing directions. Since σ_{TSV} is known, the in-plane stress in the Si can be determined. In (1), r is the distance from the center of the Cu TSV, while \emptyset is the diameter of the Cu TSV. From the measurement results in Figs. 7 and 8, σ_{TSV} is in a tensile hydrostatic stress state. FinFETs are usually located at the top region of Si (< 2 μm from the top); as we have no data from the top 5 μm of the TSV, the hydrostatic stress values at the 7.5 μm depth were used. σ_{TSV} stress values for the capped Cu TSV and the uncapped Cu TSV are 67 and 211 MPa, respectively. The in-plane stress components in the cylindrical coordinate system can be transformed to the Cartesian system using (2) and (3), θ is the angle between the x -axis and r

$$\sigma_{S_{ixx}} = \sigma_{\text{TSV}} \cdot (\cos^2 \theta - \sin^2 \theta) \cdot \left(\frac{\emptyset}{2r}\right)^2 \quad (2)$$

$$\sigma_{S_{iyy}} = \sigma_{\text{TSV}} \cdot (\sin^2 \theta - \cos^2 \theta) \cdot \left(\frac{\emptyset}{2r}\right)^2. \quad (3)$$

In this paper, the channel direction of the FinFET is parallel to the radius (r) from the center Cu TSV, simplifying the

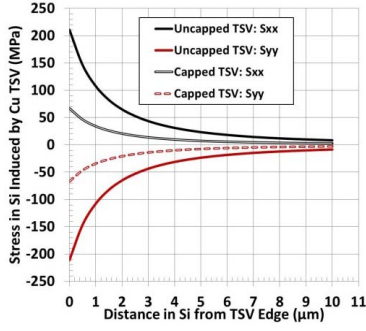


Fig. 11. Calculated induced stresses in the surrounding Si for the capped and the uncapped Cu TSV, as a function of distance from the edge of the TSV.

previous equations to just (4) and (5)

$$\sigma_{Si_{xx}} = \sigma_{TSV} \cdot \left(\frac{\emptyset}{2r}\right)^2 \quad (4)$$

$$\sigma_{Si_{yy}} = -\sigma_{TSV} \cdot \left(\frac{\emptyset}{2r}\right)^2. \quad (5)$$

Stress fields in Si lead to a change in the carrier mobility of the FinFET, which is determined by the change in the drain current [14]–[17]. By knowing the effective piezoresistivity coefficients (π') of the Si, the first approximation effect of stress on the change in drain current of the FinFETs can be determined as [17]

$$\frac{\Delta I_d}{I_d} = -(\sigma_{Si_{xx}} \cdot \pi'_{11} + \sigma_{Si_{yy}} \cdot \pi'_{12}) \quad (6)$$

π'_{11} and π'_{12} are the effective piezoresistivity coefficients in the longitudinal and transverse directions, respectively. The values used in this paper are $\pi'_{11} = 120$ ppm/MPa, $\pi'_{12} = -230$ ppm/MPa for p-FinFET devices, and $\pi'_{11} = -298$ ppm/MPa, $\pi'_{12} = -18$ ppm/MPa for n-FinFET devices [16]. Using (6), the KOZ of the transistor is determined. In this paper, the allowed change in the drain current is assumed to be $\pm 5\%$ [1], [6]. This value determines the allowed proximity of the FinFETs to the Cu TSV for the capped and uncapped Cu TSVs.

It is worth noting that the KOZ calculation based on effective piezocoefficient values, as used in this paper is simplistic. Other possible contributors to the KOZ such as access resistance, mobility saturation and strain engineering were not considered.

Fig. 11 shows the calculated in-plane induced stress in the Si surrounding the capped and the uncapped Cu TSV. From these results, it is obvious that the maximum stresses in the Si occurs close to the edge of the Cu TSV and continuously decreases away from the Cu TSVs. Also, lower stresses in the Cu TSV translates to lower stresses in the Si; for this reason, the Si surrounding the uncapped Cu TSV witnesses higher stresses than its counterpart, the capped Cu TSV.

In Fig. 12, the calculation of the change in the drain current of the p-FinFET and the n-FinFET follow a similar trend as the stress results (Fig. 11). This means that the performance of both p- and n-FinFET devices placed close to the TSV edge will witness much higher variation than if placed far

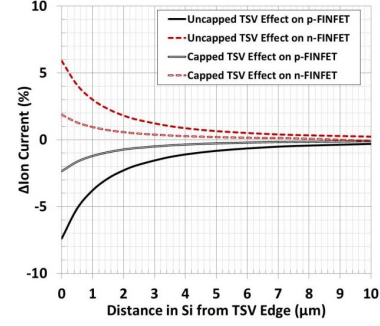


Fig. 12. Calculated change in the drain current for the p- and n-FinFET as a function of their proximity to the TSV.

from the Cu TSV. The lower stress in the uncapped Cu TSV results in a minimal change in the drain current for devices, as compared with the uncapped Cu TSV. With the assumption of 5% drain current change tolerance, the KOZ for the p- and n-FinFET surrounding the uncapped Cu TSV were estimated to be 0.6 and 0.2 μm , respectively. On the other hand, the KOZ for the p- and n-FinFET surrounding the capped Cu TSV is 0 μm . The low estimated KOZ values are related to the lower stresses in the Cu TSV and the used piezoresistivity coefficients.

From this paper, it is also obvious that the n-FinFET devices can be placed closer to the Cu TSV than the p-FinFET devices; this is due to the lower sensitivity of n-FinFET devices to the presence of stress, as their piezoresistivity coefficient values are three times lower than the p-FinFET devices.

It can also be inferred from this result that the KOZ is greatly influenced by local effects such as microstructural differences in the Cu TSVs. Thus, on a wafer, the KOZ values are expected to vary widely and an accurate KOZ design rule ought to be based on a statistical pool of accurately measured Cu TSV and Si stress data.

IV. CONCLUSION

In this paper, we presented a nondestructive, depth-resolved determination of the full stress tensor in Cu TSVs, using a synchrotron-based, X-ray microdiffraction technique. Two adjacent Cu TSVs, one capped with SiO_2 (0.17 μm) and the other without, were used for this paper. Additionally, the stresses in the surrounding Si, as well as the FinFET KOZ were estimated. FEM was used to evaluate the impact of SiO_2 cap thickness on the stresses in the Cu TSVs.

From the microdiffraction experiment, it was found that the stress in the uncapped Cu TSV (145 ± 37 MPa) was higher than that in the capped Cu TSV (89 ± 28 MPa). This disparity was attributed to the differences in their microstructure, resulting from their grain orientation dissimilarities.

FEM analysis showed that only the stresses at the top region (≤ 5 μm) of the Cu TSV increased with SiO_2 cap thickness, being the region where the stresses were not experimentally determined. This further affirms that the measured difference in the stresses of the two Cu TSVs is not related to their capping state, but to their microstructure.

Based on the experimentally determined stress in the Cu TSVs, the stresses in the surrounding Si were calculated, as well as the KOZ of FinFETs. The changes in the drain current of the p-FinFET devices were found to be influenced much more by the presence of stress fields than their n-FinFET counterpart. Additionally, the variation in the microstructure of the Cu TSVs, which influence their stress state, leads to variations in the KOZ of FEOL devices. Therefore, in setting up KOZ design rules, the localization and the variability in the Cu TSVs and the surrounding Si ought to be accounted for.

REFERENCES

- [1] C. Okoro *et al.*, "Analysis of the induced stresses in silicon during thermocompression Cu-Cu bonding of Cu-through-vias in 3D-SIC architecture," in *Proc. 57th ECTC*, Reno, NV, USA, May/Jun. 2007, pp. 249–255.
- [2] X. Liu, Q. Chen, V. Sundaram, R. R. Tummala, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free standing wafer under thermal-shock test," *Microelectron. Rel.*, vol. 53, no. 1, pp. 70–78, 2013.
- [3] C. Okoro *et al.*, "Elimination of the axial deformation problem of Cu-TSV in 3D integration," in *Proc. 11th Int. Workshop, AIP Conf. Stress-Induced Phenomena Metallization*, vol. 1300, Nov. 2010, pp. 214–220.
- [4] C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng, "A detailed failure analysis examination of the effect of thermal cycling on Cu TSV reliability," *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 15–22, Jan. 2014.
- [5] A. Mercha *et al.*, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-*k*/metal gate CMOS performance," in *Proc. IEEE IEDM*, San Francisco, CA, USA, Dec. 2010, pp. 2.2.1–2.2.4.
- [6] C. Okoro *et al.*, "Extraction of the appropriate material property for realistic modeling of through-silicon-vias using μ -Raman spectroscopy," in *Proc. IITC*, San Francisco, CA, USA, May 2008, pp. 16–18.
- [7] C. Okoro, "Thermo-mechanical characterization of copper through-silicon via interconnect for 3D chip stacking," Ph.D. dissertation, Dept. Mech. Eng., Katholieke Univ. Leuven, Leuven, Belgium, Dec. 2010.
- [8] A. S. Budiman *et al.*, "Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits," *Microelectron. Rel.*, vol. 52, no. 3, pp. 530–533, Mar. 2012.
- [9] T. Jiang *et al.*, "Characterization of plasticity and stresses in TSV structures in stacked dies using synchrotron X-ray microdiffraction," in *Proc. IEEE 63rd ECTC*, Las Vegas, NV, USA, May 2013, pp. 641–647.
- [10] C. Okoro *et al.*, "X-ray micro-beam diffraction determination of full stress tensors in Cu TSVs," in *Proc. IEEE 63rd ECTC*, Las Vegas, NV, USA, May 2013, pp. 648–652.
- [11] B. C. Larson, W. Yang, G. E. Ice, J. D. Budai, and J. Z. Tischler, "Three-dimensional X-ray structural microscopy with submicrometre resolution," *Nature*, vol. 415, no. 6874, pp. 887–890, 2002.
- [12] L. E. Levine *et al.*, "Disordered long-range internal stresses in deformed copper and the mechanisms underlying plastic deformation," *Acta Mater.*, vol. 59, no. 14, pp. 5803–5811, 2011.
- [13] L. E. Levine, C. Okoro, and R. Xu, "Full elastic strain tensor measurements from individual dislocation cells in copper through Si vias," In preparation.
- [14] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954.
- [15] Y. Kanda and K. Yozo, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Trans. Electron Devices*, vol. 29, no. 1, pp. 64–70, Jan. 1982.
- [16] W. Guo *et al.*, "Copper through silicon via induced keep out zone for 10 nm node bulk FinFET CMOS technology," in *Proc. IEEE IEDM*, Washington, DC, USA, Dec. 2013, pp. 12.8.1–12.8.4.
- [17] E. Beyne, "Electrical, thermal and mechanical impact of 3D TSV and 3D stacking technology on advanced CMOS devices—Technology directions," in *Proc. 2011 IEEE Int. 3DIC*, Osaka, Japan, Jan./Feb. 2012, pp. 1–6.

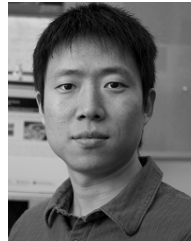


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