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Defect and microstructural evolution in thermally cycled Cu through-silicon vias

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ABSTRACT

In this study, the effect of thermal cycling on defect generation, microstructure, and RF signal integrity of blind Cu through-silicon vias (TSVs) were investigated. Three different thermal cycling profiles were used; each differentiated by their peak cycling temperature (100 °C, 150 °C, 200 °C) and the time needed to complete one cycle (cycle time). The study was performed on two Cu TSV wafer sample types; one containing large processing-induced voids (voided sample), the other without (non-voided sample). It was found that the RF signal return loss $|S_{11}|$ of the Cu TSVs increased upon thermal cycling for both the voided and the non-voided sample types. This was attributed to the increase in the void area due to the formation of new voids, rather than the growth of preexisting voids. On the other hand, the grain orientation and grain sizes of the Cu TSVs were found to be unaffected by all studied thermal cycling conditions and sample types.

1. Introduction

Three-dimensional stacked integrated circuits (3D-SIC) popularity has grown due to their superior performance over planar electronic devices. Through-silicon vias (TSVs) are becoming widely used in electronics as a conduit for transmitting current between chips in this new era of (3D-SIC) devices.

TSVs are typically embedded into a silicon (Si) substrate through a multi-step, multi-material fabrication process. A typical TSV consists of three layers of material; an isolation liner, a barrier layer, and conduction layer. The innermost conduction layer is made of materials such as Cu, W, or poly-silicon; Cu is preferred due to its high electrical conductivity [1]. The isolation liner is typically made of a silicon oxide, such as tetraethyl orthosilicate (TEOS), to prevent current from leaking into the substrate. The barrier layer is sandwiched between the isolation liner and conduction layer to inhibit the conduction layer (e.g. Cu) from diffusing into the isolation liner, and subsequently into the substrate. In the case of Cu-filled TSVs, the Cu is electro-chemically deposited (ECD) into deep reactive ion etched (DRIE) trenches, following the deposition of the isolation and the barrier layers. Differential deposition rates associated with the employed bottom-up deposition (the filling of the bottom of the via at a faster rate than the deposition of Cu on the via sidewalls) has been shown to produce void-free TSVs compared to traditional conformal deposition, which can result in voids in the as-formed TSV [2–5].

Thermo-mechanical reliability is a major concern for TSVs due to stress buildup from applied heat during the chip fabrication process and subsequent device use. For example, the mismatch in the coefficient of thermal expansion (CTE) between the Cu and surrounding layers within the TSV, including the Si substrate, can cause the Cu to expand and contract more rapidly than the Si with temperature, leading to the buildup of stresses. These stresses subsequently lead to the formation and growth of voids in TSV, interfacial delamination and crack propagation in Si. The stresses in the substrate (Si) have been measured using Raman spectroscopy [6]. In recent times, the stresses in the Cu TSVs have been successfully quantified using a synchrotron-based X-ray micro-diffraction technique [7–10]. For instance, Shin et al. in their study, found that the formation of voids in Cu TSVs due to annealing treatment results in the reduction of the hydrostatic stresses in the Cu TSVs [8]. This is in agreement with other reported studies that observed that voids and other defects form as a stress relief mechanism and grow with increasing temperature budget [11]. It has also been shown that voids induce radio-frequency (RF) signal scattering, which can deteriorate the integrity of the TSVs by distorting signals and

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increasing electrical resistance [12,13]. Thermo-mechanical stresses can also cause the Cu to protrude out of the trenches in the out-of-plane direction. This process can be detrimental to any layers deposited atop the TSVs, such as layers added during back end of the line (BEOL) processing steps [14]. Studies have shown that the height of such protrusions increase with temperature upon holding from 250 °C to 450 °C for up to 30 min [14–17]. Kumar et al. attributed the expansion, after isothermal holds and cycling at elevated temperatures, to interfacial sliding caused by the stresses between the Cu and the surrounding Si substrate [16].

Semiconductor devices can undergo many cycles of temperature depending on their environment of use and device operating temperatures are typically rated according to their intended application. While most commercial and industrial products are rated to function up to maximum temperatures below 100 °C, some applications, such as in military and automotive systems, require higher temperature tolerance [18]. Microstructure and defect changes in Cu TSVs have been studied extensively for isothermal exposures, as well as under long interval thermal cycling aimed at replicating back end of the line (BEOL) integration temperatures and other fabrication processes [8,11,15,19]. However, limited pre- and post-cycling evaluation has been done to simulate the multiple-cycle conditions these structures may be exposed to in use. The reported TSV thermal cycling studies were all performed using only one thermal cycling profile [13,20,21].

The present study focuses on the use of multiple thermal cycling profiles, with maximum peak cycling temperatures between 100 °C and 200 °C to investigate RF signal degradation and morphological changes in Cu and its surrounding materials. This study was performed on two different types of TSV-containing wafers; TSVs containing processing induced voids and non-voided TSVs. A correlation between the RF signal integrity measurements and the morphological changes in the Cu TSV due to thermal cycling was achieved [22].

2. Experimental procedure

For this work, two commercial types of TSV-containing Si wafers were evaluated. While details of the specific TSV fabrication processes are not known, the two sample sets are known to differ in the age of the Cu electro-chemical deposition (ECD) bath that was used in TSV fabrication. In one set of samples, copper was deposited using a fresh ECD bath; in the second set, the bath had been previously used and thus was potentially contaminated with process-related by products and moisture. As discussed below, variation in morphology within the Cu TSVs resulting from the "fresh" and "aged" baths, are clearly visible as shown in Fig. 1. It can be seen that the TSV filled with Cu from the aged ECD bath (Fig. 1a), clearly shows visible seams, large bottom voids, and smaller micro-voids. These defects were routinely observed in the many (100's) of TSVs examined from this lot of samples. In comparison, the TSV fabricated from the fresh ECD bath (Fig. 1b) exhibited no seams or large voids, and contain much smaller numbers of micro-voids. In the context of this analysis, micro-voids observed are nominally 1 μm or less in diameter. In this paper we differentiate between the two wafer types as follows, the wafers containing TSVs fabricated with the aged bath, which possess higher defect/void area, will be denoted as the voided (V) samples and the TSVs made from fresh ECD bath, with lower/smaller void numbers/area will be labeled as non-voided (NV) samples. Both TSV-containing wafer types contained blind Cu TSVs with an approximate size of 5.5 μm in diameter and 50 μm in depth. The studied TSVs were a group of 6 × 6 arrays that are covered by Cu bond pads as seen in Fig. 2, the approximate locations of the TSVs underneath the bond pads are outlined. These bond pads were configured in rows of 12 on the Si substrate.

For completeness, the thermal histories of the samples during their fabrication are discussed. Both the non-voided and voided samples underwent the same heat treatment conditions. After TSV electroplating, the wafers were annealed at 150 °C for 1 h. This is followed by front-side dielectric and etch-stop deposition heat treatment of about 2 min at 350 °C and 400 °C, respectively. After

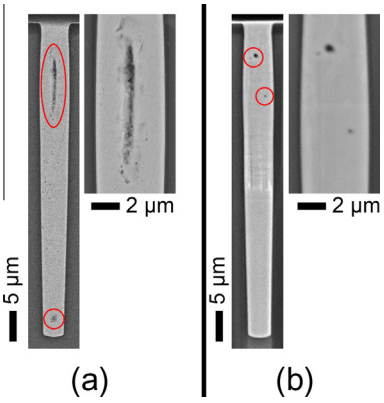

Fig. 1. SEM images of the as-received (a) voided (V) and (b) non-voided (NV) samples. Clearly visible are seams and large bottom voids in the voided (V) samples (the circles are shown as a guide to the eye) and the much smaller micro-voids found in the non-voided (NV) samples.

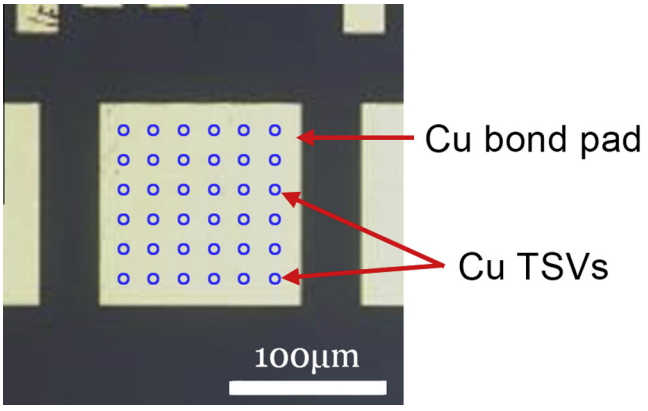

Fig. 2. Top of a typical sample containing Cu bond pads with the approximate underlying positions of the TSVs indicated by the circles.

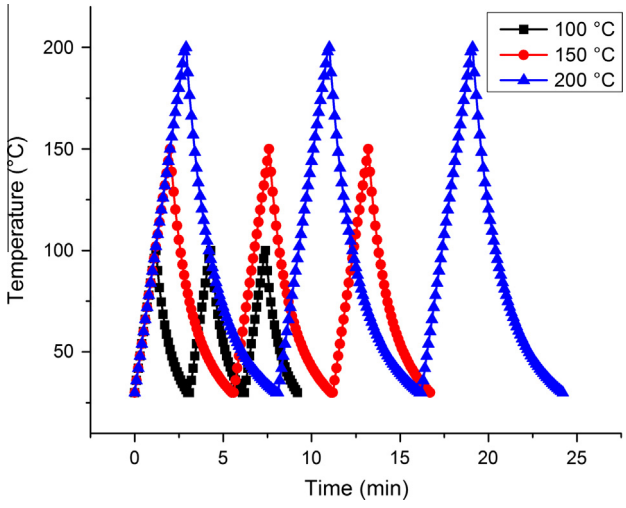

Fig. 3. The three thermal cycling profiles used in this study. Each thermal cycling profile is differentiated by their maximum peak cycling temperature (100 °C, 150 °C, and 200 °C) and the time it took to complete each thermal cycle.

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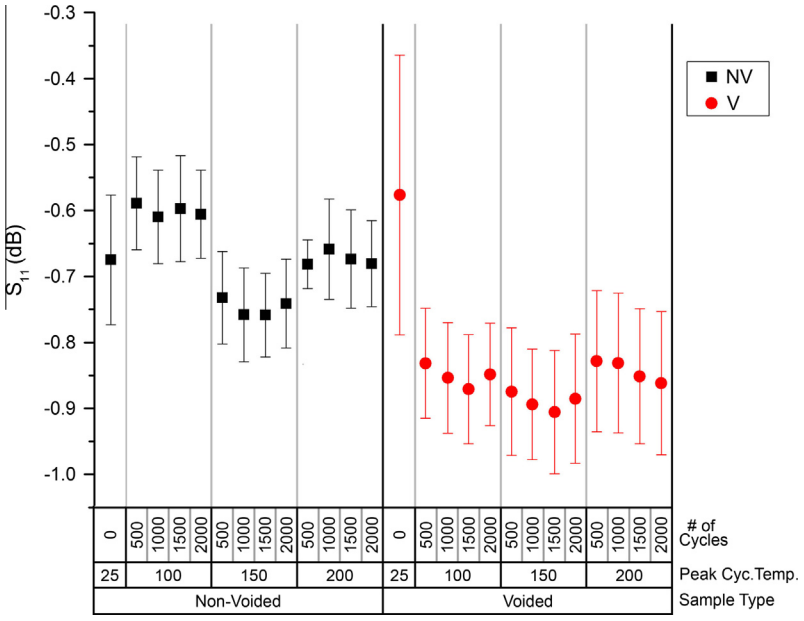

Fig. 4. A chart of the average return loss $|S_{11}|$ at 10 GHz for the different cycling conditions (number of cycles and maximum peak cycle temperature).

front-side metallization, the structure was annealed at 150 °C for 1 h. These stated conditions, represents the thermal history of the as-received sample used in this work.

In this paper, all the reported uncertainties in the results are one standard deviation of the reported arithmetic mean (sigma). The data variability is a composite of sample-to-sample variability and systematic experimental variability.

2.1. Thermal cycling and RF-based measurements

To simulate and reproduce *in-use* conditions that chips in components might encounter, samples were thermally cycled up to 2000 times from room temperature to peak cycling temperatures of 100 °C, 150 °C, or 200 °C. Fig. 3 shows the temperature profiles for the three thermal cycling conditions. The duration of a single cycle depends on peak cycling temperature, being approximately 3 min, 5.5 min, and 8 min for the 100 °C, 150 °C, and 200 °C peak cycling temperatures, respectively. The cycling was carried out in laboratory air ambient within a cycling chamber. Prior to and following defined thermal cycles, the RF-based signal integrity measurements were performed on the blind TSV-containing dies, and after every 500 thermal cycles for up to 2000 cycles, using a vector network analyzer (VNA). From these measurements, the changes in the magnitude of the reflection coefficient or the return loss $|S_{11}|$ were determined with respect to the noted number of thermal cycles. An Agilent VNA model, the PNA N5230A[1], was used as the RF generator and analyzer. The measured value of the return loss $|S_{11}|$ represents the total signal return loss from the array of 6×6 TSVs underneath a Cu bond pad as shown in Fig. 2. Propagation behavior under each stated measurement condition was evaluated for ten bond pads. Measurements were performed at a broad frequency range from 700 MHz to 40 GHz; however, only data at 10 GHz was used in assessing the impact of sample cycling conditions. Due to the multiplicity of TSVs per bond pad, it was not possible to explicitly identify individual TSVs for direct pre- and post-cycle comparison; hence, an assumption was made that representative TSVs within a common chip were similar and would undergo representative changes with fixed thermal excursions and a defined number of cycles.

2.2. Defect and microstructure analytical techniques

Scanning electron microscopy (SEM) and focused ion beam (FIB) imaging of the TSV cross-sections were used to image the sectioned TSVs pre- and post-thermal cycling in order to investigate grain morphology characteristics along with indication of void presence and growth. All TSVs were cross-sectioned to their centers to evaluate identical areas of each TSV for defect and microstructural changes. Void area was calculated by determining the total area of voids per TSV at each condition and void size was measured from the average length and width of every void in the TSVs. While the SEM images provided a clear distinction of the void boundaries, the FIB's excellent grain contrast imaging capability permitted the correlation between the location of the voids and the Cu microstructure. For the microstructural analysis, electron backscattering diffraction (EBSD) has been utilized to ascertain grain sizes and orientations. The FIB-prepared cross-sections permitted distinct diffraction patterns for EBSD mapping to be obtained on post-cycled samples. Inverse pole figures (IPF) and grain size maps have been used to study the Cu orientation and average grain size, respectively. General trends in these features were quantified as a function of thermal cycles and maximum peak thermal cycling temperatures. Again, as stated above, while direct TSV-to-TSV comparisons were not examined, the goal of our study was to develop fabrication methods which would allow us to identify, qualify, and, where possible, quantify general trends in morphological features that occur with cycling for TSVs produced from fresh and aged ECD baths. At least four TSVs per cycling condition were examined, with 100's of voids and grains analyzed to form the conclusions stated in this study.

3. Results and discussion

3.1. Radio frequency signal integrity of blind Cu TSVs

To understand and quantify the RF signal degradation in the blind TSVs as a function of defect concentration, fabrication

[1] Certain commercial equipment, instruments, or materials are identified in this paper to specify experimental or theoretical procedures. Such identification does not imply recommendation by NIST nor the authors, nor does it imply that the equipment or materials are necessarily the best available for the intended purpose.

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method, and thermal cycling history, samples were mounted on a VNA to measure the reflection coefficient (S_{11}), also known as return loss. The return loss S_{11} measures the ratio of the reflected signal to the incident signal; only the real part (or magnitude), $|S_{11}|$, is reported in this study. The return loss $|S_{11}|$ was the only measured parameter since the TSVs used in this study were blind, and were not designed for signal transmission. This means that in the perfect situation, 100% of the incident signal is expected to be reflected (0 dB), as there is no signal transmission. On the other hand, the presence of discontinuities, such as defects, is expected to lead to the absorption or the scattering of the incident RF signal, resulting in partial reflection of the signals. The $|S_{11}|$ data at 10 GHz for each thermal cycling condition is shown in Fig. 4. Depicted are variations in the return loss $|S_{11}|$ with cycle number, for both voided (V) and non-voided (NV) sample sets. For each cycling condition, the same 10 bond pads were measured on four separate samples, and since 36 TSVs lay underneath each bond pad, every point in Fig. 4 is a culmination of at least 1440 TSVs.

Several general trends can be seen from the data in Fig. 4. Firstly, prior to thermal cycling, the voided (V) and non-voided (NV) samples show similar levels of 'as-fabricated return loss', with large (~20%) error bars. This result indicates that even within a fixed fabrication protocol, a wide range of resulting morphology in the Cu structures exist, resulting in similar return loss $|S_{11}|$ behavior between the voided (V) and non-voided (NV) samples. Deviation in performance between the sample types become more apparent once cycling occurs; sample type and maximum peak cycling temperature are clearly shown to influence resulting $|S_{11}|$ performance, especially in the NV samples. Upon cycling, it is apparent that the higher void content of the voided (V) samples show more return losses than the non-voided (NV) samples. As noted above, defects, specifically voids, can act as scattering centers and have been shown to degrade electrical performance in conductors [13,14,23]. This is what we believe is influencing the observations seen here. While no distinct trends can be seen with increasing number of cycles, the maximum peak cycling temperature appears to play a role in the return loss $|S_{11}|$, at least in the non-voided (NV) samples, as the increase in the peak cycling temperature induces more return losses except for peak temperature of 200 °C. Interestingly, the return loss $|S_{11}|$ of the voided (V) samples appear to remain fairly unchanged with varying maximum peak cycling temperatures.

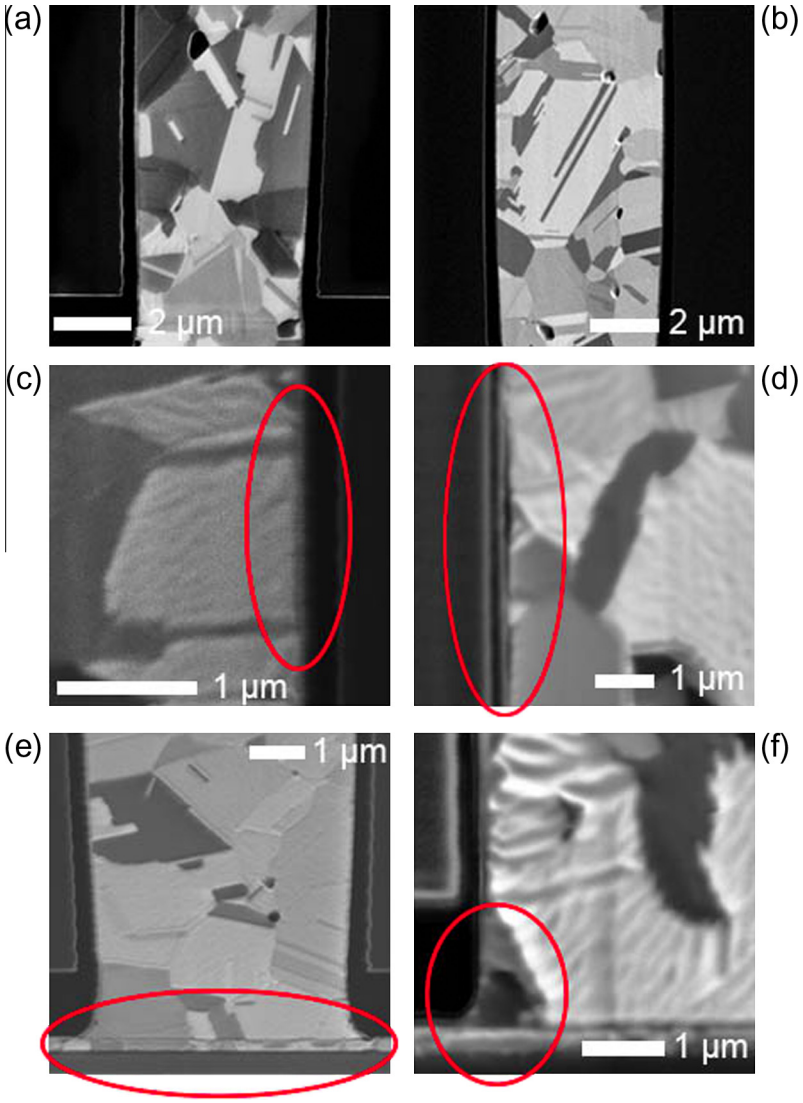

Fig. 5. FIB micrographs comparing the growth of defects in the Cu TSV structure for the as-fabricated and after 2000 cycles, using a thermal cycling profile, with maximum peak temperature of 150 °C, for the non-voided (NV) sample type. Voids in Cu TSV (a) As-fabricated, (b) after 2000 cycles. TSV sidewall integrity (c) as-fabricated, (d) after 2000 cycles. TSV–Cu bond pad integrity, (e) as-fabricated, (f) after 2000 cycles.

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Since the number of cycles in the above data was shown to have little influence on the signal integrity of the TSVs, only the as-fabricated and 2000 cycled samples were chosen for subsequent SEM evaluation for defect and microstructural changes. These analyses are reported in the subsequent section.

3.2. Observation of defects caused by thermal cycling

Fig. 5 presents FIB images of the defects in Cu TSV for the non-voided (NV) sample type pre- and-post thermal cycling (2000 cycles). Voids were observed in all Cu TSVs examined, for both the pre- and-post thermal cycling samples, as shown in Fig. 5a and b respectively. Inspection of the micrographs reveals that most voids are located at grain boundary triple junctions and at twin boundaries. These voids were presumably formed as a stress relief mechanism due to the anisotropic nature of Cu [8,11]. This argument is consistent with prior observations that indicate that grain boundaries serve as a pathway for vacancy/void migration [24]. The observation of voids before thermal cycling, particularly in the non-voided samples, suggests that voids were generated during the Cu TSV fabrication process and thermal cycling lead to the further nucleation of voids as shown in the succeeding section in Fig. 6 and Table 1.

Additionally, thermal cycling was found to lead to the formation of other new defects in the Cu TSV, such as the sidewall delamination (Fig. 5d) and crack growth along the Cu bond pad – TSV interface (Fig. 5f). These new defect types were not present in the samples before thermal cycling, as shown in Fig. 5c and e. Similar defects types were also observed by [20], and they were attributed to the buildup of stresses in the structure due to the thermal cycling process.

These defects are anticipated to impact RF performance of the TSVs as they act as discontinuities in the structure, serving as signal scattering centers, which could result in the deterioration of the return loss $|S_{11}|$ signals [13].

In an attempt to quantify the size of voids as a function of thermal cycling, extensive image analysis was carried out on TSV cross-sections. Fig. 6 and Table 1 summarize the change in the measured percentage void area and average void size in the TSVs, respectively, as a function of the maximum peak cycling temperature and the sample type. As mentioned in Section 2.2, void areas were measured using SEM micrographs of the FIB cut specimens. The percentage void area was calculated with respect to the total TSV cross-sectional area, which is identical for all samples evaluated.

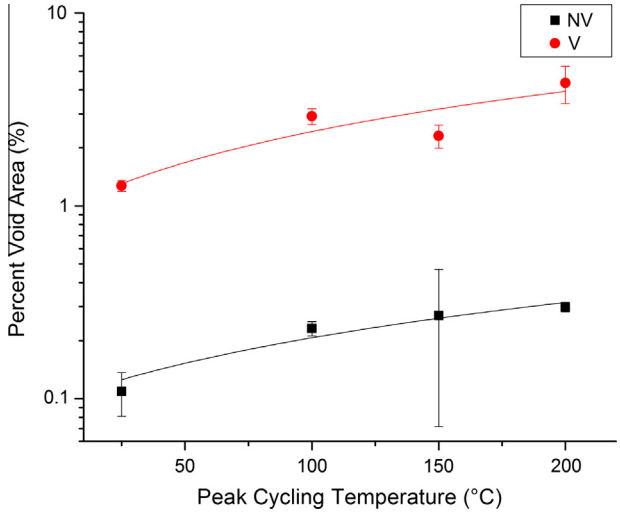

Fig. 6. Evolution of the percentage void area in the TSVs with maximum peak cycling temperature for voided (V) and non-voided (NV) specimens.

As shown in Fig. 6, the TSVs of the voided samples have a percentage void area that is an order of magnitude higher than that of the non-voided samples as quantified by microscopic evaluation. It must be emphasized that only general trends are reported here as the pre- and post-cycle (2000 cycles) analyses were not carried out on the uniquely tracked TSVs, but on the ensembles of TSVs.

Fig. 6 shows that thermal cycling increased the void area by at least ~2X over that seen in the as-fabricated TSVs for both the voided and the non-voided sample types. The absolute sizes of voids are much larger for TSVs of the voided sample type. The measured void area also scales with the maximum peak cycling temperature for both wafer types, extending from $0.22 \pm 0.06\ \mu m^2$ and $2.62 \pm 0.17\ \mu m^2$ for the as-fabricated wafers to $0.62 \pm 0.03\ \mu m^2$ and $8.94 \pm 1.96\ \mu m^2$ after 2000 cycles at a maximum peak cycling temperature of 200 °C for the non-voided and voided samples, respectively.

As shown in Table 1 and consistent with Fig. 6, the average void sizes in the voided samples are larger than the non-voided samples due to the contributions of the seams and bottom voids that are absent in the non-voided samples. The lack of significant void size increases in the TSVs after cycling indicates that new void formation is possibly contributing to the void area increases seen in Fig. 6. This observed increase in void nucleation with the peak

Table 1
Average void size under various maximum peak cycling temperature conditions.

Peak cycling temperature	Non-voided samples	Voided samples
Un-cycled	0.19 ± 0.04 μm	0.68 ± 0.02 μm
100 °C	0.33 ± 0.11 μm	1.06 ± 0.23 μm
150 °C	0.37 ± 0.20 μm	1.15 ± 0.47 μm
200 °C	0.27 ± 0.02 μm	1.04 ± 0.23 μm

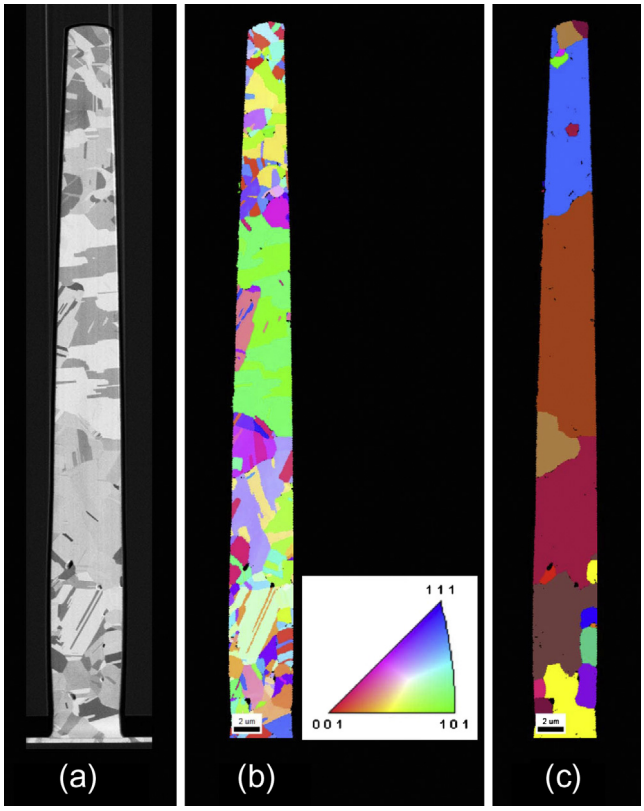

Fig. 7. The maps and images used to examine microstructure in the Cu TSVs including (a) Focused ion beam image, (b) inverse pole figure (IPF), and (c) grain size map. This specific TSV shown in all three images is from a non-voided sample set cycled 2000 times using a maximum peak cycling temperature of 100 °C.

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thermal cycling temperature is attributed to the increase in stress concentrations at the grain and twin boundaries of the Cu TSV, caused by the elastic anisotropy of its microstructure. The stresses generated in the Cu TSVs for peak thermal cycling temperatures of 200 °C is expected to be two times higher than that performed at a peak thermal cycling temperature of 100 °C. The increase in the stresses, results in higher stress gradients in the polycrystalline Cu TSV. This serves as a driving force for the increased nucleation sites of voids at higher peak thermal cycling temperatures. This is in agreement with the studies performed by Kong et al.; their X-ray images showed that void nucleation sites increased with higher annealing temperatures [11]. On the other hand, void growth is governed by vacancy diffusion, thus is rate-controlled [11,25]. In our studies, no soak-time was allowed at the peak thermal cycling temperatures, as such, possible void growth was hindered, as is shown in Table 1.

The larger average void area in the voided samples appears to correlate with the measured RF signal integrity data; measurements showed that the void-containing samples (V) had more return loss $|S_{11}|$ compared to the non-voided (NV) samples, which contained smaller voids and void areas. The formation of voids with increasing maximum peak cycling temperature leads to larger void areas and corresponds to the higher return loss observed after thermal cycling; this correlates directly with what was observed in the $|S_{11}|$ measurements.

3.3. Thermal cycling effects on Cu microstructure

The microstructure of the thermally cycled TSVs have been characterized in the present study using the EBSD maps, shown in Fig. 7 alongside a FIB image of the same TSV. The three maps shown in Fig. 7 are representative of all the TSVs examined. Fig. 7a illustrates a micrograph of a non-voided TSV obtained with the FIB system which has undergone 2000 cycles with a maximum peak cycling temperature of 100 °C; an IPF image (Fig. 7b) of the same TSV, assigns a color map to the grain orientations. The grain size map in Fig. 7c has been modified from Fig. 7b to exclude the twin boundaries present and allow straightforward grain size measurements.

Fig. 7b shows that color map of the Cu grains are not homogenous all through the Cu TSV, which suggests that the Cu grains are non-preferentially oriented. Further EBSD studies performed for the non-voided and voided samples, respectively in Figs. 8 and 9, clearly show that the Cu TSV microstructure is non-preferentially oriented, irrespective of the used peak cycling temperature. This is in agreement with previously reported studies [15,19,26,27]. Figs. 8 and 9 also indicate that the thermal cycling profiles did not appear to affect the TSVs' overall random orientation.

Likewise, Table 2 indicates that the average grain size of the post thermal cycled samples does not deviate greatly from the 'as-fabricated' samples with the grains of the 'as-fabricated' non-voided samples averaging 2.68 ± 0.68 μm and the voided samples averaging 3.40 ± 0.55 μm before cycling. The Cu grains are large and typically spanned the width of the TSVs, which is optimal for current flow due to the small number of grain boundaries. As previously stated, Cu grain growth has been observed in TSVs under isothermal holding conditions [15], however, this study shows only small changes in microstructure for thermally cycled Cu TSVs. The unchanged grain sizes with thermal cycling in our results can be attributed to the thermal history of the Cu TSVs prior to thermal cycling. As discussed earlier, the Cu TSV wafers underwent fabrication-related heat treatment conditioning, that includes a 2 min

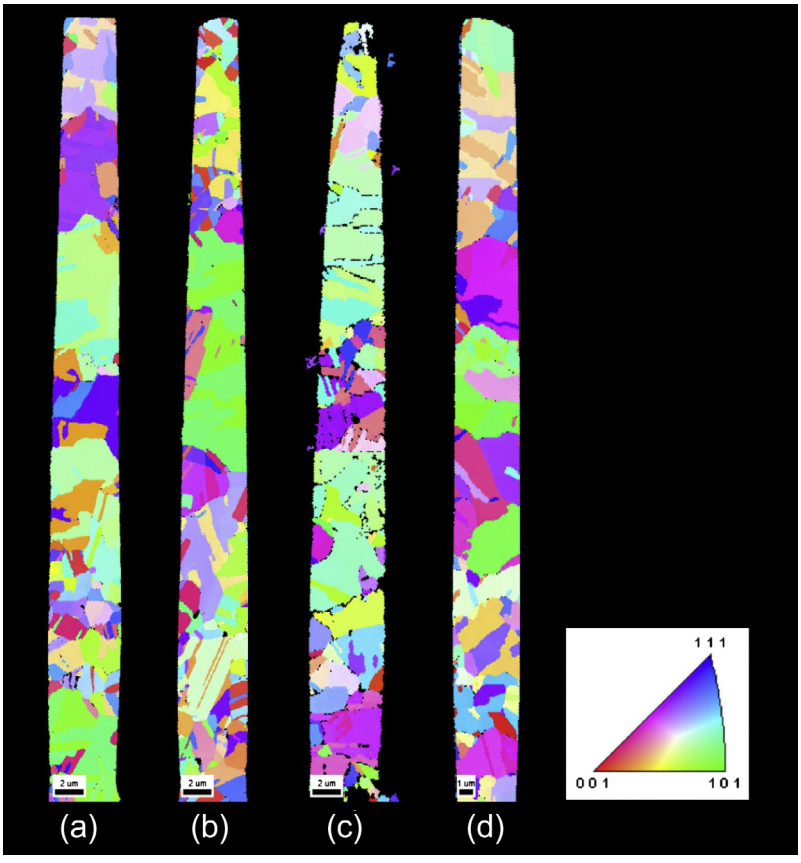

Fig. 8. Examples of the normal direction IPF maps for the non-voided TSVs (a) before thermal cycling and after 2000 cycles with maximum peak cycling temperatures of (b) 100 °C, (c) 150 °C, and (d) 200 °C.

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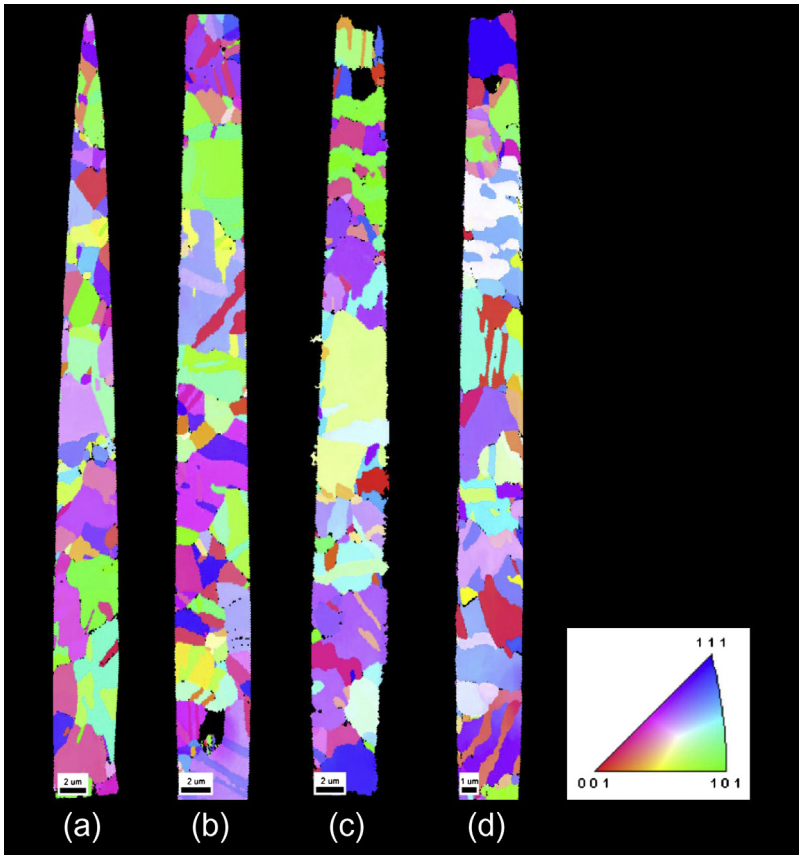

Fig. 9. IPF maps of the (a) as-received and 2000 cycled (b) 100 °C, (c) 150 °C, and (d) 200 °C maximum peak cycling temperature voided sample TSVs.

Table 2
The average grain size for the Cu TSVs before and after cycling at different maximum peak cycling temperatures.

Peak cycling temperature	Non-voided samples	Voided samples
Un-cycled	2.68 ± 0.68 μm	3.40 ± 0.55 μm
100 °C	3.17 ± 0.07 μm	2.19 ± 0.54 μm
150 °C	2.72 ± 1.58 μm	4.37 ± 1.32 μm
200 °C	3.33 ± 0.43 μm	3.74 ± 0.31 μm

heat treatment at a maximum temperature of 400 °C. Heat treatment of Cu at 400 °C is known to result in the growth and stabilization of their microstructure [28], which will lead to decrease total free energy of the grains. This is because grain growth occurs mainly by grain boundary motion, which results in the reduction in the grain boundary area and energy, leading to the increase in the average grain size [19,26]. In order to initiate further grain growth, the driving force required to induce any grain boundary motion, will require higher heat treatment temperature and/or longer time. In this study, the peak thermal cycling temperatures of $\leqslant$200 °C are not sufficient to initiate further growth of the grains. Additionally, the lack of a soak-time at the peak thermal cycling temperatures means that enough time is not allowed for grain boundary diffusion to occur, leading to no further grain growth. The micrographs, such as Fig. 7a, also show the presence of many twins in the TSVs, made evident by the difference between the IPF (Fig. 7b) and grain size maps (Fig. 7c), the latter excluding twins. This is in agreement with reports on the density of twins in electroplated TSVs [8]. While void formation scaled with the maximum peak cycling temperatures (Fig. 6), the grain sizes did not appear to change with the used thermal cycling conditions and preferential orientation was nonexistent in the samples examined.

4. Conclusion

In the present study the RF performance of blind Cu TSVs under thermal cycling conditions (up to 2000 cycles) were analyzed. The Cu TSV structures were subjected to three different thermal cycling profiles, which are differentiated by their maximum peak cycling temperatures (100 °C, 150 °C, and 200 °C) and the time taken to complete a single cycle. Their performance was assessed using RF-based signal integrity measurements and failure analysis studies. Two Cu TSV sample types were evaluated; wafers with large processing-induced voids (V) and wafers consisting of Cu TSVs with minimal voids (NV).

RF signal return loss $|S_{11}|$ showed that the signal integrity of Cu TSVs degraded upon thermal cycling for both the voided and the non-voided sample types. This was attributed to the increase in the void area due to the formation of new voids, rather than growth of preexisting voids. Other defect types such as TSV sidewall delamination and crack growth at the TSV–Cu bond pad interface are anticipated to also contribute to the degradation of the return loss with thermal cycling. The maximum peak cycling temperature was found to influence the return loss $|S_{11}|$ data, especially in the non-voided sample type. The void area in the Cu TSVs was found increase with increasing maximum peak cycling temperature for both Cu TSV sample types.

The microstructural analysis revealed that the grain orientation of Cu TSVs (which were randomly oriented) and their grain size were unaffected by all thermal cycling conditions.

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