Quasi-TEM Model for Coplanar Waveguide on Silicon

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Abstract- This paper compares a simple quasi-TEM model for coplanar waveguide fabricated on moderately doped silicon substrates to measurement. While the coplanar waveguide currents and magnetic fields are unaffected by the substrate, a simple capacitive model can accurately account for the effects of the substrate.

INTRODUCTION

We apply the calibration comparison method [1], [2] to directly measure the resistance $R$, inductance $L$, capacitance $C$, and conductance $G$ per unit length of coplanar waveguide (CPW) fabricated on silicon substrates and show that the model of Fig. 1 accurately determines $C$ and $G$.

Kwong, et al. [3], Seguinot, et al. [4], and Ko, et al. [5] have proposed closed-form expressions for analyzing CPW on silicon substrates. However, the analysis of [3] requires some finite-difference calculations, the models of [3] and [4] neglect the capacitance through the silicon substrate, and Williams, et al. [6] point out some difficulties in the analysis of [5]. Here we compare to measurement the model of Fig. 1, which is based on closed-form expressions from [3], [5], [7], and [8] and accounts for substrate capacitance, conductance, and fringing fields.

MEASUREMENT PROCEDURE

Reference [2] showed how to use the calibration comparison method [1] to accurately determine the inductance $L$, capacitance $C$, resistance $R$, and conductance $G$ per unit length of printed transmission lines. A multiline thru-reflect-line (TRL) calibration [9] measures the line’s propagation constant $\gamma$ directly. A comparison of this calibration, whose reference impedance is equal to the characteristic impedance $Z_0$ of the transmission line [10], to a multiline TRL reference calibration with reference impedance correction [11] determines $Z_0$. Then $L$, $C$, $R$, and $G$ are found from $R+j\omega L = \gamma Z_0$ and $G+j\omega C = \gamma / Z_0$.

In this work we apply this method to CPW fabricated on moderately doped silicon substrates using CPW reference lines fabricated on semi-insulating gallium arsenide. These reference lines had a metal thickness $t$ of 0.5 µm and center conductor width $w$ of 73 µm separated from two ground planes of width $w_g=250$ µm by gaps of width $s=49$ µm.

INDUCTANCE AND RESISTANCE

We first investigated the $L$, $R$, $C$, and $G$ per unit length of the three CPWs of [2] fabricated directly on silicon substrates. These CPW conductors were formed by evaporating a thin titanium adhesion layer followed by approximately 0.5 µm of gold directly on three different silicon substrates. To assure the maximum measurement accuracy, [2] used the same metal geometries and metal thickness as the reference wafer.

Figure 2 of [2] compared $L$ and $R$ for these CPWs to that of the CPW fabricated on the semi-insulating gallium arsenide reference wafer and showed that $R$ and $L$ were insensitive to changes in the substrate. This indicates that the magnetic fields in the CPW are not affected by these moderately doped substrates: the currents are still confined to the metals.

CAPACITANCE AND CONDUCTANCE

Figure 2 shows the capacitance $C$ and conductance $G$ per unit length of the CPW measured in [2]: this figure shows that $C$ and $G$ are changed by the substrate parameters. It also compares the measurements of $C$ and
that the physics of the metal-semiconductor interface. The authors thank Nita Morgan for test-structure fabrication and David Walker for his explanations of the physics of the metal-semiconductor interface.

REFERENCES


Fig. 1. The capacitive model used in this work. Here $w$ is the center conductor width, $s$ the gap width, $w_g$ the ground-plane width, $t$ the metal thickness, $h_i$ and $\epsilon_i$ the thickness and permittivity of the lower oxide or depleted layer, and $h_p$ and $\epsilon_p$ the thickness and permittivity of the passivation layer. The expression for $F(w,s,w_g,t)$ is given in (1) of [8]. The expressions for $w'$ and $s'$ are taken from [7].
Fig. 2. The modeled and measured $C$ and $G$ for three CPWs fabricated directly on silicon. (Measurements from [2].)
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Fig. 3. The modeled and measured $C$ of CPW with and without a thick SiO$_2$ passivation layer. c:\htb386\CPWmodel\Janezic_TI\sio50_c.plt