An Experimentally Verified IGBT Model Implemented in the Saber Circuit Simulator

Allen R. Hefner, Jr., Senior Member, IEEE, and Daniel M. Diebolt, Member, IEEE

Abstract—A physics-based IGBT model is implemented into the general purpose circuit simulator Saber\textsuperscript{TM}. The IGBT model includes all of the physical effects that have been shown to be important for describing IGBT's, and the model is valid for general external circuit conditions. The Saber IGBT model is evaluated for the range of static and dynamic conditions in which the device is intended to be operated, and the simulations compare well with experimental results for all of the conditions studied.

I. NOMENCLATURE

\begin{itemize}
  \item $A$: Device active area (cm\textsuperscript{2}).
  \item $A_{ds}$: Body region area (cm\textsuperscript{2}).
  \item $A_{gd}$: Gate-drain overlap area (cm\textsuperscript{2}).
  \item $b$: \(\mu_n/\mu_p\): Ambipolar mobility ratio.
  \item $BV_{CEO}$: Open-base, collector-emitter breakdown voltage (V).
  \item $C_{bc}$: Base-collector depletion capacitance (F).
  \item $C_{ce}$: Collector-emitter redistribution capacitance (F).
  \item $C_{ds}$: Drain-source depletion capacitance (F).
  \item $C_{eb}$: Implicit emitter-base capacitance (F).
  \item $C_{eb}$: Emitter-base depletion capacitance (F).
  \item $C_{eb}$: Emitter-base diffusion capacitance (F).
  \item $C_{f}$: External feedback capacitance (F).
  \item $C_{gd}$: Gate-drain capacitance (F).
  \item $C_{gd}$: Gate-drain overlap capacitance (F).
  \item $C_{ge}$: Gate-source capacitance (F).
  \item $C_{ov}$: Gate-source overlap capacitance (F).
  \item $C_{s}$: Snubber capacitance (F).
  \item $D_{n}, D_{p}$: Electron, hole diffusivity (cm\textsuperscript{2}/s).
  \item $D$: \(2D_{n}D_{p}/(D_{n} + D_{p})\): Ambipolar diffusivity (cm\textsuperscript{2}/s).
  \item $D_{c}$: Carrier-carrier scattering diffusivity (cm\textsuperscript{2}/s).
  \item $I_{f}$: Feedback current (A).
  \item $I_{q}$: Gate current (A).
  \item $I_{gen}$: Collector-base thermally generated current (A).
  \item $I_{L}$: Load inductor current (A).
  \item $I_{mult}$: Avalanche multiplication current (A).
  \item $I_{mos}$: MOSFET channel current (A).
  \item $I_{nec}$: Emitter electron saturation current (A).
  \item $I_{T}$: Anode current (A).
  \item $K_{Pin}$: Linear region MOSFET transconductance parameter (A/V\textsuperscript{2}).
  \item $K_{Prot}$: Saturation region MOSFET transconductance parameter (A/V\textsuperscript{2}).
  \item $L$: Ambipolar diffusion length (cm).
  \item $L_{L}$: Series load inductance (H).
  \item $M$: Avalanche multiplication factor.
  \item $N_{B}$: Base doping concentration (cm\textsuperscript{-3}).
  \item $n_{eff}$: Effective base doping concentration (cm\textsuperscript{-3}).
  \item $n_{i}$: Intrinsic carrier concentration (cm\textsuperscript{-3}).
  \item $N_{sat}$: Velocity saturation component of $N_{sat}$ (cm\textsuperscript{-3}).
  \item $N_{sat}$: Collector-base space charge concentration (cm\textsuperscript{-3}).
  \item $P_{0}$: Carrier concentration at emitter end of base (cm\textsuperscript{-3}).
  \item $\overline{v}$: Average carrier concentration in base (cm\textsuperscript{-3}).
  \item $q$: Electronic charge (1.6 \times 10^{-19} C).
  \item $Q$: Instantaneous excess carrier base charge (C).
  \item $Q_{B}$: Background mobile carrier base charge (C).
  \item $Q_{B}$: Emitter-base junction built-in charge (C).
  \item $Q_{s}$: Drain-source capacitor charge (C).
  \item $Q_{gs}$: Gate-source capacitor charge (C).
  \item $R_{b}$: Conductivity-modulated base resistance (\Omega).
  \item $R_{f}$: Series feedback resistance (\Omega).
  \item $R_{g}$: Gate drive resistance (\Omega).
  \item $R_{g}$: Turn-on gate resistance (\Omega).
  \item $R_{s}$: Series load resistance (\Omega).
  \item $R_{s}$: Snubber bleeder resistor (\Omega).
  \item $R_{ae}$: Device anode voltage (V).
  \item $R_{ae}$: Anode supply voltage (V).
  \item $V_{ae}$: Conductivity-modulated base resistance voltage (V).
  \item $V_{cc}$: Base-collector voltage (V).
  \item $V_{ce}$: Collector-emitter voltage (V).
  \item $V_{cf}$: External feedback capacitor voltage (V).
  \item $V_{dd}$: Drain-gate voltage (V).
  \item $V_{ds}$: Drain-source voltage (V).
  \item $V_{eb}$: Emitter-base capacitor voltage (V).
  \item $V_{eb}$: Emitter-base diffusion, depletion voltage (V).
  \item $V_{ee}$: Emitter-collector voltage (V).
\end{itemize}
As purposes and have significantly different structures than the microelectronic devices. The depletion region for high blocking voltages while still main-

parts because they have been designed for different functional device types influence the behavior of IGBT's. However, the physical phenomena of both bipolar and MOSFET power semiconductor devices.

The n-channel IGBT behaves as a p-n-p bipolar transistor and the regions of the device structure corresponding to the thick, lightly doped drain region (epitaxial layer) to support the high output current capability of power bipolar transistors but with the efficient gate drive requirements of power MOSFET's.

IGBT's have become widely accepted among circuit designers as an alternative to power bipolar transistors and Darlington transistors in a variety of power converter and motor drive applications. To design power electronic circuits containing IGBT's, circuit simulations are needed to examine the behavior of the devices within the circuit. However, the device models currently available in most commercial circuits simulators were originally intended to describe microelectronic devices and cannot readily be modified to describe IGBT's or other power semiconductor devices.

The basic equivalent circuit of the IGBT is shown in Fig. 2, and the regions of the device structure corresponding to the elements of this circuit are indicated on the right half of Fig. 1. The n-channel IGBT behaves as a p-n-p bipolar transistor that is supplied base current by an n-channel MOSFET, and thus the physical phenomena of both bipolar and MOSFET device types influence the behavior of IGBT's. However, the internal MOSFET and the internal bipolar transistor of the IGBT behave differently than their microelectronic counterparts because they have been designed for different functional purposes and have significantly different structures than the microelectronic devices [1]-[3].

For example, the internal VDMOSFET of the IGBT has a thick, lightly doped drain region (epitaxial layer) to support the depletion region for high blocking voltages while still maintaining a short channel length to supply high current densities. As a consequence, the gate-drain overlap capacitance of the IGBT is to inject a high level of excess minority carriers into the epitaxial layer which thereby reduces the on-state resistance of this layer (conductivity modulation). Thus, IGBT's have the high output current capability of power bipolar transistors with the efficient gate drive.

II. INTRODUCTION

THE IGBT (Insulated Gate Bipolar Transistor) is a new power device that is designed to overcome the high on-state loss of the power MOSFET. The structure of the IGBT shown in Fig. 1 is similar to that of an n-channel VDMOSFET (Vertical double Diffused MOSFET), with the exception that the n-type drain contact of the conventional VDMOSFET is replaced by the p-type anode region for the IGBT. The purpose of the additional anode-epitaxial layer p-n junction of the IGBT is to inject a high level of excess minority carriers into the epitaxial layer which thereby reduces the on-state resistance of this layer (conductivity modulation). Thus, IGBT's have the high output current capability of power bipolar transistors but with the efficient gate drive requirements of power MOSFET's.

VDMOSFET is highly nonlinear. The gate-drain capacitance is equal to the gate-drain overlap oxide capacitance for low drain voltages where the silicon beneath the gate-drain overlap is not depleted. However, at high drain voltages, the gate-drain overlap has a depletion layer in the silicon beneath the gate oxide, and the gate-drain capacitance is reduced by about two orders of magnitude [3].

The bipolar transistor of the IGBT is introduced for the purpose of modulating the conductivity of the epitaxial layer. This transistor has a lightly doped wide base (epitaxial layer) to support high voltages, and its base contact is at the collector edge of the neutral base where the MOSFET channel current supplies electrons to the base. This bipolar transistor is also typically designed with a low excess carrier lifetime in the base to achieve a high speed turn-off. As a consequence, the bipolar transistor of the IGBT has a low current gain and is operated in the high-level injection condition for the practical current density range of the IGBT. This is in contrast to microelectronic bipolar transistors which are designed to have a narrow base, a high base lifetime, and which are typically operated in low-level injection to achieve a high current gain.

To describe the high-level injection operation of the wide base bipolar transistor of the IGBT and other conductivity-modulated power devices, ambipolar transport theory must be used to describe the transport of electrons and holes in the base, and the transient behavior cannot be described using the conventional quasi-static approach [1]. A physics-based model for the low-gain, high-level injection bipolar transistor of the IGBT is developed in [2] and is combined with a VDMOSFET model in [3], resulting in a general purpose model for the IGBT. The model has been verified for various external circuit conditions [1]-[4] and for the full range of static and dynamic conditions in which the IGBT's are intended to be operated. The model has also been used to design power electronic circuits.

IEEE 533
shown to be suitable for simulating the behavior of IGBT's for general external circuit conditions [5], [6].

The purpose of this paper is to describe the methodology for implementing the IGBT mathematical model developed by Hefner into the Saber circuit simulator [7], and to provide a Saber IGBT model that can be used for general purpose circuit simulations. Furthermore, the techniques demonstrated for modeling IGBT's with the Saber circuit simulator are generally applicable to modeling other power semiconductor devices. Many diverse types of power devices are currently available with structures that differ significantly from one another, and different device model equations are generally required to describe each device type. This is in contrast to microelectronic devices for which many different devices can be described by using the appropriate model parameters in a few standard device models. Thus, the techniques described in this paper for implementing model equations into the Saber circuit simulator are essential for accurate simulation of power semiconductor devices.

### III. IGBT Dynamic Model

Fig. 3 shows a detailed IGBT equivalent circuit superimposed on a schematic of the structure of one of the many thousand cells of an n-channel IGBT. The elements of the circuit of Fig. 3 represent the nonlinear physical phenomena associated with each region of the device structure. The basic IGBT equivalent circuit of a bipolar transistor that is supplied base current by a MOSFET is indicated by the MOSFET and bipolar transistor symbols within the circuit of Fig. 3. The other components connected between the emitter (e), base (b), and collector (c) nodes are associated with the bipolar transistor, and those connected between the gate (g), source (s), and drain (d) nodes are associated with the VDMOSFET.

Table I gives a list of the expressions used in the Saber IGBT model to describe the phenomena associated with each of the components in Fig. 3. The IGBT model equations in Table I are equivalent to those presented in [3] with the
exception that they have been augmented to show how the following effects are included [6]: 1) mobility reduction due to carrier-carrier scattering, 2) mobile carrier space charge concentration in the base-collector depletion region due to velocity saturation, and 3) avalanche multiplication within the base-collector depletion region. The equations have also been reformulated to emphasize the Saber implementation, which is described in Section III. In this section, the circuit elements of Fig. 3 are used to describe the physical origin of the expressions in Table I and to explain the influence of each physical phenomenon on the device behavior.

**MOSFET Characteristics**

The MOSFET portion of the IGBT's studied in this work behaves similarly to the power VDMOSFET, with the exception that the resistance of the lightly doped epitaxial layer is accounted for as the conductivity-modulated base resistance of the bipolar transistor, \( R_{B} \) [3]. In addition, the drain-source and gate-drain depletion capacitances coincide with the base-collector depletion capacitance of the bipolar transistor and hence are only included in the MOSFET model. In order to describe IGBT's made with MOSFET structures other than the VDMOSFET, only the components of Fig. 3 associated with the MOSFET portion of the device need to be changed.

The expression for the current through the MOSFET channel \( I_{MOS} \) given in Table I includes the effects of diffusion of carriers in the MOSFET channel due to the nonuniform channel dopant density. This results in the different value for the saturation region and linear region transconductance parameters \( K_{Psat} \) and \( K_{Plin} \), respectively. The reduction in channel mobility due to the high transverse electric field for high gate voltages is included through the parameter \( \theta \) and results in a linear increase in saturation current with \( V_{gs} - V_{T} \) for high gate voltages, whereas the saturation current increases as the square of \( V_{gs} - V_{T} \) for low gate voltages. The channel length modulation factor of traditional micro-electronic MOSFET models is not necessary for the VDMOSFET due to the high channel dopant density.

The VDMOSFET gate-source capacitance \( C_{gs} \) consists of the sum of the gate oxide capacitance of the source overlap \( C_{oxs} \) and the source metallization capacitance \( C_{m} \). The VDMOSFET gate-drain feedback capacitance (or Miller capacitance) \( C_{pd} \) is equal to the gate oxide capacitance of the gate-drain overlap for \( V_{ds} \leq V_{gs} - V_{Td} \), but for \( V_{ds} > V_{gs} - V_{Td} \) the silicon beneath the gate-drain overlap becomes depleted, and the gate-drain capacitance consists of the series combination of the gate-drain overlap oxide capacitance \( C_{oxd} \) and the gate-drain overlap depletion capacitance \( C_{dph} \). The VDMOSFET drain-source capacitance \( C_{dsj} \) consists of the depletion capacitance of the drain-body junction.

The gate-drain overlap depletion capacitance \( C_{dph} \) and the drain-source depletion capacitance \( C_{dsj} \) are voltage dependent due to the voltage dependencies of the depletion widths. The drain-source depletion width \( W_{dsj} \) is proportional to the square root of the drain-source voltage plus the built-in potential of the junction (\( \sim 0.6 \) V). The gate-drain depletion width \( W_{dph} \) is proportional to the square root of the gate-drain voltage where the threshold voltage for the depletion of the epitaxial layer \( V_{Td} \) is approximately equal to zero due to the low doping concentration of the epitaxial layer except in devices with a neck region implant (region between adjacent body diffusions). The gate-drain capacitance is also proportional to the area of the gate-drain overlap \( A_{gd} \), and the drain-source capacitance is proportional to the area of the body region \( A_{ds} \) (Fig. 3), where the sum of \( A_{gd} \) and \( A_{ds} \) is the active area of the chip \( A \).

**Bipolar Transistor Characteristics**

The transient behavior of the lightly doped wide base bipolar transistor of the IGBT (and other conductivity-modulated devices) was analyzed in [2]. In that analysis, the ambipolar transport equations were solved for the boundary conditions of the bipolar transistor to obtain the transient carrier distribution, the collector and base currents, and the emitter-base voltage. Fig. 4 shows the coordinate system used to develop the IGBT bipolar transistor model. Because the base-collector voltage changes with time during transient conditions, the
The bipolar transistor symbol in Fig. 3 corresponds to the 
IGBT model but are not described on the phenomenological 
circuit of Fig. 3 are: 1) mobility reduction due to high free-
carrier levels, 2) velocity saturation in the base-collector 
depletion region, and 3) carrier multiplication within the 
base-collector depletion region [3]-[6]. These effects do not 
change the qualitative behavior of IGBT's operated within 
their maximum current and voltage ratings, but do have a 
second-order effect on the quantitative results of the model. 
However, the carrier multiplication effect results in avalanche 
breakdown for operating conditions in which the maximum 
rated voltage is exceeded. The mobility reduction and velocity 
saturation effects are a result of the bias dependence of the 
physical parameters which are used to derive the model. 
These two effects are included implicitly because an explicit 
analytical solution is not readily obtained if these effects are 
included in the derivation of the basic model. 
The space charge concentration due to mobile carriers 
 flowing through the base-collector depletion region at the 
saturation limited velocity has a second-order effect on the 
time rate-of-change of the base-collector voltage [2]. The 
component of base-collector space charge due to velocity 
saturation is given in terms of $\mu_{c}$ and $I_{ons}$ by 

$$N_{sat} = I_c / (qA_{umax}) - I_{ons} / (qA_{umsat}).$$

Because the expressions for the currents $I_c$ and $I_{ons}$ in Table I 
depend upon the space charge concentration, the variable $N_{sat}$ 
is solved for iteratively to satisfy (1).

The mobility reduction due to carrier-carrier scattering has a 
second-order effect on the on-state emitter-base voltage at high 
free-carrier levels [2]. The reciprocal component of mobility 
due to carrier-carrier scattering is given in terms of the excess 
carrier concentration by 

$$1/\mu_{c} = \left[ \delta \rho \ln(1 + \alpha_{2} (\delta \rho)^{-2/3}) \right] / \alpha_{1}. $$

Because the expression for the average excess carrier concen-
tration $\delta \rho$ given in Table I depends upon the mobility, 
the variable $1/\mu_{c}$ is solved for iteratively to satisfy (2). This 
technique can also be used to include the influence of other 

Base-collector depletion width $W_{bcj}$ changes with time, and 
the excess carrier charge stored in the base is swept into 
a neutral base width $W$ that changes with time. The quasi-
static condition cannot be assumed for the transient analysis 
because the base width typically changes faster than the base 
transit speed for excess carriers, and because the transports of 
electrons and holes are coupled for ambipolar transport [1]. 

In addition to the above-mentioned depletion capacitances, 
the bipolar transistor of the IGBT contributes a collector-
emitter redistribution capacitance $C_{rer}$ which is a result of 
the nonquasi-static behavior of the bipolar transistor base 
charge for the moving base-collector boundary condition. The 
expression for the collector-emitter redistribution capacitance 
in Table I is equal to the ratio $Q/Q_B$ times one-third the 
based-collector depletion capacitance $C_{bcj}$. In the IGBT model, 
the base-collector depletion capacitance is defined to relate 
the time rate-of-change of the base-collector depletion width 
and the time rate-of-change of base-collector voltage, but is 
not used to describe the base-collector depletion capacitance 
displacement current which is accounted for in the gate-drain 
and drain-source capacitances of the VDMOSFET. 

Because the excess carrier base charge $Q$ is much larger than 
the background base charge $Q_B$ for the high-level injection 
condition, the redistribution capacitance is much larger than 
the depletion capacitances and thus dominates the output 
capacitance of the IGBT at turn-off [1]-[4]. Because the 
redistribution capacitance is a result of a component of collector 
current, this capacitance appears as an anode-to-cathode 
capacitance, and the gate-to-drain feedback capacitance is 
unchanged from that of the VDMOSFET [3]. The effective 
output capacitance at turn-off for the IGBT depends upon the 
device base lifetime, because the steady-state value of $Q$ at 
the initiation of turn-off depends upon the device base lifetime. 
The effective output capacitance at turn-on is much less than 
that at turn-off for the IGBT, because $Q$ is zero in the off-state 
before the initiation of the turn-on.

The bipolar transistor symbol in Fig. 3 corresponds to the 
expression for the component of collector current $I_{ces}$ and 
the component of base current $I_{bas}$. The expression for $I_{ces}$ 
in Table I consists of the nonquasi-static component due to 
the coupling between the transports of electrons and holes 
in the base [1] (first term on the right-hand side), and the 
well-known charge-control component due to the diffusion 
of holes through the base for the high-level injection conditions 
(second term). The expression for $I_{bas}$ consists of a component 
due to recombination in the base (first term) and a component 
due to injection of electrons into the emitter (second term). 
The base current is a significant component of the total anode 
current for the low-gain condition of the bipolar transistor of 
the IGBT, and is also important in determining the time rate-
of-change of base charge for transient conditions, i.e., current 
in the emitter-base capacitor.

The emitter-base voltage consists of the potential across the 
conductivity-modulated base resistance $R_b$, plus the potential 
across the emitter-base diffusion capacitance $C_{ebd}$ or the 
depletion capacitance $C_{edj}$ [3]. For forward conduction, the 
emitter-base voltage is determined by the diffusion capacitance 
and the conductivity-modulated base resistance. The emitter-
base diffusion capacitance is represented implicitly in Table I, 
because the expression for the emitter-base capacitor voltage 
$V_{ebd}$ in terms of the base charge $Q$ cannot be inverted to 
obtain an expression for the charge in terms of voltage. The 
emitter-base junction depletion capacitance $C_{edj}$ is important 
when the emitter-base junction is reverse biased or has a 
small forward bias, but for larger forward biases the emitter-
base diffusion capacitance $C_{ebd}$ is dominant. The charge $Q$ 
is also used to describe the space charge of the emitter-base 
deployment capacitance for the bias range where this capacitance 
is dominant, and a continuous transition between the depletion 
and diffusion capacitances is obtained by using the larger of 
the two capacitances or equivalently the minimum voltage. 
For reverse blocking $Q < 0$, the collector and base currents 
are also replaced by the emitter-base leakage current and the 
reverse collector current.

**Second-Order Effects**

The second-order effects that are incorporated into 
the IGBT model but are not described on the phenomenological 
circuit of Fig. 3 are: 1) mobility reduction due to high free-
carrier levels, 2) velocity saturation in the base-collector 
depletion region, and 3) carrier multiplication within the 
base-collector depletion region [3]-[6]. These effects do not 
change the qualitative behavior of IGBT's operated within 
their maximum current and voltage ratings, but do have a 
second-order effect on the quantitative results of the model. 
However, the carrier multiplication effect results in avalanche 
breakdown for operating conditions in which the maximum 
rated voltage is exceeded. The mobility reduction and velocity 
saturation effects are a result of the bias dependence of the 
physical parameters which are used to derive the model. 
These two effects are included implicitly because an explicit 
analytical solution is not readily obtained if these effects are 
included in the derivation of the basic model.

The space charge concentration due to mobile carriers 
flowing through the base-collector depletion region at the 
saturation limited velocity has a second-order effect on the 
time rate-of-change of the base-collector voltage [2]. The 
component of base-collector space charge due to velocity 
saturation is given in terms of $I_c$ and $I_{ons}$ by 

$$N_{sat} = I_c / (qA_{umax}) - I_{ons} / (qA_{umsat}).$$

Because the expressions for the currents $I_c$ and $I_{ons}$ in Table I 
depend upon the space charge concentration, the variable $N_{sat}$ 
is solved for iteratively to satisfy (1).

The mobility reduction due to carrier-carrier scattering has a 
second-order effect on the on-state emitter-base voltage at high 
free-carrier levels [2]. The reciprocal component of mobility 
due to carrier-carrier scattering is given in terms of the excess 
carrier concentration by 

$$1/\mu_{c} = \left[ \delta \rho \ln(1 + \alpha_{2} (\delta \rho)^{-2/3}) \right] / \alpha_{1}. $$

Because the expression for the average excess carrier concen-
tration $\delta \rho$ given in Table I depends upon the mobility, 
the variable $1/\mu_{c}$ is solved for iteratively to satisfy (2). This 
technique can also be used to include the influence of other
bias-dependent model parameters which cannot readily be included in the derivation of the analytical model, i.e., lifetime reduction due to Auger recombination [8].

Carrier multiplication due to impact ionization in the high electric field of the base-collector depletion region has a second-order effect on the anode current for large anode voltages that are within the device maximum voltage rating. Carrier multiplication also determines the avalanche breakdown behavior for operating conditions in which the device maximum voltage rating is exceeded. Carrier multiplication in the base-collector depletion region results in an additional component of base-to-collector current that increases exponentially with anode voltage near the open-base, collector-emitter breakdown voltage. The carrier multiplication current is included in the derivation of the IGBT model equations by including the additional components of base-to-collector current $I_{\text{mull}}$ that is proportional to the electron and hole currents entering the depletion region, $I_e$ and $I_{\text{mos}}$, and that is proportional to the multiplication factor $(M - 1)$ [3]. The thermally generated leakage current $I_{\text{gen}}$ is also included, but this component of current is only important when using the model at high temperature or to describe the structurally equivalent power MOSFET.

IV. IMPLEMENTING THE IGBT MODEL INTO SABER

To describe the behavior of a system such as an electrical network using the Saber circuit simulator, the interconnections of the different components of the system are described using a network listing (net-list). The net-list contains a statement for each component of the system that defines the name of the model template used to describe the component, the terminal connection points of the component, and the values of the model parameters that are to be changed from the default values of the generic model template (see Section IV). The models that describe each of the components of the system can be accessed from the Saber libraries of standard component models, or from user-defined Saber templates where the equations that describe the physical behavior of the device are implemented. The implementation of the IGBT model equations into a Saber template is described in this section, and the net-lists describing the operation of the IGBT within various test circuits are given in the next section.

Saber Templates

Saber templates are written in the MAST® modeling language which is similar to the C programming language with the addition of specially designed modeling constructs which facilitate the implementation of Kirchhoff’s laws and aid convergence. Both user-defined models and the standard Saber library models are implemented in Saber templates using the MAST modeling language. Electrical component models are implemented into templates by expressing the current through each element of the component in terms of the system variables of the component; system variables for electrical component models consist of terminal node voltages, internal node voltages, and explicitly defined system variables. The simulator solves for the system variables of the entire network such that the net current into each node of the system sums to zero (i.e., Kirchhoff’s current law is satisfied), and such that the equations defining the explicitly defined system variables for each component are satisfied.

A skeleton template of the Saber IGBT model is shown in Fig. 5 [7] where each section performs the following functions: In this example, the IGBT template header defines the anode, gate, and cathode terminal connection points as well as the names and default values for model parameters such as the high level lifetime $\tau_{\text{HL}}$. The local declarations define constants, designate internal nodes, and explicitly define the additional system variables (in addition to the node voltages) needed to describe the state of the device. The parameters section is used to calculate quantities that only need to be calculated once at the beginning of the simulation. Quantities that are functions of the system variables (i.e., Table I) are implemented in the values section. The control section contains information about the nonlinear model relationships and commands to aid convergence. Finally, the equations section describes how the quantities calculated in the values section are assembled to solve for the system variables.

**IGBT Model Formulation**

To implement the IGBT model presented in Section II into the Saber circuit simulator, the model is formulated such that the currents between each of the terminal nodes are expressed in terms of the nonlinear functions of the system variables (Table I) and in terms of the time rate-of-change of these functions of the system variables. Fig. 6 is a schematic of the components of current flow between the terminal nodes of the IGBT (gate, anode, and cathode), indicating the internal nodes (drain and emitter) that are required to implement the IGBT model equations given in Table I into the Saber circuit simulator. Fig. 6 is an analog circuit representation 2The "sans serif" symbols throughout the text represent computer mnemonics.
for the equations in Table I. The expressions in Table I are implemented in the values section of the Saber template, and these values are used in the equations section of the template to describe the interconnection of the components of current through each element of Fig. 6.

The analog circuit representation of the IGBT model equations of Fig. 6 differs from the phenomenological circuit of Fig. 3 with the bipolar transistor symbol replaced by the base and collector current sources. In the phenomenological circuit which is based upon the IGBT structure without considering the effects of ambipolar transport, the emitter-base diffusion capacitance is represented as a lumped capacitor located at the metallurgical emitter-base junction, and only the flow of base current through the conductivity modulated base resistance is indicated. However, the potential drops due to drift and diffusion are actually distributed throughout the base region, and the drift terms of the ambipolar transport equations depend upon both the base and collector currents [2]. Thus, both the base and collector components of current contribute to the resistive potential drop $V_{ce}$, and $R_{b}$ appears at the emitter terminal in the analog circuit representation of the IGBT model equations (Fig. 6).

The emitter-base capacitor current $I_{ceb}$ represents the time rate-of-change of the base charge, where the nonlinear expression given in Table I for the emitter-base voltage in terms of the base charge describes implicitly the capacitance of the emitter-base junction. The collector-emitter redistribution capacitance represents the component of collector current that depends upon the time rate-of-change of the base-collector voltage $I_{ccf}$ (represented as the emitter-collector voltage for easier conceptualization). $I_{ccf}$ represents the component of collector current that does not depend upon the time rate-of-change of the base-collector voltage. $I_{bbs}$ represents the component of base current that does not depend upon the time rate-of-change of the base charge and does not flow through the emitter-base capacitor. The avalanche multiplication current $I_{mult}$ flows from the base to the collector and provides an additional component of base current to the bipolar transistor.

**Saber Implementation**

The expressions in Table I are implemented in the values section of the Saber IGBT model template and are functions of the IGBT system variables, the IGBT model parameters (Table II), and the physical constants of silicon (Table III). The system variables for the node voltages and the explicitly defined system variables: $Q$, $N_{sat}$, $I_{mult}$, $dV_{ce}$/dt, and $dV_{gd}$/dt. The first six equations in Table I evaluate the voltage differences used by other expressions in Table I, where the notation $V(a)$ is the MAST syntax for the voltage at node $a$. The quantities evaluated in the values section (Table I) are used in the equations section shown in Fig. 7 to describe the currents through each of the elements of Fig. 6, and to describe the expressions that define the explicitly defined system variables: $Q$, $N_{sat}$, $I_{mult}$, $dV_{ce}$/dt, and $dV_{gd}$/dt.

The first six statements in the equations section of Fig. 7 describe the currents between the node pairs of Fig. 6 in terms of the system variables using the values in Table I. The notation $i(a \rightarrow b)$ indicates that a component of current, given by the expression on the right-hand side of $+_m$, flows from node $a$ to node $b$. The currents through the gate-source and drain-source capacitances, $I_{gs}$ and $I_{ds}$, are formulated as the time derivative of the capacitor chargers $Q_{gs}$ and $Q_{ds}$, where $d_{by_d}t$ is the Saber time derivative operator, whereas the
equations 
\[
\begin{align*}
\text{t 있게게 } \text{> 캐테드로} & = t_{\text{by dt}(Q_{\text{ds}})} \\
\text{t 생원 } \text{> 태계로} & = C_{\text{gd}} + v_{\text{gd}} \\
\text{t 생원 } \text{> 캐테드로} & = N_{\text{sat}} + l_{\text{mos}} + l_{\text{mult}} + v_{\text{by dt}(Q_{\text{ds}})} \\
\text{t 생원 } \text{> 캐테드로} & = l_{\text{in}} + C_{\text{er}} + v_{\text{ed}} + v_{\text{by dt}(Q)} \\
\text{t 에미터 } \text{> 생원으로 } & = v_{\text{ae}} / R_{\text{b}} \\
\text{dVgd } & = d_{\text{by dt}}(v_{\text{gd}}) \\
\text{dvect } & = d_{\text{by dt}}(v_{\text{ect}}) \\
Q & : V_{\text{eq}} - V_{\text{b}} \\
\text{Nsat } & : N_{\text{sat}} = \frac{l_{\text{c}} / (q * A * v_{\text{psat}}) - l_{\text{mos}} / (q * A * v_{\text{psat}})}{2} \\
\mu_{\text{cin}} & : \mu_{\text{cin}} = P_{\text{m}} * \log(1 + \alpha_{2} / P_{\text{m}} * (2 / 3)) \\& / \alpha_{1}
\end{align*}
\]

Fig. 7. Equations section of Saber IGBT model template.

The range and density of the sample points can be tailored to the nature of the model nonlinearities by specifying the sample points arrays in the control section of the Saber template. The Saber simulator also provides the capability to control the maximum step size that a given variable can take between successive iterations (Newton steps) in regions where the nonlinear model functions have discontinuous partial derivatives with respect to the system variables. This feature of the Saber simulator is beneficial in implementing models which use different expressions to describe different regions of operation; for example, $I_{\text{mos}}$ is described by a different expression for gate voltages above and below $V_{\text{gs}} = V_{T}$. Newton steps for the independent variables can be introduced near the transition between different regions by specifying the Newton step arrays in the control section. The Newton steps tend to confine the iterations of the independent variables to the regions where they are introduced so that the variables do not overshoot the transition regions during iterations.

In implementing the IGBT model into the Saber simulator, the equations in Table I must be formulated such that they are continuous and nonsingular in the range that the system variables may take during iterations. For example, $C_{\text{gd}}$ becomes infinite at $V_{\text{gd}} = -V_{T}$ which would result in numerical overflows even though the reciprocal sum that describes $C_{\text{gd}}$ is well defined mathematically. This problem is alleviated by reformulating the gate-drain capacitance expression in terms of reciprocal capacitances so that only $1/C_{\text{gd}}$ needs to be evaluated. Some of the expressions in Table I are only valid for limited ranges of the system variables and should be left undefined or be given a definite value in the inapplicable range. For example, the expression for $W_{\text{pdl}}$ is only applicable when a depletion region exists (i.e., $V_{\text{gd}} > -V_{T}$), and the expressions would result in the square root of a negative number otherwise.

Other expressions are nonsingular and continuous in the range of all physical solutions to the nonlinear equations, but are not so in ranges which may be entered into during the iterations necessary to find the physical solution. For example, the expression for $W_{\text{ds}}$ is not valid for $V_{\text{ds}} < -0.6$ V, and although no physical solutions exist in this range, it is necessary to provide a value in this range, because the drain-source voltage can enter the $V_{\text{ds}} < -0.6$ V range during the iterations necessary to find the physical solution.
defined in Fig. 8(a). The parameters of each component that component, where the names of these connection points are given on the right-hand side of the period. The resistor, elements of Fig. 8(a). The first column in these statements is given on the left-hand side of the equal sign define the connection points for each given template that is used to model the component is designated each component of the circuit, where the name of the given Saber template library, and the user-defined IGBT template is described in Section 111. The evaluations are demonstrated in this paper for a 7.1-A, 600-V rated IGBT’s with the same base lifetime, although the model has also been evaluated for faster devices with lower base lifetimes. Fig. 8 shows the basic test circuit (a) and the corresponding net-list (b) used for the evaluations. Modifications to this net-list are also discussed below to describe the polarized active feedback snubber circuit results of [3] and to describe the passive polarized turn-off snubber and soft clamp circuit results of [4].

The statements in Fig. 8(b) describe each of the six circuit elements of Fig. 8(a). The first column in these statements designates each component of the circuit, where the name of the given template that is used to model the component is given on the left-hand side of the period (.), and the name of the specific instance of the component within the circuit is given on the right-hand side of the period. The resistor, inductor, and voltage supply templates are provided within the Saber template library, and the user-defined IGBT template is described in Section III. The remaining columns to the left of the equal sign define the connection points for each component, where the names of these connection points are defined in Fig. 8(a). The parameters of each component that are to be changed from the default values of the generic templates are given to the right of the equal signs.

Fig. 9 compares the low anode voltage static characteristics of the Saber IGBT model (dashed lines) with the characteristics measured on a curve tracer (solid lines). The simulated characteristics are obtained using a Saber command file that varies the gate voltage in 1-V steps and performs a dc sweep analysis for the anode voltage at each gate voltage step. The following features of the low-voltage static characteristics are indicated on Fig. 9: 1) the diode voltage offset due to the anode-epitaxial layer p-n junction, 2) the on-state region which has a low resistance due to conductivity modulation, 3) the current saturation region which is due to saturation of the MOSFET channel current, and 4) the triode like region which is referred to as the linear region for MOSFET’s. The agreement between the simulated and measured static characteristics for 1) the diode voltage offset validates the implementation of $V_{	ext{deg}}$, 2) the on-state characteristics validate the implementation of $R_o$, and 3) the saturation characteristics validate the implementation of $I_{	ext{mos}}$, $I_{	ext{bas}}$, and $I_{	ext{css}}$.

The triode-like region indicated as 4) in Fig. 9 has a larger transconductance parameter ($K_{	ext{phia}}$) than does the saturation region ($K_{	ext{sat}}$), due to diffusion in the nonuniformly doped MOSFET channel. This results in a steeper slope for the linear region than would occur if the transconductance parameters were identical. This behavior is typical of the channel current for the VDMOSFET structure [9], although the triode region is not as evident for power MOSFET’s as it is for IGBTs due to the large series drain resistance of high-voltage MOSFET’s. The expression for $I_{	ext{mos}}$ in Table I accounts for the difference in transconductances and has a continuous first derivative with respect to $V_a$, at the transition between the linear and saturation regions. Reference [6] describes the method used to extract the two transconductance parameters. For low gate voltages, the saturation current indicated as 3) in Fig. 9 increases proportional to $(V_{	ext{gs}} - V_T)^2$. However, at high gate voltages, the channel mobility is reduced due to the high transverse electric field which is accounted for by the factor $1+\theta(V_{	ext{gs}} - V_T)$ in the expression of Table I.

The slope of the current saturation region (output conductance) is small for VDMOSFET’s, because the channel length modulation effect is minimal for the lightly doped drain [9]. However, IGBT’s do exhibit a significant output

<table>
<thead>
<tr>
<th>V, Va</th>
<th>Va</th>
<th>300</th>
</tr>
</thead>
<tbody>
<tr>
<td>L Lg</td>
<td>Va</td>
<td>80u</td>
</tr>
<tr>
<td>R Lg</td>
<td>Va</td>
<td>30</td>
</tr>
<tr>
<td>R Lg</td>
<td>Vgs</td>
<td>0.1k</td>
</tr>
<tr>
<td>Pulsgen 1</td>
<td>Vgg</td>
<td>0</td>
</tr>
<tr>
<td>IGBT 1</td>
<td>Va</td>
<td>Vgs</td>
</tr>
</tbody>
</table>

Fig. 8. Series resistor-inductor load, resistive gate drive (a) test circuit and (b) corresponding net-list.

![Fig. 9](image-url)
conductance for anode voltages larger than those in Fig. 9, due to the increase in the bipolar transistor current gain with decreasing neutral base width $W$ (Early effect), and due to the increase in avalanche multiplication. In addition, the IGBT anode current increases exponentially with anode voltage near the open-base, collector-emitter breakdown voltage of the internal bipolar transistor (600 V). Both of these features of the high-voltage static characteristics of the IGBT (not shown in Fig. 9) are also well described by the Saber IGBT model.

Fig. 10 compares the Saber IGBT model (dashed lines) with the measured (solid lines) anode voltage, anode current, gate voltage, and gate current waveforms for different values of gate resistance. These characteristics are obtained using a Saber command file that varies the gate resistance in values of 0.1 k, 1 k, 2 k, and 3 kΩ, and performs a transient simulation for each gate resistance. The agreement between the simulations and measurements as indicated on Fig. 10 for 1) the slowly decaying portion of the turn-off current waveform validates the implementation of $C_{ebd}$ and $I_{bss}$, 2) the value of the voltage overshoot at turn-off for the stiff gate drive ($R_g = 0.1$ kΩ) validates the implementation of $C_{ov}$ which dominates the effective output capacitance, 3) the turn-off delay time for the different values of gate resistance validates the implementation of the low-voltage gate-drain capacitance, and 4) the anode voltage overshoot for different gate resistances validates the high-voltage gate-drain capacitance. The agreement between the simulated and measured gate voltage waveforms also validates the implementation of the VDMOSFET capacitances.

Fig. 11 compares the simulated and measured anode voltage turn-off waveforms for an IGBT being switched off both with and without the protection circuits shown in Fig. 12. The anode voltage turn-off waveform of the $R_g = 0.1$ kΩ curve in Fig. 10 is repeated on Fig. 11 for reference. The soft clamp circuit shown in Fig. 12(a) is connected to the anode terminal of Fig. 8(a). For a polarized turn-off snubber, $R_g$ is connected to $V_a$ instead of $V_{cs}$. The simulations including the soft clamp are performed by adding the following statements to the net-list of Fig. 8(b): where $mr1366$ is the part number of the 500-V, 6-A power diode used in this circuit which is included in the Saber component library. For the large load inductance used in this circuit (200 µH), the anode voltage would overshoot the IGBT maximum rated voltage (600 V) if the protection circuit were not added, but with the protection circuit, the IGBT can be switched off without excessive voltage overshoot. The Saber IGBT model also predicts the IGBT anode current and the diode current waveforms for this circuit [4], and is thus useful in the design and selection of components for the protection circuit.

The polarized active snubber circuit shown in Fig. 12(b) is connected to the IGBT anode and the IGBT gate in the circuit of Fig. 8(a). The simulations including the polarized active snubber are performed by adding the following statements to the net-list of Fig. 8(b): where $d1n4148$ is the part number of the 50-V, 100-mA small-signal diode used in this circuit which is included in the Saber component library. Notice that the voltage overshoot is reduced without the need for the large
The IGBT model can be used to determine circuit parameters and external circuit conditions. It has been shown that the Saber simulator can be readily enhanced to describe the steady-state and the dynamic characteristics for various ranges of static and dynamic conditions in which the device is intended to be operated. The model has been used to describe the behavior of this circuit using the Saber IGBT model.

VI. CONCLUSIONS

The previously developed physics-based model for the IGBT is suitable for implementation into general purpose simulators. To incorporate the IGBT model into the Saber simulator, the model is formulated such that the currents between the terminal nodes are expressed in terms of the system variables, where several system variables are introduced to account for the nonintegrable capacitance formulas, for the implicit emitter-base capacitance, and for the bias-dependent model parameters. The resulting Saber IGBT model performs well and describes experimental results accurately for the range of static and dynamic conditions in which the device is intended to be operated. The model has been used to describe the steady-state and the dynamic characteristics for various external circuit conditions. It has been shown that the Saber IGBT model can be used to determine circuit parameters and component ratings in the design of protection circuits. The basic Saber IGBT model can be readily enhanced to describe the characteristics of IGBT's manufactured using the various power MOSFET technologies.

REFERENCES


Allen R. Hefner, Jr. (S‘84–M‘84–SM‘93) was born in Washington, DC, on June 29, 1959. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland in 1983, 1985, and 1987, respectively.

He joined the Semiconductor Electronics division of the National Institute of Standards and Technology (formerly the National Bureau of Standards) in 1983. He is currently Project Leader for the Electrical and Thermal Characterization Project in the Device Technology Group of the Semiconductor Electronics Division at NIST. His research interests include characterization, modeling, and circuit utilization of power semiconductor devices. He is the author of 20 publications in IEEE TRANSACTIONS and conference proceedings.

Dr. Hefner received the U.S. Department of Commerce Silver Medal Award for his pioneering work in modeling advanced power semiconductor devices for electro-thermal circuit simulation. He is also the recipient of an IEEE Industry Applications Society prize paper award. He was an instructor for the IEEE Power Electronic Specialist Conference tutorial course (1991 and 1993). He has served as a program committee member for the IEEE Power Electronics Specialist Conference (1991–1994) and as the IEEE Industry Applications Society Transactions Review Chairman for the Power Electronics Devices and Components Committee (1989–1994).

Daniel M. Diebolt (M‘80) received the B.S.E.E. degree from the University of Michigan, Ann Arbor, in 1982, and the M.S.E.E. and M.B.A. degrees from Rensselaer Polytechnic Institute, Troy, NY, in 1986 and 1988, respectively.

He is presently a marketing manager with Analog Inc., Beaverton, OR. His research activities are in the areas of simulation and modeling of power electronics and control systems for automotive and aerospace applications.