Automating Thermo-Mechanical Warpage Estimation of PCBs/PCAs using a Design-Analysis Integration Framework

Authors:
Manas Bajaj (Georgia Tech), Russell Peak (Georgia Tech), Dirk Zwemer (AkroMetrix), Thomas Thurman (Rockwell Collins), Lothar Klein (LKSoft), Giedrius Liutkus (LKSoft), Kevin Brady (NIST), John Messina (NIST), Mike Dickerson (InterCAX)
Abstract

Accurate prediction, validation and reduction of thermally-induced PCB warpage are critical for enhancing manufacturing yield and reliability in time-to-market driven electronics product realization.

In this paper, we describe a methodology to simulate thermally-induced warpage of PCBs and PCAs. We will demonstrate this analysis methodology using the following path: read ECAD designs from Mentor Board Station, identify features relevant to warpage analysis, create idealized analysis models, select solution technique and create solver-specific models (e.g. ANSYS models for finite-element solution), identify warpage-hotspots and calculate metrics to assist PCB/A designers in reducing warpage. We shall also present initial results from experimental verification of this technique using Shadow Moiré (TherMoiré®) method.


Project page: http://eislab.gatech.edu/projects/nist-warpage/
Contents

- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results
- Methodology
  - MRA-based Design Analysis Integration Framework
- Conclusion
Electronics Product Realization
**Warpage - Definition**

- **WARPAGE** is out of plane deformation of the artifact, caused by differential (non-homogenous) shrinkage or expansion of elements composing the artifact.

\[ \delta = \left( \alpha_b L^2 \Delta T \right) / t \]

- **Out of plane deformation of a linear element**
- **Warpage of 2D artifacts (basic modes)**
  - Saddle Deformation
  - Bowl Deformation

\[ L: \text{ Undeformed Length; } t: \text{ Undeformed Thickness; } \Delta T: \text{ Temperature Change; } \alpha_b: \text{ Specific Co-efficient of Thermal Bending} \]
PCA/B Warpage - Illustration

Undeformed Shape

Deformed Shape
Warpage – Factors and Effects
[after Ding, 2003; et al.]

Estimated Impact: $100M / year

Factors:
- CTE mismatch
- Material rigidity
- Thermal conductivity
- Geometric size & aspect ratio
- Component layout
- Temperature variation
- Temperature gradient

Consequences:
- Misregistration
- Delamination
- Die crack
- Solder fatigue
- Solder shortening
- Solder opening

Estimated Impact: $100M / year
Warpage – Impact and Requirements

Ref: Thinking Globally, Measuring Locally
Editorial by Patrick Hassell, AkroMetrix

Impact

- Low manufacturing yield and high rework of interconnects
  - Lack of co-planarity of component footprints
  - Fine pitch technology
  - Low solder paste volume

Requirements

- Managing warpage requirements
  - Enforce local warpage requirements
  - Relax global warpage requirements
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Complex Features Affecting Thermo-Mechanical Behavior

**PCB level**

Footprint occurrence
This comprises of four lands, in this case. The component sits atop the lands.

Complete trace curve not shown

Mechanical (Tooling / Drilling) Hole

Circuit Traces

via

land

plated through hole

Comprised of straight lines and arcs (primitive level)
Complex Features Affecting Thermo-Mechanical Behavior

**PCA level**

- Isometric View
- Side View

![Diagram](www.shinko.co.jp)

Photo: www.shinko.co.jp
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- Warpage – Definition and Impact
- PCB/A features affecting warpage
- Requirements for Warpage Analysis
- Results and Validation
- Methodology and Tools
  - Multi-Representation Architecture
  - Beta-level PWB warpage estimation tool
  - Prototype-level PWAB warpage estimation tool
- Conclusion
Requirements for Warpage Analysis

- Availability of a rich product model
  - ECAD design details
  - PCB layer stackup details
  - Material behavior and properties

- Analysis model creation capabilities
  - Idealized PCB/A features
  - Boundary conditions
  - Thermal loading

- FEA Model creation and solution capabilities
  - FE mesher
  - FE solver
Rich Product Model

Traditional Tools
- Zuken
- Eagle
- Mentor Graphics

AP210 interface

Electrical CAD Tools
- XaiTools
- PWA-B

Systems Engineering Tools
- Doors
- Slate

Manufacturing product model components integrated into STEP AP210-based model

Gap-Filling Tools
- XaiTools PWA-B
- pgpdm
- LKSoft, ...

Core PDM Tool

Instance Browser/Editor
- STEP-Book AP210, SDAI-Edit, STI AP210 Viewer, ...

PWB Stackup Tool, ...

STEP-Book AP210,
SDAI-Edit,
STI AP210 Viewer,
STEP AP210 (ISO 10303-210)

Domain: Electronics Design

~950 standardized concepts (many applicable to other domains)

Development investment: $O(100 \text{ man-years})$ over ~10 years

Configuration Controlled Design of Electronic Assemblies,
their Interconnection and Packaging

Interconnect Assembly

Printed Circuit Assemblies (PCAs/PWAs)

Product Enclosure

External Interfaces

Die/Chip

Packaged Part

Printed Circuit Substrate (PCBs/PWBs)
STEP AP210 (ISO 10303-210)

Scope

**Functional Models**
- Functional Unit
- Interface Declaration
- Network Listing
- Simulation Models
- Signals
- Test Bench

**Assembly Models**
- User View
- Design View
- Component Placement
- Material product
- Complex Assemblies with Multiple Interconnect

**Design Control**
- Geometric Dimensioning and Tolerancing

**Configuration Mgmt**
- Identification
- Authority
- Effectivity
- Control
- Net Change

**Requirements Models**
- Design
- Constraints
- Interface
- Allocation

**Rules Models**
- Design
- Manufacturing
- ...

**Component / Part Models**
- Analysis Support
- Package
- Material Product
- Properties
- “White Box” / “Black Box”
- Test Bench

**Interconnect Models**
- User View
- Design View
- Bare Board Design
- Layout templates
- Layers

**Geometric Models**
- 2D
- 3D
- CSG, Brep…
- EDIF, IPC, GDSII compatible “trace” model

http://www.ap210.org
Example Design in STEP Book AP210 Pro (PCB Layout View)

Originating ECAD Model from: Mentor Board Station
Current Tool: STEP Book AP210 v2.3
Current Model based on: STEP AP210
Example Design in XaiTools PWA-B 2.0.b1 Stackup Editor

Originating ECAD from: Mentor Board Station
Current Tool: XaiTools PWA-B v2.0.b1
Current Model based on: STEP AP210
PCB Warpage Analysis Model Creation

Context Attributes
- Thermal loading profile
- Boundary Conditions (mostly displacement)
- Idealize PWB stackup as a layered shell

Given:
- Thermal loading profile
- Boundary Conditions (mostly displacement)
- Idealize PWB stackup as a layered shell

AP210-based Manufacturing Product Model

Single Layer View

Effective Material Property Computation

Context

Building Block-based Analysis Model

Top view of “effective” grid elements in top layer of the PCB

Side view of the PCB with “effective” grid elements across the strataums

Grid (Sieve) Size
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Chopped PCB Regions for Analysis in XaiTools PWA-B 2.0.b1

First (Top) Design Layer

Second (Bottom) Design Layer
Example Design - Finite-Element Model Creation and Solution Input to ANSYS

ANSYS APDL-based description for creating and solving the finite-element model

XaiTools PWA-B 2.0.b1
Example Design

Out-of-plane deformation

Conditions

\( \Delta T = 125 \text{ deg. C} - \text{uniform heating from 25 deg. C to 150 deg. C} \)

Outermost edges along Y-axis are fully constrained
Example Design - Coeff. Of Thermal Bending results in XaiTools PWA-B 2.0.b1
Overall Process - Circuit Board Stackup Design & Warpage Analysis Using AP210 (WIP)
GIT and NIST EEEL in collaboration with AkroMetrix, InterCAX/LKSoft, and Rockwell Collins

STEP AP210-based Product Model

Analysis Building Block Model (idealized bodies with effective material properties)

Feedback

PCB Warpage Profile (given: thermal profile + boundary conditions)

http://eislab.gatech.edu/projects/

Identification of warpage “hotspots” on a PCB

CTB Map (smeared property to identify material distribution)
PCA Warpage Analysis Model Creation

c1. Component designs / libraries (e.g., chip packages like plastic ball grid arrays (PBGAs))

c2. Idealized component designs (APMs) and simulation templates (CBAMs)

b1. PCB design

b2. Idealized PCB design (APM) and simulation template (CBAM)

b3. Analytical system model (ABBs) (~50 analytical multilayer shell bodies)

a1. PCA design plus b1. PCB design

Idealized PCB

Idealized PCA

d1. Combined analytical system model (~1000+ analytical bodies)

Idealized components

e1. Combined FEA mesh model (SMM) (~50K elements avg. per complex component)
Case 1:
1 PBGA 265 on top

Automated PCA design warpage analysis
Case 2: 2 PBGA 265s on top
Case 3: 3 PBGA 265s on top

Qualitative comparison
- Different board & components (somewhat similar)
- Good warpage shape results comparison
- Similar total warpage results (2.2 mils vs. 1.7 mils = ~23% delta)

[Ding, 2004] results

InterCAX results

*XaiTools Electronics (SBIR Phase 1 prototype)*
Case 4: PCA with top & bottom PBGAs

Analytical model in IDA-STEP as imported from AP203

Produced by idealizing AP210-based PCB design (from Zuken Visula ECAD tool) and combining with idealized chip package models in XaiTools Electronics prototype (XE), and exporting as AP203.
Case 4: PCA with top & bottom PBGAs
Mesh model in Abaqus as imported from native Abaqus format
Case 4: PCA with top & bottom PBGAs
FEA mesh model in Abaqus (cont.)

Mesh in dense chip package solder ball regions

Auto-generated mesh between chip package substrate layers, solder balls, and PCB layers

(same region in full wireframe view)
**Case 4: PCA with top & bottom PBGAs**

Solved FEA model in Abaqus

Preliminary Warpage Results
(to be further validated in Phase 2)

**Results - Case 4:**

- Demonstrated FEA meshing feasibility (main challenge)
- Good results, trends, and compatibility with similar cases [Ding, 2004; Powell, 2006]
- Results reveal anticipated asymmetric effects
  - High fidelity PCB model considers local feature density differences
- Future work will try more effective idealizations (ex. shells) & correlate with physical measurements
Case 5: PBGA Chip Package on Sample PCB
Deformation magnitude results: PCA 6230 (with PBGA 441)

Known Results [Zeng, 2004; Shinko]

InterCAX SBIR Phase 1 Results

XCP + Patran pre-processing
Abaqus solving and Patran post-processing

XE + Simmetrix pre-processing
Abaqus solving and post-processing

Phase 1 Results - Case 5
- Excellent comparison of deformation pattern
- Very good comparison of max. warpage values (1.61 mils vs. 1.50 mils = ~7% delta)
  - Possible deviation causes: different meshing approach, different solver version, etc.
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Multi-Representation Architecture (MRA) for Design Analysis Integration

Tree View

Bare PWB

Electrical

Mechanical

Manufacturability

Warpage

PTH Fatigue

Layered Shell Effective Materials Properties

Finite Element

Manufacturing
Product Model

Analysis
Product Model

Context-Based
Analysis Model

Analysis
Building Blocks

Solution
Method Model
Multi-Representation Architecture (MRA) for Design Analysis Integration

Stepping-Stone Model View

Manufacturing Product Model
(STEP AP210-based)

Analyzable Product Model

Context-Based Analysis Model

Analysis Building Block

Solution Method Model

Solution Tools
(ANSYS, ABAQUS ...)

APM
Printed Wiring Assembly (PWA)

Component
Solder Joint
Printed Wiring Board (PWB)

CBAM

Component
Solder Joint
PWB

ABB

Solution Tools
(ANSYS, ABAQUS ...)

SMM

Printed Wiring Board (PWB)

Solder Joint

Component
MRA-based Model Browser

Design Artifacts – PCA, PCB, Components, etc.

Design Libraries

Product-specific Analysis Models

Reusable Analysis Models

Solution Models and Results – Finite Element Model, etc.
Status of Tools

- **STEP Book AP210 Pro v2.3 (LKSoft)**
  - Import Mentor Board Station designs

- **XaiTools PWA-B v2.0.b1 (Georgia Tech)**
  - Stackup Editor
  - Bare Board Warpage Analysis

- **XaiTools Electronics v1.0 Prototype (Georgia Tech)**
  - PCA Warpage Analysis
Invited Collaboration

- Collaboration Opportunities
  - Test Case Providers
  - Users of this service
  - Users of the tool
- Future Extensions
  - Bare board stackup design & warpage tool
    - Detailed stackup
  - PCA warpage tool
    - Alpha-level refinement
Summary

- Use of rich product models to drive high-fidelity analyses
- **Stackup Design and Warpage Analysis**
  - Bare board stackup design and warpage analysis
  - PCA warpage analysis
  - Initial validation
- **Methodology and Tools**
  - MRA-based design-analysis model management pattern
  - Beta level bare board stackup design and warpage tool
  - Early prototype PCA warpage analysis tool
NIST Disclaimer

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