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Field effects of current crowding in metal-MoS$_2$ contacts

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Gate assisted contact-end Kelvin test structures and gate assisted four-probe structures have been designed and fabricated to measure the field effects of current crowding at the source/drain contacts of top-gate MoS$_2$ field effect transistors. The transistors exhibited n-type transistor characteristics. The source/drain contact resistance was measured by using both gate-assisted Kelvin and gate-assisted four-probe structures. The values of contact resistance measured by these two test structures are significantly different. The contact-front contact resistance obtained from the four-probe structure is strongly influenced by field effects on current crowding, while the contact-end resistance obtained from the Kelvin test structure is not. The metal-MoS$_2$ contact current transfer length, $L_T$, can be determined from the comparison between these two measurements. $L_T$ was observed to increase linearly with increasing gate voltage. This work indicates that the contact characteristics can be more precisely measured when both gate-assisted test structures are used. © 2016 AIP Publishing LLC.

Top-gated FETs have a larger contact resistance as compared to back-gated ones. Because, unlike back-gated devices, the carrier density in MoS$_2$ under source/drain metal contacts will not change at higher positive gate bias in top-gated transistors. Our previous work has shown that using the gate-assisted test structures is an excellent approach to measure properties of the metal contacts to low-dimensional materials. Here, we present a study on current crowding in metal-MoS$_2$ contacts determined by using both gate-assisted Kelvin structures and four-probe structures where the channel current is effectively tuned by a top gate.

We fabricated Ag-contacted bilayer MoS$_2$ transistors with Au/Ti/Al$_2$O$_3$ top gates on SiO$_2$/Si substrate. Our devices show good n-type current-voltage (I-V) characteristics. Then gate assisted Kelvin structure and four-probe method were used to analyze the contacts. The contact resistance extracted from both methods is significantly different because the position where the voltage is sampled is different. By comparing the contact resistance extracted from both methods, we found that the current transfer length ($L_T$) of Ag-contact on MoS$_2$ transistors ranged from 114.3 nm to 128.5 nm, which increased with increasing gate voltage. The channel sheet resistance, which is measured by the four-probe method, is larger than the contact resistance. This indicates that the MoS$_2$ transistors are channel-dominant. Our results have shown that the gate affects not only the channel resistance but also the current crowding at the contacts.

In this work, the MoS$_2$ was grown on a 285 nm SiO$_2$/Si substrate via chemical vapour deposition (CVD). During the CVD of MoS$_2$, Mo$_x$ and sulfur are used as the precursors. In detail, an alumina crucible with 5 mg MoO$_3$ powder was placed in the center of a tube furnace. An alumina crucible with 1.5 g was placed at the
Plotted here is the integrated intensity from 340 cm\(^{-1}\) (Fig. 1(c)) shows that the separation between the two major metal contacts were deposited on a MoS\(_2\) triangle flake to five S/D contacts. Therefore, all four channels share a gate covers the whole structure including the channels and finally, 5 nm Ti/50 nm Au was deposited as top gate. The top plane modes. The optical contrast and Raman map suggest that the MoS\(_2\) flake thickness is quite uniform. Raman spectrum of a representative point on the uniform MoS\(_2\) flakes (Fig. 1(c)) shows that the separation between the two major peaks is 21 cm\(^{-1}\), indicating these are two-layer MoS\(_2\) flakes.

To fabricate MoS\(_2\) MOSFETs, first, the MoS\(_2\) flakes on the substrate were located with an optical microscope. Conventional lithography processes were then applied to define the device structures. 5 nm Ag/50 nm Au was deposited on MoS\(_2\) as the S/D contacts. Ag was chosen because it has been reported for forming a good contact on WSe\(_2\),\(^{33}\) which is a similar material to MoS\(_2\). And our previous work shows that Ag forms a smooth and solid film on MoS\(_2\) which makes the carrier transport efficiently across the contacts.\(^{34}\) Five parallel metal contacts were deposited on a MoS\(_2\) triangle flake to form the FETs, gate assisted Kelvin test structures and four-probe structures with the same contacts. Then, a rectangular MoS\(_2\) channel was defined by O\(_2\) plasma etching. To integrate the gate dielectric, 1 nm Al was deposited on MoS\(_2\) and then oxidized in air as a seeding layer before the atomic layer deposition (ALD) of 30 nm Al\(_2\)O\(_3\). This will promote gate dielectric quality.\(^{35}\) The ALD of Al\(_2\)O\(_3\) was performed at 300°C with trimethylaluminum (TMA) and H\(_2\)O as precursors. Finally, 5 nm Ti/50 nm Au was deposited as top gate. The top gate covers the whole structure including the channels and five S/D contacts. Therefore, all four channels share a common gate. A schematic of device structure and scanning electron microscopic image of two adjacent channels and three contacts are shown in Figs. 2(a) and 2(b), respectively. The channel length (\(L_C\)) and width (\(W\)) are 370 nm and 4 \(\mu\)m, respectively. And the contact length (\(L_C\)) is 1.09 \(\mu\)m.

The devices were then measured by a semiconductor parameter analyzer (Hewlett-Packard\(^\circ\) 4156) in a probe station (Cascade\(^\circ\) summit semi-automated probe station) at room temperature. Figs. 2(c) and 2(d) show the I-V characteristics of a typical MoS\(_2\) FET with details mentioned above. The channel current is normalized to current per one \(\mu\)m in channel width. The transistor exhibits strong n-type device characteristics which is similar to those reported by other groups.\(^{9,15–17}\) The small hysteresis in \(I_D-V_G\) measurement indicates a good quality of Al\(_2\)O\(_3\) which is used as gate dielectric. Also, the On-state current of these FETs is quite large compared to the published results.\(^{9,15–17,36,37}\) The threshold voltage and field effect mobility are extracted from the linear fitting of \(I_D-V_G\) curve measured at \(V_D=50\) mV. The threshold voltage is \(-10.2\) V. At a small \(V_{DS}\), the field effect mobility of the transistor can be extracted from the linear mode \(I_D\), expressed as

\[ \mu_{ef} = \frac{L}{W V_{DS}} \frac{1}{C_{ox}} \frac{\partial I_D}{\partial V_{GS}}. \]

Here, \(V_{GS}\) should be large enough and \(V_{DS}\) should be small to keep the transistor working in linear mode. The value of the field effect mobility of our device is 7.8 cm\(^2\) V\(^{-1}\) s\(^{-1}\). This value is close to some recent publications using similar device structures.\(^{37,38}\) The linear relationship between drain current (\(I_D\)) and drain voltage (\(V_D\)) at low voltage indicates good S/D contacts.

In order to evaluate the metal contacts on MoS\(_2\), contact resistance measurements using both gate assisted Kelvin test structure and gated assisted four-probe test structure were performed on these MoS\(_2\) FETs. Figs. 3(a)–3(c) show the contact resistance measured by the gate assisted Kelvin test structure. The measurement set-up is illustrated in Fig. 3(a). In the

![Fig. 1. MoS\(_2\) crystal characterization: (a) Optical image of typical MoS\(_2\) flakes grown on SiO\(_2\)/Si substrate. The scale bar is 5 \(\mu\)m. (b) Raman mapping of the MoS\(_2\) flakes in (a). The intensity in the image is the integrated signal intensity from 340 cm\(^{-1}\) to 430 cm\(^{-1}\). (c) Raman spectrum of a representative point on MoS\(_2\) flakes compared to exfoliated 1L MoS\(_2\).](image)

![Fig. 2. Device structure and I-V characterization of a representative MoS\(_2\) FET: (a) Schematics of MoS\(_2\) FETs. (b) SEM image of a MoS\(_2\) transistor. Scale bar in this image is 1 \(\mu\)m. (c) \(I_D-V_G\), and (d) \(I_D-V_D\) characteristic. The orange arrows indicates the voltage sweeping direction during the measurement and the black arrows pointing to the corresponding scale labels for the data shown in linear and log scale.](image)
Kelvin test structure, $I_D$ is driven through the middle contact by the MoS$_2$ FET on the left. Non-local voltage ($V_{23}$) was measured between the middle and right electrodes. Since a common gate is applied to the whole test structure, both channels are biased to the same conditions. Because there is no current flowing through the right channel and contact on the right, $V_{23}$ is measured as the voltage drop at the end edge of MoS$_2$ underneath the middle contact (source of the FET on the left). As shown in Fig. 3(b), the curves of $V_{23}$ versus $I_D$ at different gate voltage are quite linear, indicating an Ohmic contact. The overlap of the $V_{23}$ curve at different $V_G$ shows that the contact resistance obtained by Kelvin test method ($R_{C,K}$) is not affected by $V_G$. Fig. 3(c) shows the variation of $R_{C,K}$ which is the slope extracted from the linear fitting of $V_{23}$–$I_D$ curves. The value of $R_{C,K}$ is only a little more than 20 $\Omega$, which is much lower than the contact resistance extracted from other methods in previous publications.\textsuperscript{22,28,29}

Then, a gate assisted four-probe measurement was carried out to obtain the contact resistance and further understand the contact behaviour. The measurement set-up is shown in Fig. 3(d). A voltage source was connected to the S/D contacts at the ends to drive the current through the channel under the gate voltage varying from $-5$ V to 0 V. The $I_D$ and the voltage difference between the second and third contacts ($V_{23}$) are measured at the same time. Based on previous publications, the transfer length ($L_T$) is typically in hundreds of nm scale.\textsuperscript{28,29} The contact length we used in the two middle contacts is comparably large. So, the voltage distribution across the two middle contacts must be accounted for.\textsuperscript{39} The voltage drop on the two middle contacts would contribute a resistance of $R_{M}$ to the total resistance we measured. So

$$R_{14} = 2R_C + 2R_M + 3R_{ch},$$

(2)

$$R_{23} = R_M + R_{sh}.$$  

(3)

$R_{14}$ and $R_{23}$ can be extracted by the linear fitting of $V_D$ and $V_{23}$ vs. $I_D$. $R_C$ is the contact resistance. $R_M$ can be viewed as parallel resistance of $2R_C$ and the resistance of MoS$_2$ under the contact. Theoretically, the sheet resistance of MoS$_2$ under the contacts should not change under different gate bias, because the contact metal shields it from the top gate.\textsuperscript{40} But, as we will discuss later, it may not be the reality. To simplify the calculation, we assumed that the sheet resistance of MoS$_2$ under the contacts is the same with the one in the channel. So $R_M$ and the channel resistance ($R_{ch}$) can be estimated

$$R_M = \frac{2R_C \cdot L_C}{W} \cdot \frac{R_{sh}}{2R_C + \frac{L_C}{W} R_{sh}},$$

(4)

$$R_{ch} = \frac{L_C}{W} R_{sh}.$$  

(5)

Combining Eqs. (2)–(5), we can solve $R_C$ and $R_{sh}$

\[
R_C = \frac{\left(1 - \frac{L_C}{L_G}\right) (R_{14} - 3R_{23}) + \sqrt{\left(1 - \frac{L_C}{L_G}\right)^2 (R_{14} - 3R_{23})^2 + \frac{4L_C}{L_G} (R_{14} - 3R_{23})(R_{14} - 2R_{23})}}{4},
\]

(6)

\[
R_{sh} = \frac{W}{L_G} \left( (R_{14} - 2R_{23}) - \frac{\left(1 - \frac{L_C}{L_G}\right) (R_{14} - 3R_{23}) + \sqrt{\left(1 - \frac{L_C}{L_G}\right)^2 (R_{14} - 3R_{23})^2 + \frac{4L_C}{L_G} (R_{14} - 3R_{23})(R_{14} - 2R_{23})}}{2} \right).
\]

(7)

FIG. 3. Gate assisted contact measurement: (a) Set-up of gate assisted Kelvin measurement; (b) $V_{23}$–$I_D$ measured at different $V_G$; (c) $R_{C,K}$ extracted from the linear fitting of $V_{23}$ and $I_D$ at different $V_G$; (d) Set-up of gate assisted four-probe measurement; (e) Channel sheet resistance at different $V_G$ measured by four-probe test structure; (f) Contact resistance ($R_C$) extracted from four-probe measurement.
Figs. 3(e) and 3(f) show the channel sheet resistance and contact resistance varying with gate voltage, respectively. The channel conductance is effectively tuned by the gate (see Fig. 3(e)) as expected. It is quite interesting that the contact resistance is also effectively tuned by the gate (see Fig. 3(f)). Compared to the channel resistance, the contact resistance is higher in these transistors, indicating that these are contact-dominated MoS$_2$ transistors.

It should be noted that $R_C$ is much larger than $R_{C,K}$ and strongly depends on the gate voltage. This provides clear evidence of current crowding at metal-MoS$_2$ contacts. According to transmission line model (TLM),$^{40-43}$ illustrated in Fig. 4, the current transport in a contact is concentrated at the front of the contact. The voltage at the front of the contact is much higher than the voltage at the end of the contact. The voltage distribution in MoS$_2$ under a metal contact can be expressed as $^{40-43}$

$$V(x) = \frac{\sqrt{\rho_C R_{sh} \cosh((L_C - x)/L_T)}}{W \sinh(L_C/L_T)} I_D, \quad (8)$$

where $\rho_C$ is contact resistivity, $x$ is the position on MoS$_2$ where the voltage is sampled, $L_C$ is the contact length (1.09 μm in our devices), $R_{sh}$ is the sheet resistance of MoS$_2$ under contact, and $L_T$ is current transfer length of MoS$_2$. It is the distance which the current would penetrate into the MoS$_2$ under the metal contact, i.e., the length of MoS$_2$ used as effective contact. In a conventional bulk FET, $L_T$ is defined as

$$L_T = \sqrt{\frac{\rho_C}{R_{sh}}}. \quad (9)$$

Here we still use Eq. (8) to express the voltage distribution under the contact in our devices. In the Kelvin test structure, the non-local voltage at the middle contact ($V_{23}$) is measured at the end of the contact (i.e., $x = L_C$), so

$$R_{C,K} = \frac{V(L_C)}{I_D} = \frac{\sqrt{\rho_C R_{sh}}}{W \sinh(L_C/L_T)}. \quad (10)$$

However, in the four-probe method, the voltage on the contact is measured at the front of the contact (i.e., $x = 0$), so

$$R_C = \frac{V(0)}{I_D} = \frac{\sqrt{\rho_C R_{sh} \cosh(L_C/L_T)}}{W \sinh(L_C/L_T)}. \quad (11)$$

It is clear that the ratio of $R_C$ to $R_{C,K}$ can be expressed as

$$\frac{R_C}{R_{C,K}} = \cosh(L_C/L_T). \quad (12)$$

Therefore, the ratio of $R_C$ over $R_{C,K}$ is highly dependent on the ratio of the contact length over transfer length. Since $R_C$ is much larger than $R_{C,K}$ in our devices, the $L_C$ is much larger than $L_T$. The current is concentrated at the front part of the contact. As shown in Fig. 5(a), the $L_T$ of the MoS$_2$ devices can be extracted from the ratio of $R_C$ over $R_{C,K}$. The $L_T$ is weakly affected by the gate bias: it increases from 114.3 nm when $V_G$ equals to −5 V to 128.5 nm for $V_G$ equals to 0 V. These values are slightly larger than those in the previous work which also shows $L_T$ increased with increasing gate voltage in bottom gated MoS$_2$ transistors.$^{28}$

In this work, $L_C$ is much larger than $L_T$. So, $R_C$ can be approximately expressed as

$$R_C \approx \frac{\rho_C}{WL_T}. \quad (13)$$

The contact resistivity $\rho_C$ can be extracted from Eq. (13). As plotted in Fig. 5(b), $\rho_C$ sharply decreases with increasing gate voltage. This means that the contact resistivity of the S/D contacts in a MoS$_2$ transistor is strongly dependent on gate voltage. So, the contacts also contribute to the switching of these MoS$_2$ transistors. It may indicate that, in addition to minimizing contact resistance, the gate voltage can also be used to modulate the barrier so that the device performance can be optimized where a barrier at the metal contact is preferred, such as in solar cells and photovoltaic devices. Unlike bulk devices, the band bending in 2D MoS$_2$ transistors takes place along the current transport direction instead of the vertical direction.$^{22}$ Even though the top-gate would not affect the charge density under the contact,$^{90}$ it affects the barrier height and width along the edge of the contacts. As the gate bias gets higher, the band in the channel bends downward. However, the energy band of MoS$_2$ under the contact would not change because it is shielded from the top gate by the metal contact. The barrier between the MoS$_2$ under contact and in the channel gets lower and narrower. As a result, the contact resistivity gets lower. Meanwhile, the current transfer length increases a little from 114.3 nm to 128.5 nm. It may be a result of the limited density of state in 2D MoS$_2$. At higher gate bias, the current density is higher. The limited density of state in 2D MoS$_2$ requires a larger area for the carrier injection. Correspondingly, the transfer length increases. In total, the lower contact resistivity and larger transfer length result in a lower contact resistance at higher gate bias.

In summary, n-type MoS$_2$ FETs were fabricated with a conventional lithography process. All MoS$_2$ transistors exhibited good n-type I-V characteristics. The contacts of the MoS$_2$ transistors were analyzed with gate assisted contact measurement structures including Kelvin test structure and four-probe test structure. Contact resistance is smaller than the channel resistance, indicating that these MoS$_2$ transistors are channel-dominant devices. The values of contact resistance extracted from Kelvin test structure and four-probe test structure are significantly different. According to TLM, this difference is due to the current crowding and the different
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FIG. 5. (a) Transfer length and contact resistivity of MoS2 transistors: (a) current transfer length and (b) contact resistivity at different VGS.