Planarized process for single-flux-quantum circuits with self-shunted Nb/Nb$_{x}$Si$_{1-x}$/Nb Josephson junctions

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Abstract—We describe our process for fabricating single-flux-quantum circuits for applications in communications metrology, advanced computing, and quantum information. The process flow includes four superconducting metal layers, one junction layer, one palladium-gold bias resistor layer, and a contact pad layer. Planarization using chemical-mechanical polishing is performed on the two lower insulating layers. This process is based on Josephson junctions with niobium superconducting electrodes and self-shunted, amorphous niobium-doped silicon barriers on the insulating side near the metal-insulator transition. The barrier material is deposited by co-sputtering silicon and niobium, with the junction properties controlled by the relative sputtering powers and the duration of the barrier deposition step. The profiles of the deposition rates across 3-in (76.2 mm) wafers give a corresponding radial profile of the critical current density $J_c$ that increases by $\sim 46\%$ from the center to the edge of the wafer. To characterize our process, we show data for niobium metal quality and magnetic penetration depth, wire and via inductances, and via critical currents. The uniformity of the junction critical current $I_c$ across a wafer was measured on test chips with 2.7-$\mu$m-diameter junctions. Within a 5 mm $\times$ 5 mm area, the standard deviation of $I_c$ was $\sim 2\%$ for chips near the center of the wafer and up to $\sim 7\%$ for chips near the edge. We also describe process improvements and innovations under development aimed at increasing circuit density and high-speed performance.

Index Terms—Josephson junctions, self-shunted junction, superconducting electronics, Josephson devices, single flux quantum, fabrication process.

I. INTRODUCTION

The application of state-of-the-art digital single-flux-quantum (SFQ) electronics for metrology, advanced computing, and quantum information requires an advanced process for fabricating these circuits [1]–[3]. The fabrication process that we have developed and used for over two decades for voltage standards circuits [4] is based on only two superconducting metal layers. Although this is sufficient for fabricating series arrays of Josephson junctions embedded in coplanar waveguide (CPW) microwave circuits, it cannot be used to make complex SFQ circuits. For these circuits, a new fabrication process is required that provides a minimum of four superconducting metal layers and utilizes planarization. After an initial development stage, this new SFQ process is now being used to fabricate mixed-signal SFQ circuits to extend quantum-based waveform synthesis from megahertz [5] to gigahertz frequencies as part of a program to develop advanced calibration tools for the telecommunications industry. An early result of this effort was the synthesis of waveforms with frequencies up to 4 GHz with -74 dBm output power [6]. This process will also be integrated with others at the NIST Boulder Microfabrication Facility to produce superconducting circuits for advanced computing and quantum information applications.

II. FABRICATION PROCESS

The circuits are fabricated on 3-in (76.2 mm), p-doped silicon wafers with a thermal oxide layer of 150 nm. As shown in Fig. 1, the circuits contain four niobium (Nb) superconducting layers (labeled M0 to M3 from bottom to top) for ground plane, interconnects, transmission lines, and inductors. There is also a layer of amorphous niobium-silicide (Nb$_x$Si$_{1-x}$) that defines the barriers of the Josephson junctions (JJ) and resides between M1 and M2. There are also two palladium-gold (Pd-Au) normal metal layers for biasing resistors (RS) and for contact pads (layer not shown). Either the bottom or top Nb layer may be utilized as the ground plane, as shown in the cross-sectional images obtained by focused ion beam scanning electron microscopy (FIB-SEM) in Fig. 2. Wiring layers are made of Nb deposited via magnetron sputtering and etched using sulphur hexafluoride (SF$_6$) reactive ion etching (RIE).

All photolithography steps are done using the same positive tone imaging resist. For each layer the spin speed is set to obtain the appropriate resist thickness for the desired resolution and tolerance to dry etching. Alignment and exposure is done with an i-line stepper with a resolution of 0.4 $\mu$m and 60 nm overlay.

Josephson junctions are made by in-situ deposition of the Nb base electrode (BE), co-sputter deposition of Nb and Si for the barrier material, and Nb deposition of the counter electrode.
An important and distinctive feature of our fabrication process is the broad tunability of the electrical properties of these junctions. The properties are adjusted by changing the Nb sputter rate for a fixed Si rate as well as the thickness of the barrier. An additional benefit of Nb$_x$Si$_{1-x}$ barriers is that their thickness is 5 to 10 times greater than that of insulating aluminum oxide barriers for the same value of critical current density $J_c$, which can translate to better junction uniformity, especially for high values of $J_c$.

For voltage standard circuits such as the one in [5], the metallic barriers are tuned to give self-shunted, overdamped junctions with high critical currents $I_c$ (close to 10 mA). For fast, energy-efficient SFQ digital circuits, we tune the nonmetallic barriers so that the junctions are critically damped or slightly underdamped, $I_c < 0.5$ mA, and the characteristic frequency $f_c$ is increased for high-speed operation ($f_c = I_c R_n / \Phi_0$, where $\Phi_0$ is the magnetic flux quantum and $R_n$ is the JJ normal resistance) [7]. We have previously fabricated circuits with externally-shunted JJs containing pure amorphous Si barriers (i.e., without Nb doping) using a simpler process than the one described here [8]. While such externally-shunted junctions can be readily introduced into our new process, only self-shunted JJs are discussed here.

The barrier material for the self-shunted junctions with Stewart-McCumber parameter $\beta_c \approx 1.5$ (where $\beta_c = 2\pi f_c R_n C$ and $C$ is the junction capacitance) is deposited by co-sputtering with the Nb gun at 15 W power and the Si gun at 200 W power. This corresponds to $\sim 9$ % Nb atomic composition, while the metal-insulator transition of Nb occurs at $\sim 11$ %. $I$-$V$ curves for a single junction with $\sim 9$ % composition and a diameter of 2.1 $\mu$m are shown in Fig. 3. They show the highly nonlinear resistance of the junction all the way to the gap voltage. The conductance mechanism for normal electrons across the junction is via elastic and inelastic resonant tunneling through localized states in the barrier. As described by the Glazman-Matveev theory [9], [10], the quasiparticle current $I_{qp}$ can be separated into linear and nonlinear terms according to $I_{qp} = G_l V + G_{nl} V^{7/3}$. This nonlinear $I$-$V$ relationship is included in our simulations by compiling a nonlinear resistor using Verilog-A and importing it into the simulation program [11].

Self-shunting of the junctions is critical for future scaling to higher circuit densities, because it eliminates the external shunt resistors that would otherwise be necessary and consume significant chip area. Eliminating these shunts also eliminates the associated parasitic inductances and thus further enables faster circuits.
process and our SFQ cell library. The smallest JJ’s in these circuits were designed with a diameter of 2 µm and an $I_c = 125$ µA. When we increase $J_c$ to obtain higher SFQ circuit operating speeds, we will reduce the junction size in order to maintain a similar minimum value of $I_c$. Setting 0.7 µm as the lower limit of the JJ diameter based on a conservative estimate of our photolithographic capabilities corresponds to a maximum of $\sim 30$ kA/cm$^2$ for $J_c$ with this process.

Insulator layers consist of silicon oxide ($SiO_x$) deposited by electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD). Backside helium flow during deposition ensures that the wafer temperature remains below 100 °C. Planarization, which is done on insulating layers I0 and I1, follows the caldera method [12] shown in Fig. 4. First, an oxide layer 500 nm thick is deposited to cover the 200 nm thick layer of patterned metal. The oxide is then covered with photo resist in areas where the underlying metal has been etched. By timed etch of the oxide to 300 nm, calderas are left on an otherwise flat surface. Finally, chemical-mechanical polishing (CMP) removes 100 nm of the remaining oxide, leaving a flat surface of oxide 200 nm thick over the metal and over vias. This method avoids the need to add metal fill to obtain a flat surface after CMP. The mean oxide thickness obtained with this process can vary by ± 20 nm from run to run.

Resistors have a sheet resistance of 2 Ω per square and consist of a 135 nm layer of Pd-Au alloy with $\sim 2$ nm bottom and top titanium (Ti) adhesion layers. The layers are e-beam evaporated on a bilayer of lift-off resist and imaging resist. The lift-off resist is baked on a hot plate at 150 °C for 5 min. This is the highest temperature reached in our entire process and is lower than the temperature (200 °C) at which an increase in resistivity has been observed in insulating Nb$_2$Si$_{1-x}$ films annealed for similar periods of time as our baking step [13]. The contact pads to the resistor are made with a sputter deposition of Pd-Au with a bottom Ti adhesion layer and defined by a lift-off process.

Table I summarizes the thickness and material used for each layer in the process. The minimum feature sizes listed correspond to typical values currently used in circuit layouts and not the limits of our fabrication capabilities.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Target thickness (nm)</th>
<th>Material</th>
<th>Minimum feature size (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>200</td>
<td>Nb (sputtered)</td>
<td>1.0</td>
</tr>
<tr>
<td>I0</td>
<td>200</td>
<td>SiO$_x$ (PECVD)</td>
<td>0.75</td>
</tr>
<tr>
<td>M1</td>
<td>200</td>
<td>Nb (sputtered)</td>
<td>1.0</td>
</tr>
<tr>
<td>JJ</td>
<td>10</td>
<td>Nb$<em>2$Si$</em>{1-x}$ (co-sputtered)</td>
<td>1.5</td>
</tr>
<tr>
<td>I1</td>
<td>200</td>
<td>SiO$_x$ (PECVD)</td>
<td>0.75</td>
</tr>
<tr>
<td>RS</td>
<td>135</td>
<td>Pd-Au (evaporated)</td>
<td>0.75</td>
</tr>
<tr>
<td>M2</td>
<td>250</td>
<td>Nb (sputtered)</td>
<td>1.0</td>
</tr>
<tr>
<td>I2</td>
<td>300</td>
<td>SiO$_x$ (PECVD)</td>
<td>1.0</td>
</tr>
<tr>
<td>M3</td>
<td>350</td>
<td>Nb (sputtered)</td>
<td>1.0</td>
</tr>
<tr>
<td>Pads</td>
<td>200</td>
<td>Pd-Au (sputtered)</td>
<td></td>
</tr>
</tbody>
</table>

III. PROCESS CONTROL MEASUREMENTS

To characterize and monitor the process in each fabrication run, test structures are fabricated at multiple positions on the wafer.

A. Metal layers

For each Nb layer and the RS layer, electrical test structures are measured to obtain the sheet resistance and the actual width of the nominally 6 µm wide wires. Typical “missing wire widths,” defined as the difference between the nominal and measured widths, for each layer are as follows: M0,
0.25 μm; M1, 0.15 μm; M2, 0.5 μm; M3, 0.25 μm; and RS, < 50 nm. The same structures are also used to gauge the film quality by measuring the residual resistance ratio $R_{RRR} = R_{300K}/R_{10K}$ for each layer. $R_{RRR}$ values of Nb films deposited by sputtering on room temperature substrates typically range from 2 to 10, with higher values associated with higher purity films [14]. Typical $R_{RRR}$ values for our metal layers indicate acceptable quality films and are listed here: M0, 5; M1, 5.5; M2, 5.5; M3, 5.5; and RS, 1.2. A possible explanation for the lower value of M0 is its thinner deposition thickness (200 nm) compared to M1-M3; although the final thickness of M1 is 200 nm, it is deposited as 240 nm and then etched to 200 nm after the junction definition etch.

We extract the magnetic penetration depth $\lambda$ of our films from the dependence of the critical current $I_c$ of a large junction on the applied in-plane magnetic field [15]. The condition for a large junction is $L \geq L_J$, where $L$ is the lateral size of the junction and $L_J = [h/(2eJ_J\mu_0d)]^{1/2}$ is the Josephson penetration depth. Here, $J$ is the current density and $d = 2\lambda + t$, where $t$ is the barrier thickness. In general, the Josephson penetration depth $L_J$ gives a measure of the length within which dc currents in the junctions are confined near the edges of the junction. When the large-junction condition is met, we expect an asymmetry to develop in the Fraunhofer pattern of the critical current; the maximum is displaced from zero. For junctions where $L \approx L_J$ (yet still in the large-junction limit), this displacement is given by $\Phi_{\text{max}}/\Phi_0 = (1/4\pi)(L/L_J)^2$. Based on the position of the maximum, it is possible to extract $\lambda$.

The layout of the test structure, which includes a large JJ and a coil for applying flux, is shown in Fig. 5. The dimensions of the large JJ are 8.25 μm × 1.5 μm with thickness $t = 7.7$ nm. The coil wraps around the insulating layers I0 and I1 with wires in layers M0 (green in figure) and M2 (purple), producing an in-plane field perpendicular to the long dimension of the JJ. With $J_c = 3.7 \times 10^7$ A/m² for the junctions tested and the Fraunhofer data in Fig. 5, we obtain $\lambda = (60 \pm 5)$ nm.

**B. Inductors**

Superconducting quantum interference devices (SQUIDs) such as the one shown in Fig. 6 are used to measure the inductance of wires in the M0, M1, and M2 metal layers with M3 as the ground plane [16]. SQUIDs are fabricated with three wire widths (1 μm, 3 μm, and 5 μm) and three wire lengths for each width (83 μm, 45 μm, and 20 μm). Wire lengths are measured from center to center of the junctions. From the plot of inductance versus length for each wire width (bottom of Fig. 6), a linear fit gives the inductance per unit length for that specific wire width and layer; this removes the effect of parasitic inductances from the vias and the effect of sections of wires from other layers used to complete the circuit. Table II shows the measured inductances for each layer. Also shown are calculated values [17] that account for the missing wire widths, assuming $\lambda = 60$ nm. We did not quantify critical currents for these wire widths.

**C. Vias**

Series arrays of 100 vias between neighboring metal layers are used for continuity testing and to measure the critical current $I_c$ of the vias. Typical values are shown in Table III. The via critical current is dominated by the thinnest sections of metal in the via walls. As expected, $I_c$ is in general higher in larger vias than in smaller ones and higher in thicker metal layers than thinner ones (see Table I for thicknesses). Arrays of vias in SQUIDs are used to measure the inductance of 1 μm × 1 μm square vias. Measurements of M1-M2 and M1-M0 vias give an average inductance of 0.1 pH per via.
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D. Junctions

1) $J_c$ and Missing Radius Measurements: To determine the critical current density $J_c$, junctions of nine different sizes are fabricated in a process control chip. There are six sets of junctions in this chip, and each set has junctions of nine different sizes (all sets have the same sizes). Three sets have a single junction of each size, and three sets have an array of twenty junctions of each size. An automated measuring system that uses a switch matrix records I-V curves for each junction or array of 20 junctions and extracts the values of $I_c$ and $R_o$. This information is later compiled and analyzed to obtain $J_c$, $I_cR_o$, and the missing radius $r_0$ (i.e., the difference between the layout radius $r_L$ and the actual radius).

The values of $J_c$ and $r_0$ are obtained from graphs of $\sqrt{\Phi}$ vs. $r_L$, as seen in Fig. 7. With the relation $I_c = J_c\pi(r_L - r_0)^2$; the slope and $x$-intercept of a linear fit to the data give $J_c$ and $r_0$, respectively. In the example shown in Fig. 7, $J_c = 4.9 \times 10^7$ A/m² (4.9 kA/cm²) and $r_0 = 0.047$ μm.

2) Junction Capacitance: We extract the specific capacitance of the junction by measuring the resonance frequency of the loop inductance and the junction capacitance in a SQUID structure [18], [19]. These resonances are best observed in the I-V curves of the SQUIDs when applying a flux $\Phi = \Phi_0/2$.

In our case, the resonances are damped because the junctions are self-shunted and consequently difficult to observe. Using the formalism for resonances in low-Q Josephson interferometer devices [20], [21] and subtracting the contribution of the voltage-dependent nonlinear resistance of the junctions (described in Section II), a fit to the resonance peak is obtained. From this analysis, an estimate of the specific capacitance for self-shunted junctions is $C' = (310 \pm 20)$ fF/μm², with $J_c = 4.5 \times 10^7$ A/m² and $\beta_c \approx 1.5$.

3) Junction $J_c$ and $I_c$ Uniformity: Another process control chip contains 54 junctions of the same size that are wired so that each can be independently measured. This configuration is used to quantify the uniformity of the junction properties, especially the critical current, locally and across the wafer. We have a dedicated gun and target for the barrier Nb that is different from the ones used for wiring layers. This minimizes the change in barrier composition and thickness from a decrease in sputtering rate due to target erosion. We have installed a crystal rate monitor in the deposition chamber to track any change in the Si and barrier Nb deposition rates and adjust the sputtering settings as needed to obtain the desired composition.

The sputtering guns use 3-in targets located ~ 15 cm from the wafer, resulting in deposition rate profiles of the Si and the barrier Nb that cause $J_c$ to vary across the wafer. Since the substrate is rotating during deposition, this profile is radial. Measurements of film thicknesses on step height structures across the wafer show that the deposition rates decrease radially from the center to the edge of the wafer by 4.6% for Si and 2.6% for Nb, as shown in the top of Fig. 8. The calculated increase in Nb atomic percent of the barrier from center to wafer edge is about 0.2%.

$J_c$ depends both on barrier thickness and composition; thinner barriers and higher Nb content both contribute to
the increased values of $J_c$ towards the edge of the wafer. The bottom plot of Fig. 8 shows the measured $J_c$ vs. radial position. From the center to the exclusion zone (31.2 mm from center), this variation in $J_c$ is $\sim 46\%$. Also shown is a theoretical fit of the $J_c$ vs. radial position data, assuming an exponential dependence on barrier thickness that takes into account only the thickness profile and ignores the small change in composition. The outermost point was excluded from the fit and indicates that composition change must be included in the model to get an acceptable fit across the entire wafer.

Fig. 8. (top) Normalized deposition rate profiles of Si and barrier Nb films measured vs. wafer radial position. Also shown is the expected composition profile (Nb atomic %). (bottom) Measured radial profile of $J_c$ across the wafer. A reasonable fit to the data points for radii $\leq 25$ mm is shown, assuming an exponential dependence on barrier thickness and ignoring the small change in composition.

Histograms of $I_c$ values from single junctions of the same size measured in liquid helium are shown for a typical wafer in Fig. 9. The data show increasing spread towards the edge of the wafer. The reason for this is the deposition rate variation across the wafer of the sputtering sources discussed above. The 54 junctions are fabricated on 5 mm $\times$ 5 mm chips and are distributed along the chip perimeter, just inside the perimeter of contact pads. We fit the $I_c$ distribution to a normal distribution; the standard deviations, ranging from 2.2 % near the wafer center to 6.6 % at the edge, are shown for each chip position. The maximum distance between junctions on a single chip is 4.2 mm and is sufficient to show the effect of the deposition rate gradient, which is steepest near the edge of the wafer. A different chip layout with a maximum distance of 2 mm between junctions was measured from the same wafer, giving a standard deviation of 1.8 % for 58 junctions measured. For small SFQ circuits, an $I_c$ variation of 2 % is not an impediment to achieving good operating margins. In fact, the gradient in $J_c$ has the benefit of allowing the study of circuits with a range of $I_c$ values from a single wafer. However, as circuits become larger and more complex, improvements in the $J_c$ uniformity across the wafer will be necessary. We plan to replace the 3-in sputtering guns for Si and barrier Nb with 4-in guns and expect the resultant deposition rate profiles from wafer center to edge to reduce to $\sim 1\%$ and the $J_c$ uniformity to $< 10\%$. With this improvement, wafer-to-wafer variation becomes important and will be investigated by fabricating multiple lots targeted at the same $J_c$.

In addition to the rate profiles, a potential contributor to the $I_c$ variation is the roughness of the Nb on which the barrier is deposited. We are experimenting with smoothing layers in the base electrode to reduce the Nb roughness. Another option with potential to improve $I_c$ variation is to change the location of junctions to layer M0. M0 is expected to be the smoothest Nb layer because it is the first deposited layer on the smooth silicon oxide substrate and is deposited before any CMP process step. A test wafer with junctions on M0 showed $I_c$ standard deviations similar to the ones shown for the standard process but the distributions do not show “hot”
junction outliers with abnormally high values of $I_c$, such as the one junction shown in the histogram for chip G1 in Fig. 9. A likely cause of these hot junctions is residue from the CMP process. We have seen more residual slurry particles near the edges of the wafer than in the center, correlating with the location of hot junction incidents. Changes in residual stress in the Nb electrode films has been reported as one cause of $J_c$ variation in Nb/Nb$_x$Si$_{1-x}$/Nb junctions [22]. A future investigation will focus on how film stress from our process contributes to the nonuniformity of our junction properties.

IV. PROCESS DEVELOPMENTS

To achieve our goal of synthesizing waveforms with quantum-based amplitude accuracy in the millimeter-wave frequency range (>30 GHz), it will be necessary to make SFQ circuits clocked at greater than 120 GHz. This requires increasing the critical current density of the junctions, since the operating speed of these circuits scales approximately as $\sqrt{J_c}$ for fixed JJ damping [23].

To maximize circuit operating speeds, we will make junctions with $J_c = 10^9 \, \text{A/m}^2$ (100 kA/cm$^2$) and define them using electron-beam lithography. For this higher $J_c$, the JJ diameters need to decrease to ≤ 300 nm to keep $I_c$ below 0.5 mA to avoid self-heating. These diameters are beyond the capabilities of the stepper currently used in our process.

SFQ circuits, including T flip-flops and 12- and 16-stage static dividers, with self-shunted Nb-Si-barrier junctions and $J_c = 8.5 \times 10^8 \, \text{A/m}^2$ (85 kA/cm$^2$) have already been demonstrated at NIST [8]. The maximum operating frequency of the 12- and 16-stage static dividers was 300 GHz. We believe that the maximum frequency of those circuits was limited by (1) the fabrication process, which used an inferior e-beam lithography tool, and by (2) using circuit layouts that were optimized for low $J_c$ junctions. With our new process, we anticipate higher circuit yields and an increase in the maximum operating frequencies for the following reasons: (1) we will use a new e-beam writer that enables smaller, more uniform features sizes for better control of JJ critical currents and better alignment of the JJ via layer to the junction layer; (2) we have incorporated CMP into our process, which will improve the yield of contacts to smaller junctions and enable interconnects with higher current density and lower parasitics; and (3) we will use new design tools to optimize circuit parameters for high $J_c$ circuits.

As one strategy for increasing SFQ circuit densities, we plan to build circuits with geometric inductors replaced with the Josephson inductance of non-switching, vertically-stacked junctions [24], [25]. As a feasibility study, we have fabricated SQUIDs with both single junctions and three-junction stacks, and used both dc and RF electrical measurements to verify the performance of these junction stacks as compact inductors [26]. A process which combines small, high-$J_c$, self-shunted junctions and vertically-stacked JJ inductors enables significant reduction in the circuit area of many SFQ cells.

V. CONCLUSION

We have developed the first planarized fabrication process for SFQ digital and mixed-signal circuits based on self-shunted Nb/Nb$_x$Si$_{1-x}$/Nb junctions. The process flow includes one junction layer, four superconducting Nb metal layers, and one resistor layer, with CMP on two of the insulating layers. We show data from fabricated test structures that characterize the Nb metal quality and magnetic penetration depth, wire inductances, via inductances, and via critical currents and indicate our fabrication process is capable of making advanced SFQ circuits. We also have characterized the wafer center-to-edge profile for junction $J_c$ and the cross-chip $J_c$ variation and have identified solutions to reduce their variations.

By fabricating barriers with co-sputtered deposition of Si and Nb, we can tailor junction electrical properties over a wide range. This flexibility will enable us to utilize our process for a broad spectrum of SFQ circuits. With this process, we are developing SFQ-based circuits for gigahertz waveform synthesis with quantum-based output accuracy to be used as RF reference sources. In addition, we are also working to extend the process to yield circuits with higher speeds and circuit densities, in order to achieve our ultimate goal of circuits clocked above 100 GHz. Such capabilities are critical for next-generation applications in communications metrology, advanced computing, and quantum information.

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